8288-A,F,W

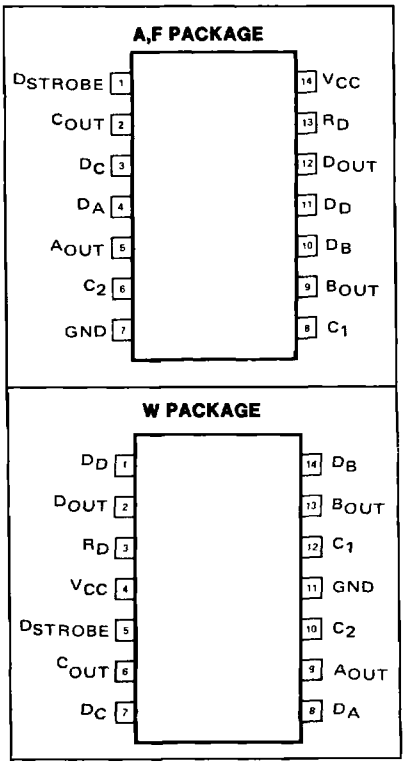
DESCRIPTION

The 8288 Divide by Twelve Counter is a four-bit subsystem consisting of divide by two and divide by six counters in a 14 pin package. For Divide-by-Twelve operation, output A is connected externally to the clock 2 input.

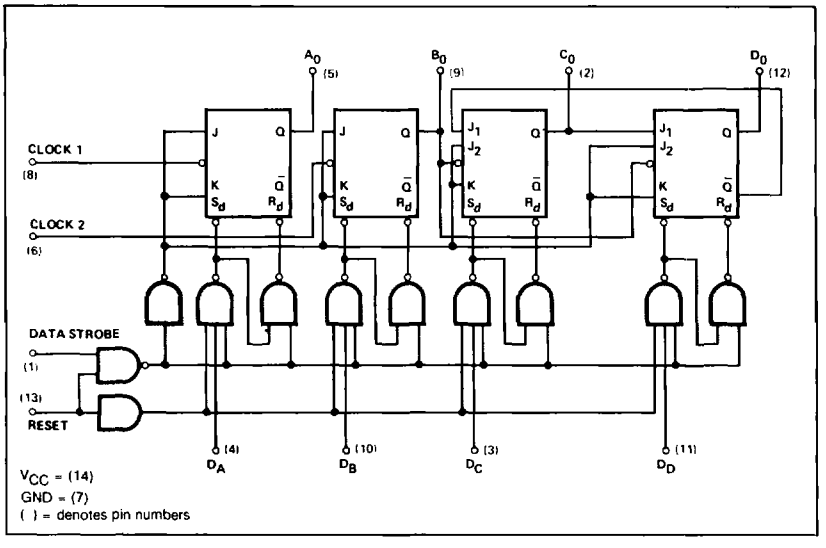
The 8288 has strobed paralleled data entry capability so that the counter may be preset to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at a "0" level. For additional flexibility, the 8288 is provided with a common reset. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative going) edge of the input clock pulse, however, there is no restriction on transition time since the individual binaries are level sensitive. The data strobe and reset functions are asynchronous with respect to the clock.

PIN CONFIGURATION



LOGIC DIAGRAM



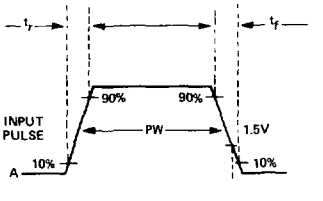
TRUTH TABLE

	OUTPUT			
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

SWITCHING CHARACTERISTICS T_A=25°C, V_{CC}=5V

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{on}	Turn-on delay time					
	Clock mode	Bit A,B,C,D		15	25	ns
	Data/strobe			20	35	
t_{off}	Turn-off time					
	Clock mode	Bit A,B,C,D		15	25	ns
	Data/strobe			25	40	
Toggle rate			20	25		MHz
t_{hold}	Hold time	V_{IN} = 0.8V:Reset=2V:				
	Strobe	Clock 1 = 2V: Clock 2 = Output A		25	35	ns
	Reset	Data strobe = 2V: V_{IN} = 0.8V: Clock 1 = 2V: Clock 2 = Output A		20	35	
$t_{release}$	Release time			30	40	ns
	Strobe					
	Reset			50	75	

AC WAVEFORMS

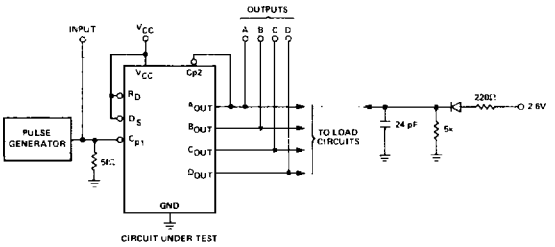


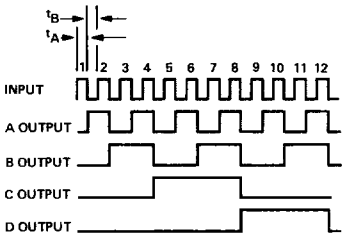
NOTE:
Input pulse notations apply unless otherwise specified

LOGIC

AC TEST FIGURES AND WAVEFORMS

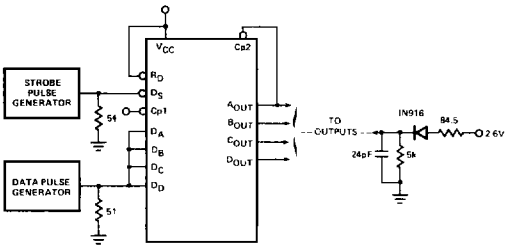
TOGGLE RATE

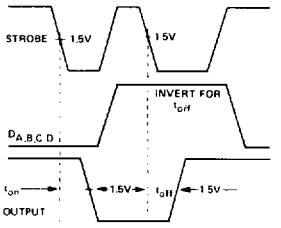




Input pulse
Amplitude = 3.4V
t_A = 100ns
t_r = 20ns
t_B = 300ns

DATA/STROBE t_{on} t_{off}

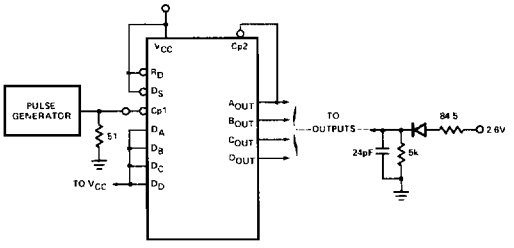


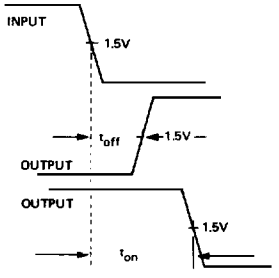


Input Pulse
Amplitude = 2.6V
t_r = t_f = 5ns

CLOCK MODE t_{on}/t_{off} DELAY

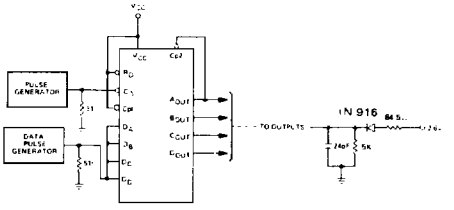
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with the following load circuit:

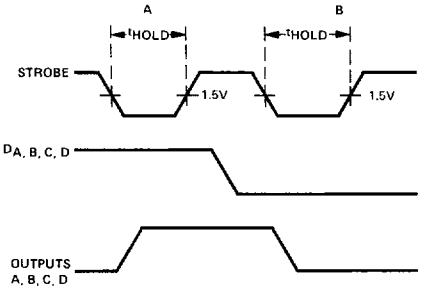




Input pulse:
Amplitude = 2.6V
P.W. = 30ns
t_r = t_f = 5ns

STROBE HOLD TIME



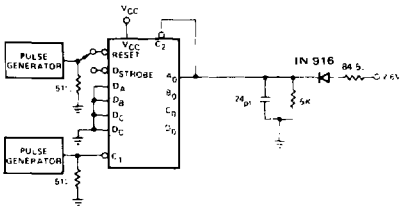


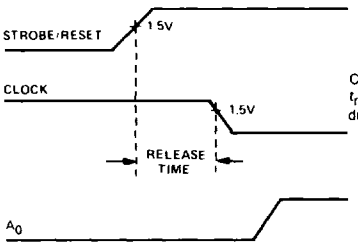
Input pulse
Amplitude = 2.6V
t_r = t_f = 5ns

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.

AC TEST FIGURES AND WAVEFORMS (CONT'D)

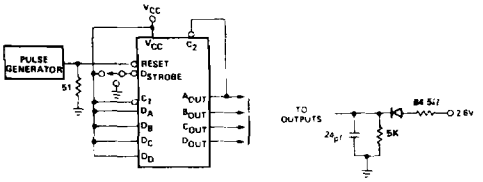
STROBE/RESET RELEASE TIME

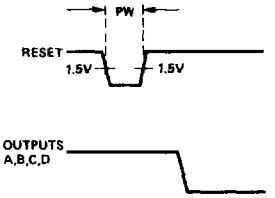




Clock, strobe/reset amplitude = 2.6V
$t_r = t_f$ = 5ns max. PRR = 1MHz 50% duty cycle

MINIMUM RESET PULSE WIDTH





Input pulse
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.

Note: outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

LOGIC

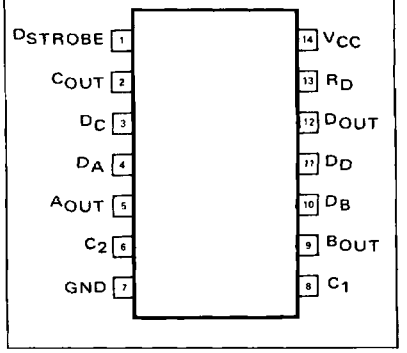
PRESETTABLE HIGH SPEED DECADE/BINARY COUNTER 8290/91

SPEED/PACKAGE AVAILABILITY

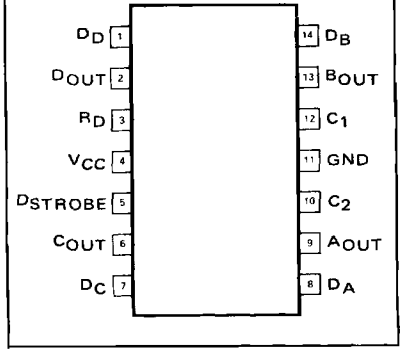
8290, 8291 A,F,W
82S90, 82S91 A,F

PIN CONFIGURATION

8290/91 82S90/82S91
A,F PACKAGE



8290/91
W PACKAGE



PIN DESIGNATIONS

CP1	Clock input to counter first stage (active low going edge)
CP2	Clock input to counter last three stages (active low going edge)
DS	Data Strobe Input for enabling data entry (active low)
RS	Reset Input for resetting all stages and outputs to zero (active low)
DA, DB, DC, DD	Data Inputs
AO, BO, CO, DO	Data Outputs

8290-A,F,W • 8291-A,F,W

DESCRIPTION

The 8290 Decade Counter and 8291 Binary Counter are high speed devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8290 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8291 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset lines produces "0" at all four outputs.

The counting operation is performed on the falling (negative going) edge of the input clock pulse.

Triggering requirements are compatible with any of the 8000 Series elements.

FUNCTIONAL DESCRIPTION

1. 82S90 Decade Counter

The 82S90 can be used in three basic modes as follows:

a. BCD Counter. The CP2 input must be connected to the AO output and CP1 receives the count input. The count sequence obtained is BCD in accordance with the truth table.

b. Bi-Quinary Counter. If a symmetrical output is required for divide by 10 operation, the DO output must be connected to the CP1 input and the count input applied to CP2. A symmetrical square wave is then obtained at AO of one-tenth the input frequency present at CP2 in accordance with the truth table.

c. Separate Divide by Two and Five Counters. Because the inherent structure of the counter is that of two separate divide by two and divide by five sections, no other connections are required for this mode of operation. An input presented to CP1 will appear at AO output at half the input frequency. An input presented to CP2 will appear at outputs BO, CO and DO as a binary divide by five count (i.e., from 0 = 000 to 4 = 100). Operation of the DS and RS inputs remain common to all four flip flops as with any other count mode.

2. 82S91 Binary Counter

The 82S90 can be used in two basic count modes as follows:

a. Binary Counter—For this mode of operation AO output must be connected to CP2 input and the count input connected to CP1. Subdivisions of the count input frequency then appear at AO = —2, BO = —4, CO = —8, DO = —16 as shown in the truth table.

b. Separate Divide by Two and Divide by Eight Counters—In similar manner to the 82S90 the 82S91 inherent structure allows separate use of the first and last three stages. In the first stage the input count frequency presented to CP2 appears at outputs BO = —2, CO = —4 and DO = —8 simultaneously. Operation of the DS and RS inputs remains common to all stages.

3. Operation of the DS Data Strobe and RS Reset Inputs:

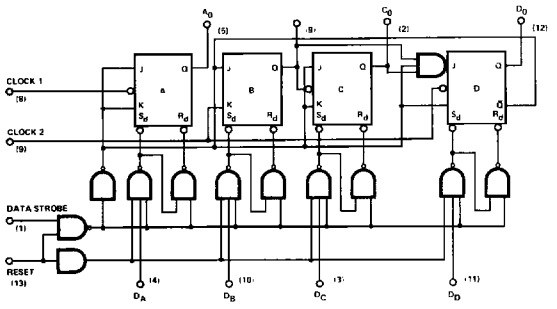
a. Data Strobe DS Input When DS = 0 the four stages of the 82S90/91 can be used as four separate latches with the outputs AO - DO following the data presented to the inputs DA - DD regardless of clock inputs.

With DS = 1 the four stages remain unchanged until the next clock inputs, which activate counting in accordance with the various modes described previously. The Reset RS inputs when low overrides DS as described below.

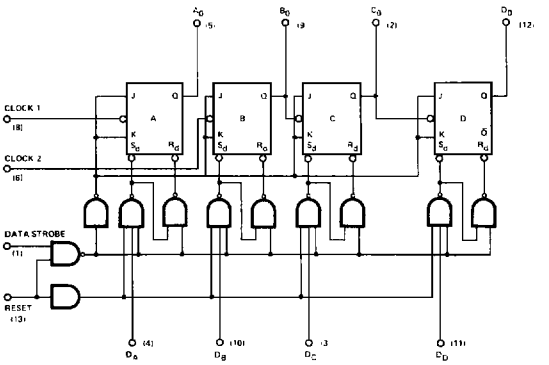
b. Reset RS Input With RS = 0 the clock inputs CP1/CP2 and DS input are overriden, all stages of the 82S90/91 are cleared and zeros appear at the counter outputs AO - DO. When RS = 1, operation is controlled by DS or DP1/CP2 clock inputs as described.

LOGIC DIAGRAM

8290



8291



V_{CC} = (14)
GND = (7)
( ) = denotes pin numbers

TRUTH TABLE

	8290								8291			
	BI-QUINARY(5-2)				DECADE (BCD)				BINARY			
INPUT	B_O	C_O	D_O	D_O	A_O	B_O	C_O	D_O	A_O	B_O	C_O	D_O
0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0	1	0	0	0
2	0	1	0	0	0	1	0	0	0	1	0	0
3	1	1	0	0	1	1	0	0	1	1	0	0
4	0	0	1	0	0	0	1	0	0	0	1	0
5	0	0	0	1	1	0	1	0	1	0	1	0
6	1	0	0	1	0	1	1	0	0	1	1	0
7	0	1	0	1	1	1	1	0	1	1	1	0
8	1	1	0	0	0	0	0	1	0	0	0	1
9	0	0	1	1	1	0	0	1	1	0	0	1
10									0	1	0	1
11									1	1	0	1
12									0	0	1	1
13									1	0	1	1
14									0	1	1	1
15									1	1	1	1

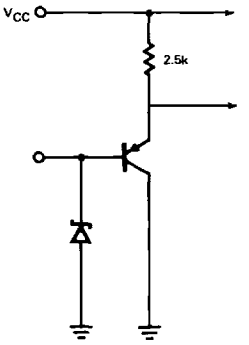
SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER		TEST CONDITION	8290/8291 MIN	8290/8291 TYP	8290/8291 MAX	82S90/82S91 MIN	82S90/82S91 TYP	82S90/82S91 MAX	UNIT
Propagation delay time									
t_{on}	Turn-on time								
	Clock mode	Bit A		12	25		9	12	ns
		Bits B,C,D		15	30		10	13	
	Strobed data	All Bits		31	42		15	22	ns
t_{off}	Turn-off time								
	Clock mode	Bit A		12	23		5	8	ns
		Bits B,C,D		15	25		6	10	
	Strobed data	All Bits		33	42		13	20	ns
t_w	Input pulse width								
	Strobe			15	25		5	10	ns
	Reset	Clock 2 = A_{out}		25	40		7	15	ns
$t_{release}$	Release time								
	Strobe/reset	Clock 2 = A_{out}		20	30		10	15	ns
Toggle rate			40	60					MHz
Switching test									
	Clock mode[1]				75				ns

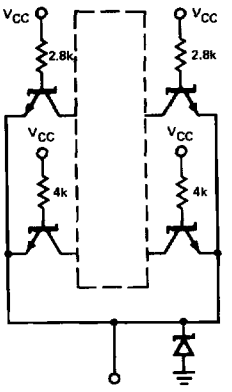
NOTES:
1. This test guarantees the device will reliably trigger on a pulse with 75ns fall-time

INPUT AND OUTPUT STRUCTURES

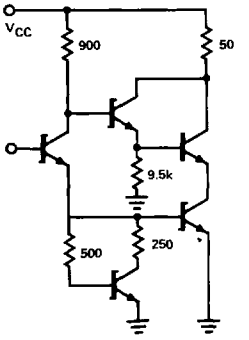
82S90,82S91
DATA, STROBE and RESET INPUTS



82S90,82S91
CLOCK INPUTS



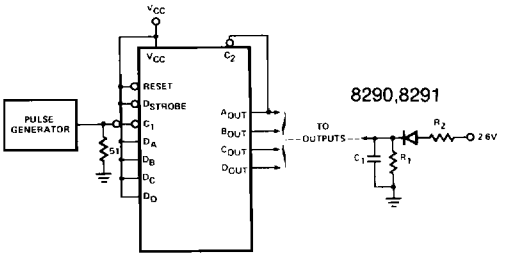
82S90,82S91
OUTPUTS

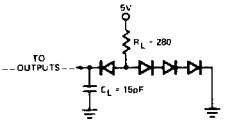


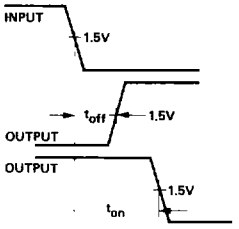
LOGIC

AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY



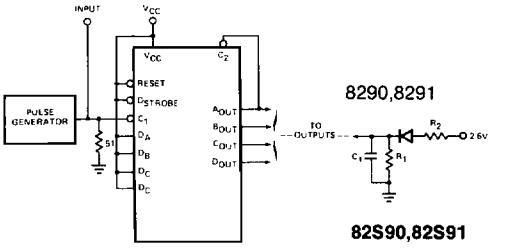


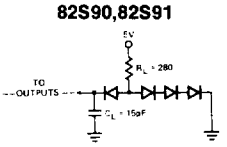


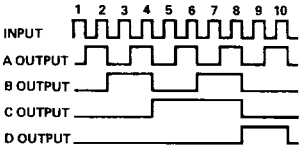
Input pulse:
Amplitude = 2.6V
PW = 30ns, 50% to 50%
$t_r = t_f$ = 5ns
PRR = 1MHz

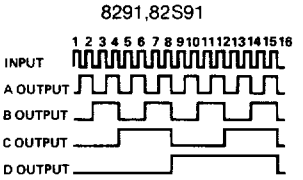
Note
t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.

TOGGLE RATE



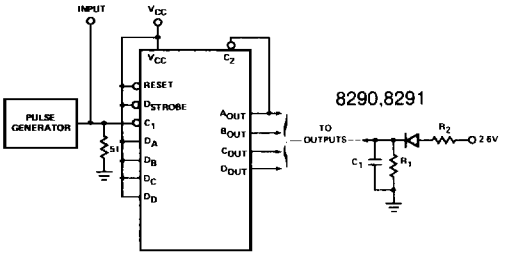


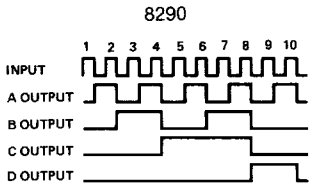


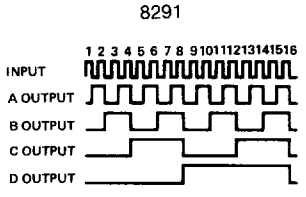


Input pulse:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.
PRR = 40 MHz, 50% duty cycle.

CLOCK MODE SWITCHING TEST

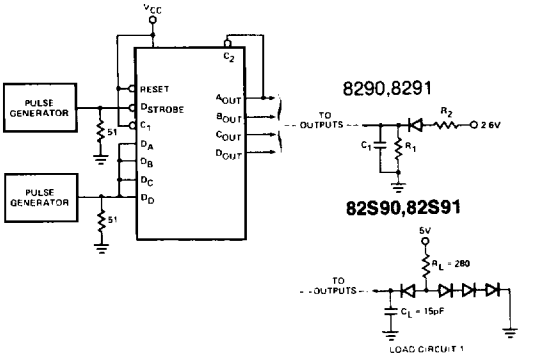




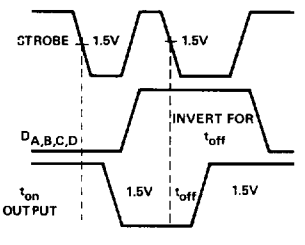


Input pulse:
Amplitude = 3.4V
PW = 100ns, 50% to 50%
PRR = 2.5MHz
t_r = 20ns, t_f = 75ns

STROBED DATA t_{on}/t_{off} DELAY



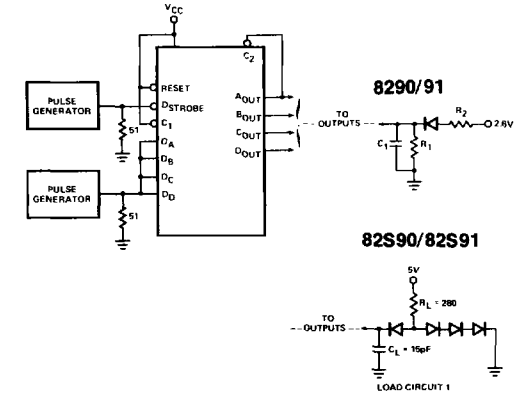
Strobe,
PA = 2.6V
PW = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f$ = 5ns

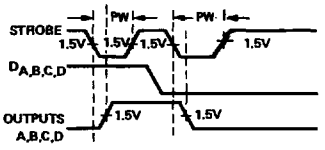


Data,
PA = 2.6V
PW = 500ns, 50% to 50%
PRR = 500kHz
$t_r = t_f$ = 5ns

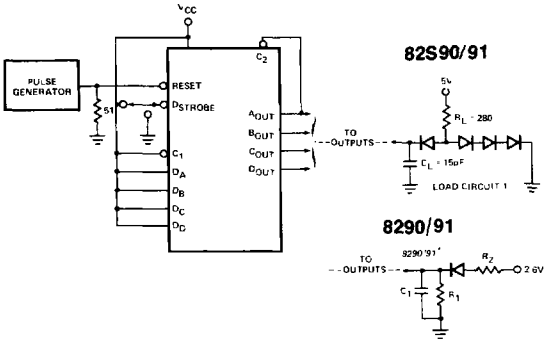
AC TEST FIGURE AND WAVEFORMS (CONT'D.)

MINIMUM STROBE PULSE WIDTH





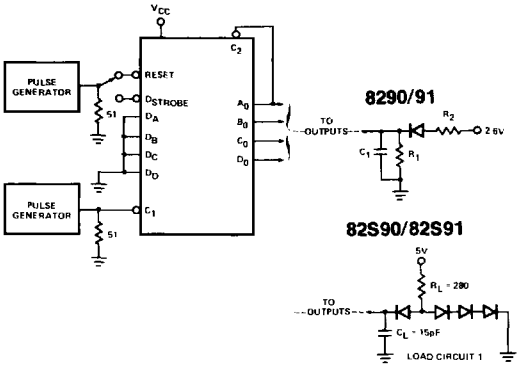
Input pulse:
Amplitude = 2.6V
$t_r = t_f = 5ns$

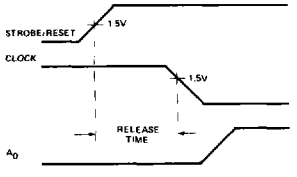


INPUT PULSE: Amplitude = 2.6V $t_r = t_f = 5ns$.

Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

STROBE/RESET RELEASE TIME





CLOCK STROBE/RESET
AMPLITUDE = 2.6V
PRR = 1MHz, 50% DUTY CYCLE
$t_r = t_f = 5$ ns MAX

NOTES
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.
3. All diodes are 1N916.
4. R1 = 20k, R2 = 146Ω C1 = 30pF

LOGIC