agere systems

Preliminary Product Brief, Rev. 1
June 2001

FW801A Low-Power PHY *IEEE* 1394A-2000 One-Cable Transceiver/Arbiter Device

Distinguishing Features

- **Compliant with *IEEE* Standard 1394a-2000, IEEE *Standard for a High Performance Serial Bus* Amendment 1.**
- Low power consumption during powerdown or microlow-power sleep mode.
- Supports extended BIAS_HANDSHAKE time for enhanced interoperability with camcorders.
- While unpowered and connected to the bus, will not drive TPBIAS on a connected port even if receiving incoming bias voltage on that port.
- Does not require external filter capacitors for PLL.
- Does not require a separate 5 V supply for 5 V link controller interoperability.
- Interoperable across 1394 cable with 1394 physical layers (PHY) using 5 V supplies.
- Interoperable with 1394 link-layer controllers using 5 V supplies.
- 1394a-2000 compliant common mode noise filter on incoming TPBIAS.
- Powerdown features to conserve energy in battery-powered applications include:
  — Device powerdown pin.
  — Link interface disable using LPS.
  — Inactive ports power down.
  — Automatic microlow-power sleep mode during suspend.
- Interface to link-layer controller supports Annex J electrical isolation as well as bus-keeper isolation.

Features

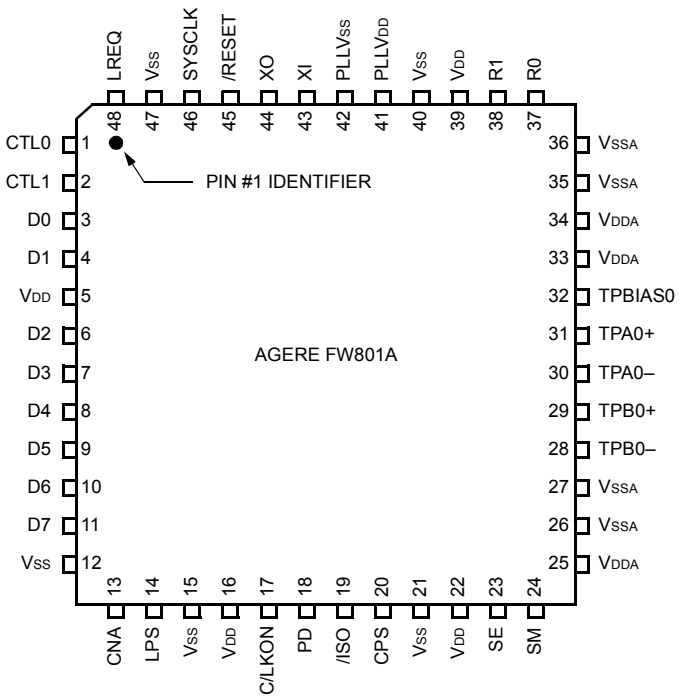
- Provides one compliant cable port at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s.
- Supports OHCI requirements.
- Supports arbitrated short bus reset to improve utilization of the bus.
- Supports ack-accelerated arbitration and fly-by concatenation.
- Supports connection debounce.
- Supports multispeed packet concatenation.
- Supports PHY pinging and remote PHY access packets.
- Supports full suspend/resume.
- Supports PHY-link interface initialization and reset.
- Supports 1394a-2000 register set.
- Supports LPS/link-on as a part of PHY-link interface.
- Supports provisions of *IEEE* 1394-1995 *Standard for a High Performance Serial Bus*.
- Fully interoperable with *FireWire*† implementation of *IEEE* 1394-1995.
- Reports cable power fail interrupt when voltage at CPS pin falls below 7.5 V.
- Separate cable bias and driver termination voltage supply for port.
- Meets *Intel*‡ *Mobile Power Guideline 2000*.

Other Features

- 48-pin TQFP package.
- Single 3.3 V supply operation.
- Data interface to link-layer controller provided through 2/4/8 parallel lines at 50 Mbits/s.
- 25 MHz crystal oscillator and PLL provide transmit/receive data at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s, and link-layer controller clock at 50 MHz.
- Node power-class information signaling for system power management.
- Multiple separate package signals provided for analog and digital supplies and grounds.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
† *FireWire* is a registered trademark of Apple Computer, Inc.
‡ *Intel* is a registered trademark of Intel Corporation.

Signal Information



Note: Active-low signals are indicated by "/" at the beginning of signal names, within this document.

5-7302.a (F) R.03

Figure 1. Pin Assignments

Description

The power-class bits of the self-ID packet do not have a default value. These bits can be initialized and read/written through the LLC using Figure 6-1 (PHY Register Map) of the *IEEE* 1394a-2000 standard. See Table 1 for address space of the Pwr_class register.

Table 1. PHY Register Map for the Cable Environment

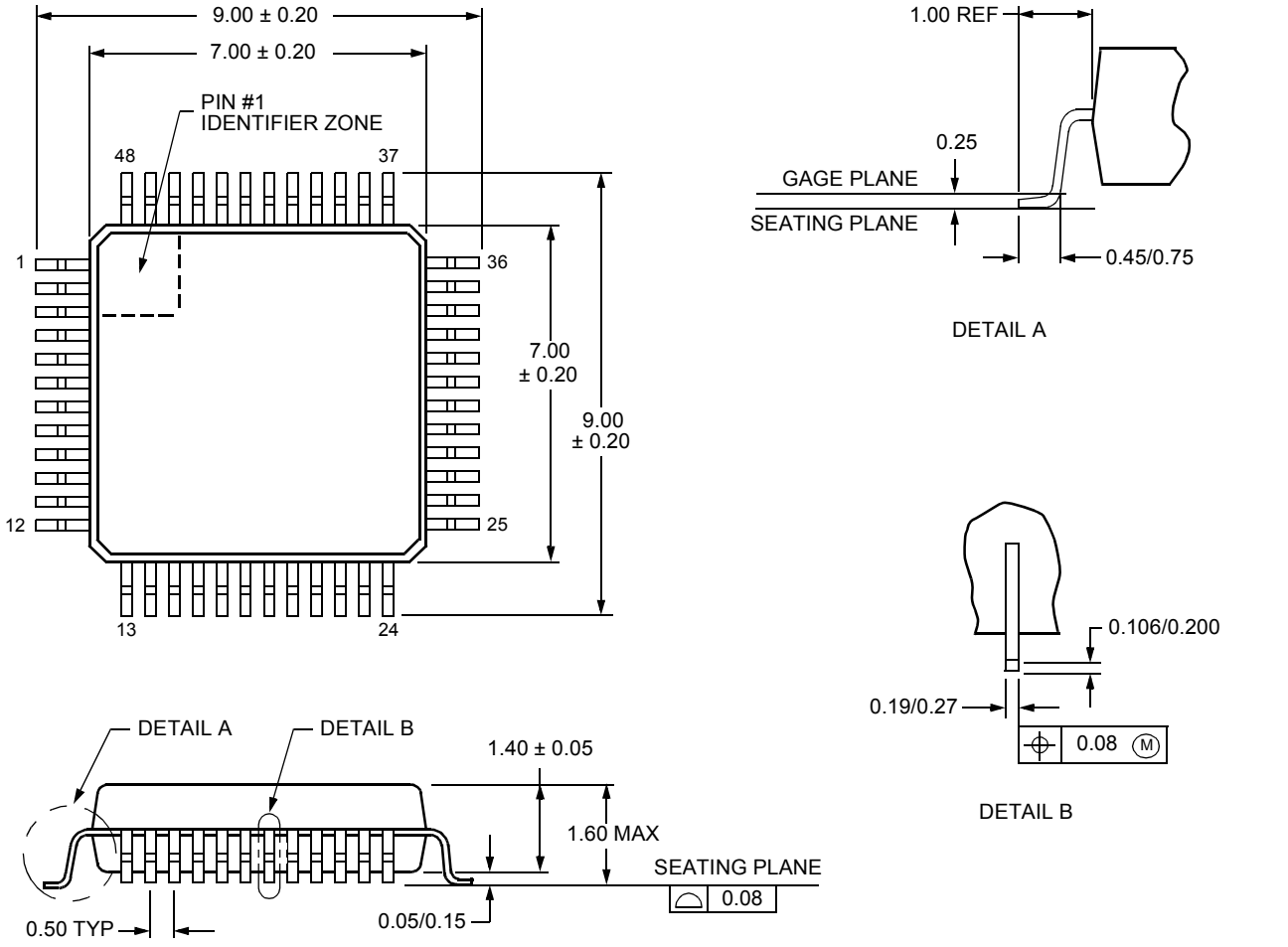
Address	Contents							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0000_2	Physical_ID						R	PS
0001_2	RHB	IBR	Gap_count					
0010_2	Extended (7)			XXXXX	Total_ports			
0011_2	Max_speed			XXXXX	Delay			
0100_2	LCtrl	Contender	Jitter			Pwr_class		
0101_2	Resume_int	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
0110_2	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
0111_2	Page_select			XXXXX	Port_select			
1000_2	Register 0 Page_select							
⋮	⋮							⋮
1111_2	Register 7 Page_select							

REQUIRED XXXXX RESERVED

Outline Diagrams

48-Pin TQFP

Dimensions are in millimeters.



5-2363 (F)R.08

1394 Application Support Contact Information

E-mail: **1394support@agere.com**

For additional information, contact your Agere Systems Account Manager or the following:
INTERNET: **http://www.agere.com**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Agere Systems Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Agere Systems Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Agere Systems (Shanghai) Co., Ltd., 33/F Jin Mao Tower, 88 Century Boulevard Pudong, Shanghai 200121 PRC
Tel. (86) 21 50471212, FAX (86) 21 50472266
JAPAN: Agere Systems Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: DATALINE: **Tel. (44) 7000 582 368**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 3507670** (Helsinki),
ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

June 2001
PB01-011CMPR-1

agere systems