XRD6622

CMOS 20MSPS, 12-Bit, High-Speed Analog-to-Digital Converter

FEATURES

- 12-Bit Resolution
- 20 MSPS Sampling Rate
- On Chip Bandgap Reference
- DNL = ±0.4 LSB, INL = ±1.7 LSB
- Internal S/H Function
- Single Power Supply: 5V
- Differential Input
- 100% Digital Test Coverage
- Low Power: 360mW
- Latch-Up Free
- ESD Protection: 2kV Minimum
- Power Down Mode (<1mW)
- 3 State Digital Outputs

APPLICATIONS

- Digital Scanners and Cameras
- Digital Copiers
- IR Image Digitizers
- Wireless Communications
- Video Capture
- XDSL Applications

GENERAL DESCRIPTION

The XRD6622 is a 12-bit Analog-to-Digital Converter. Designed using a standard 5V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The XRD6622 uses a fully pipelined architecture. Each stage is composed of a 1-bit analog-to-digital sub-converter (ADSC), a 1-bit digital-to-analog sub-converter (DASC), and a summing interstage amplifier (IAMP). By using stages with low resolution, high speed operation is possible. Digital correction logic removes any nonlinearity that would normally be caused by IAMP or ADSC offset. Overall ADC linearity depends only on capacitor ratio accuracy, thereby reducing performance variation with temperature. All internal circuitry is fully differential for improved noise rejection.

An on-chip sample-and-hold (S/H) minimizes the input "kick-back", thereby reducing ADC input driver requirements and improves accuracy for high frequency inputs. A high accuracy on-chip reference is also provided.

The device operates from a single +5V supply. Typical power consumption is 360mW at FS=20MSPS.

The XRD6622 is specified for operation over the industrial (0 to +85°C) temperature range.

BLOCK DIAGRAM

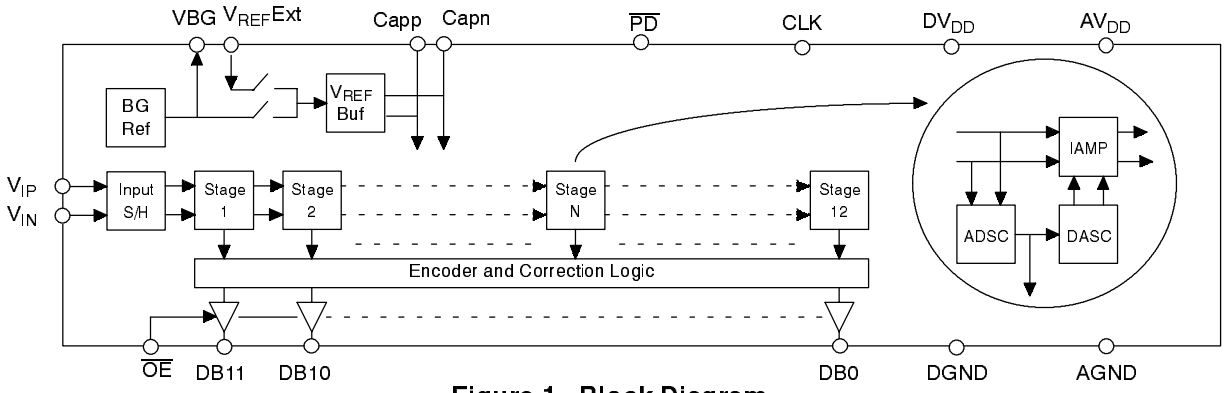
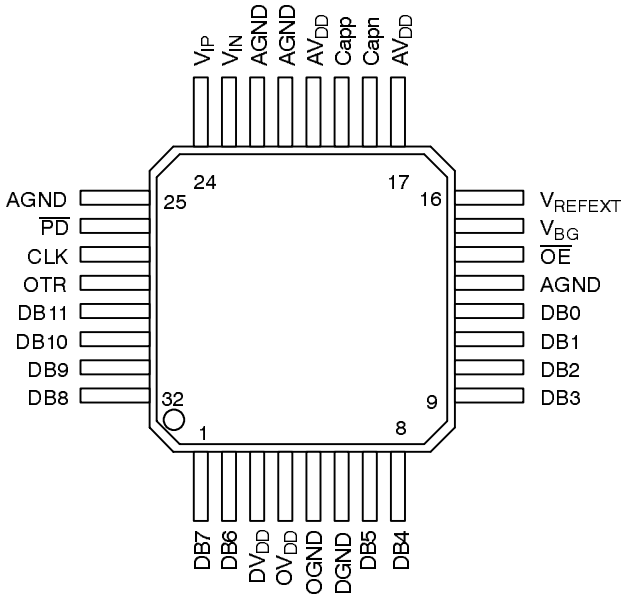


Figure 1. Block Diagram

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRD6622AIQ	32-pin TQFP (7 x 7 x 1.4mm)	0 to +85°C
XRD6622AIQ44	44-pin QFP (10 x 10 x 2.0mm)	0 to +85°C

PIN CONFIGURATION



32 Lead TQFP (7 x 7 x 1.4mm)

PIN DESCRIPTION

32 Pin TQFP

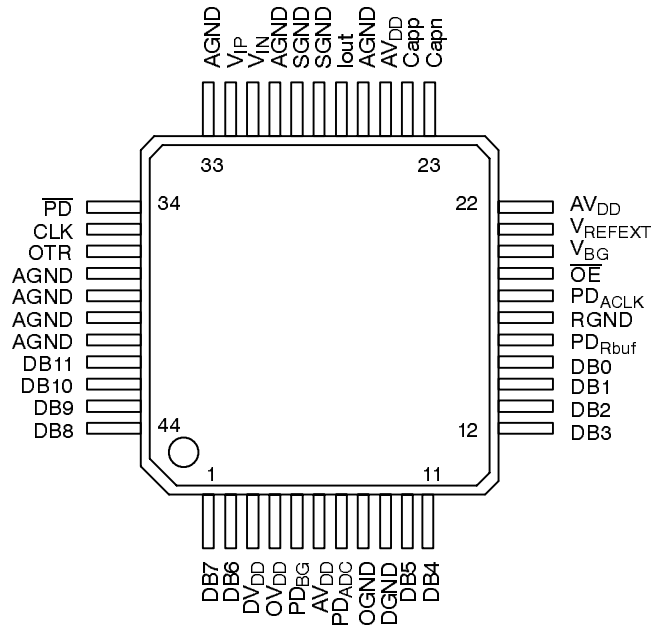
Pin #	Symbol	Description
1	DB7	**Data Output Bit 7.**
2	DB6	**Data Output Bit 6.**
3	DV_{DD}	**Digital Power Supply (Internal Decode Logic).**
4	OV_{DD}	**Digital Power Supply (Output Drivers).**
5	OGND	**Digital Ground (Output Drivers).**
6	DGND	**Digital Ground (Internal Decode Logic).**
7	DB5	**Data Output Bit 5.**

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
8	DB4	**Data Output Bit 4.**
9	DB3	**Data Output Bit 3.**
10	DB2	**Data Output Bit 2.**
11	DB1	**Data Output Bit 1.**
12	DB0	**Data Output Bit 0 (LSB).**
13	AGND	**Analog Ground.**
14	$\overline{OE}$	**Output Enable Control.**
15	V_{BG}	**Internal Bandgap Reference Voltage.**
16	V_{REFEXT}	**External Reference Input.**
17	AV_{DD}	**Analog Power Supply.**
18	Capn	**Connect External Decoupling Cap for Negative Reference.**
19	Capp	**Connect External Decoupling Cap for Positive Reference.**
20	AV_{DD}	**Analog Power Supply.**
21	AGND	**Analog Ground.**
22	AGND	**Analog Ground.**
23	V_{IN}	**Differential Negative Input.**
24	V_{IP}	**Differential Positive Input.**
25	AGND	**Analog Ground.**
26	$\overline{PD}$	**Power Down Control.**
27	CLK	**Sampling Clock.**
28	OTR	**Out of Range Indicator.**
29	DB11	**Data Output Bit 11 (MSB).**
30	DB10	**Data Output Bit 10.**
31	DB9	**Data Output Bit 9.**
32	DB8	**Data Output Bit 8.**

PIN DESCRIPTION (CONT'D)

32 Pin TQFP



44 Lead QFP (10mm x 10mm)

PIN DESCRIPTION

44 Pin QFP

Pin #	Symbol	Description
1	DB7	**Data Output Bit 7.**
2	DB6	**Data Output Bit 6.**
3	DV_{DD}	**Digital Power Supply (Internal Decode Logic).**
4	OV_{DD}	**Digital Power Supply (Output Drivers).**
5	PD_{BG}	**Power Down Control for Bandgap Voltage Reference.**
6	AV_{DD}	**Analog Power Supply.**
7	PD_{ADC}	**Power Down Control for ADC Core.**
8	OGND	**Digital Ground (Output Drivers).**
9	DGND	**Digital Ground (Internal Decode Logic).**
10	DB5	**Data Output Bit 5.**
11	DB4	**Data Output Bit 4.**
12	DB3	**Data Output Bit 3.**

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
13	DB2	**Data Output Bit 2.**
14	DB1	**Data Output Bit 1.**
15	DB0	**Data Output Bit 0 (LSB).**
16	PD_{RBUF}	**Power Down Control for Reference Buffer.**
17	RGND	**Analog Ground for Chopper-Stabailized Bandgap Reference.**
18	PD_{ACLK}	**Power Down Control for ADC Clock Generator.**
19	$\overline{OE}$	**Output Enable Control.**
20	V_{BG}	**Internal Bandgap Reference Voltage Output.**
21	V_{REFEXT}	**External Reference Input.**
22	AV_{DD}	**Analog Power Supply.**
23	Capn	**Connect External Decoupling Cap for Negative Reference.**
24	Capp	**Connect External Decoupling Cap for Positive Reference.**
25	AV_{DD}	**Analog Power Supply.**
26	AGND	**Analog Ground.**
27	Iout	**Internal Bias Current Measurement Point. (Default is no Connect).**
28	SGND	**Analog Ground (Connected to Substrate).**
29	SGND	**Analog Ground (Connected to Substrate).**
30	AGND	**Analog Ground.**
31	V_{IN}	**Differential Negative Input.**
32	V_{IP}	**Differential Positive Input.**
33	AGND	**Analog Ground.**
34	$\overline{PD}$	**Power Down Control.**
35	CLK	**Sampling Clock.**
36	OTR	**Out of Range Indicator.**
37	AGND	**Analog Ground.**
38	AGND	**Analog Ground.**
39	AGND	**Analog Ground.**
40	AGND	**Analog Ground.**
41	DB11	**Data Output Bit 11 (MSB).**
42	DB10	**Data Output Bit 10.**
43	DB9	**Data Output Bit 9.**
44	DB8	**Data Output Bit 8.**

ELECTRICAL CHARACTERISTICS

Test Conditions: Unless otherwise specified: AV_{DD} = DV_{DD} = 5V, FS = 20MHz (50% Duty Cycle); ADCFS = 4VPP, Using External Reference = 2.48V, T_A = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Key Features						
	Resolution	12			Bits	
FS	Maximum Sampling Rate	20			MSPS	
Accuracy						
DNL	Differential Non-Linearity	-0.7	±0.4	+0.7	LSB	
INL	Integral Non-Linearity		±1.7		LSB	Best Fit
	Input Referred Offset		50		mV	
	Input Referred Gain Error		2		%FS	
CMRR	Common Mode Rejection Ratio		64		dB	F_{IN}=100KHz
	DC PSRR from AV_{DD}		50		dB	
	DC PSRR from DV_{DD}		80		dB	
	Zero Error Drift		15		µV/°C	
	Gain Error Drift		0.003		%FS/°C	
Bandgap Reference						
V_{REF}	Reference Voltage	1.10	1.24	1.30	V	
TC_{BG}	TempCo		60		ppm/°C	
	Output Impedance		100		kΩ	
Reference Buffer						
	Gain		1/1.24		V/V	
TC_{RB}	TempCo		40		ppm/°C	
	Input Impedance		50		kΩ	
Analog Input						
BW	Bandwidth(-1dB)		600		MHz	
V_{ID}	Differential Input Range			$\pm V_{REF}$ /1.24	V	4VPP full scale max.
V_{ICM}	Common Mode Input Range	0		AV_{DD}	V	
V_{REFExt}	External Reference Voltage	0.5		2.5	V	
R_{IN}	Input Resistance		*			*See *Figure 5.*
C_{IN}	Input Capacitance			10	pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
AC Parameters						
SNR	Signal-to-Noise Ratio (F_{IN}=1.0MHz)	64 63	67 66		dB dB	XRD6622AIQ44 XRD6622AIQ
SNR	Signal-to-Noise Ratio (F_{IN}=3.6MHz)	62	66		dB	Both packages
SNR	Signal-to-Noise Ratio (F_{IN} = 10MHz)		62		dB	
THD	Total Harmonic Distortion (F_{IN}=1.0MHz)	70			dB	
THD	Total Harmonic Distortion (F_{IN}=3.6MHz)	60			dB	
SINAD	SNR + Distortion (F_{IN} = 1.0 MHz)	63 62	66 65		dB dB	XRD6622AIQ44 XRD6622AIQ
SINAD	SNR + Distortion (F_{IN} = 3.6 MHz)	60	64		dB	Both packages
SINAD	SNR + Distortion (F_{IN} = 10 MHz)		60		dB	
ENOB	Effective Bits (F_{IN}=1.0MHz)		10.7		Bits	
ENOB	Effective Bits (F_{IN}=3.6MHz)		10.7		Bits	
ENOB	Effective Bits (FIN = 10MHZ)		9.7		Bits	
IMD	Intermodulation Distortion	–64	–67		dBc	
SFDR	Spurious–Free Dynamic Range	75	80		dBc	F_{IN} = 1.0MHz
DG	Differential Gain		0.5		%	
DP	Differential Phase		0.1		°	
FPBW	Full Power Bandwidth		70		MHz	
t_{AP}	Aperture Delay Time		3		ns	
Δta	Aperture Jitter		7		ps–rms	
Digital Inputs						
V_{IH}	Digital Input High Voltage	AV_{DD}-1			V	
V_{IL}	Digital Input Low Voltage			1	V	
I_{IN}	DC Leakage Currents		70		µA	
	Input Capacitance		10		pF	
Digital Outputs						
V_{OH}	Output High Voltage	DV_{DD}-0.5			V	C_L = 75pf, R_L = 1mΩ
V_{OL}	Output Low Voltage			0.4	V	C_L = 75pF, R_L = 1mΩ
C_L	Max Capacitive Load		75		pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{OZ}	High-Z Leakage	-10		10	µA	
t_{DL}	Data Valid Delay		18		ns	
t_{DEN}	Data Enable Delay		10		ns	
t_{DHZ}	Data High-Z Delay		8		ns	
	Pipeline Delay (Latency)		6		cycles	Relationship between CLK and data output
Power Supplies						
PDI_{DD}	Power Down (I_{DD})		500		µA	
AV_{DD}	Operating Voltage		5		V	
DV_{DD}	Digital Supply Voltage		5		V	
OV_{DD}	Digital Output Voltage			DV_{DD}		
I_{VDD}	Supply Current		72	75	mA	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7.0V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5V
V_{IN} ..... V_{DD} +0.5 to GND –0.5V
All Inputs ..... V_{DD} +0.5 to GND –0.5V
All Outputs ..... V_{DD} +0.5 to GND –0.5V
Storage Temperature ..... –65 to +150°C

Package Power Dissipation Rating to 75°C
32-pinTQFP 1000mW
Derates above 75°C ..... 18mW/°C
Lead Temperature (Soldering 10 seconds) .. +300°C
44-pin PQFP ..... 110°mW
Derates above 75° C ..... 15mW/°C
ESD 2KV

Notes:

1 *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

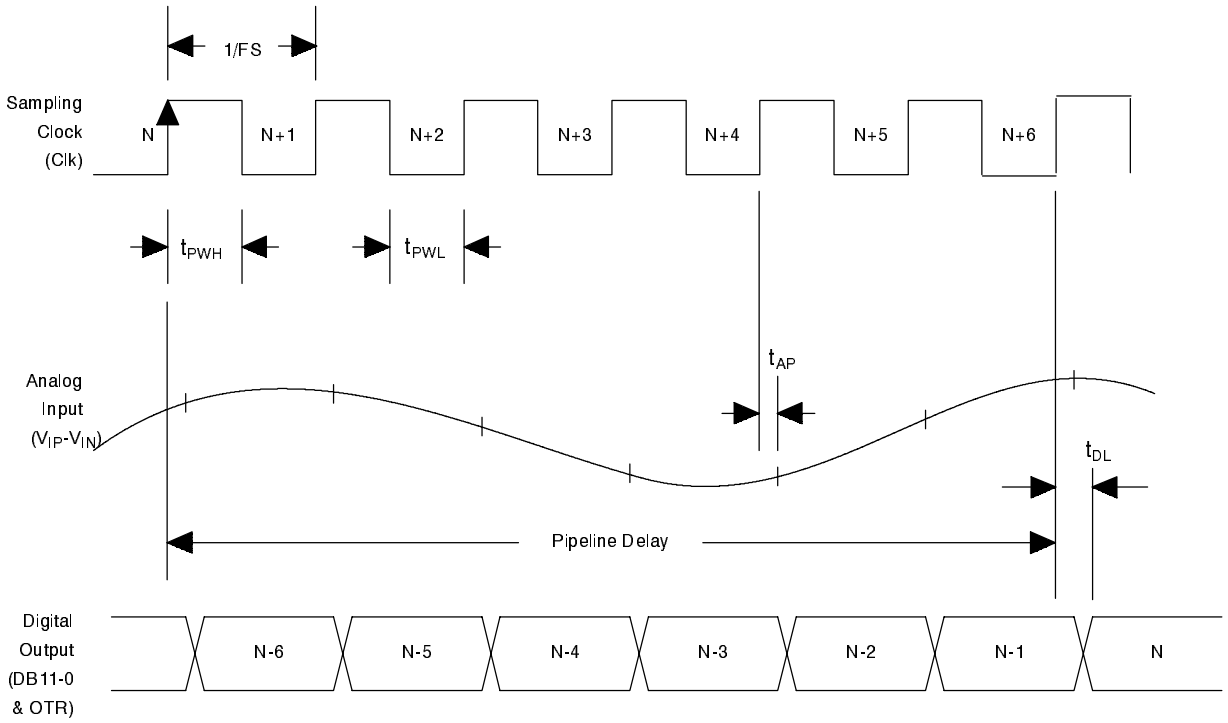


Figure 2. Timing Diagram

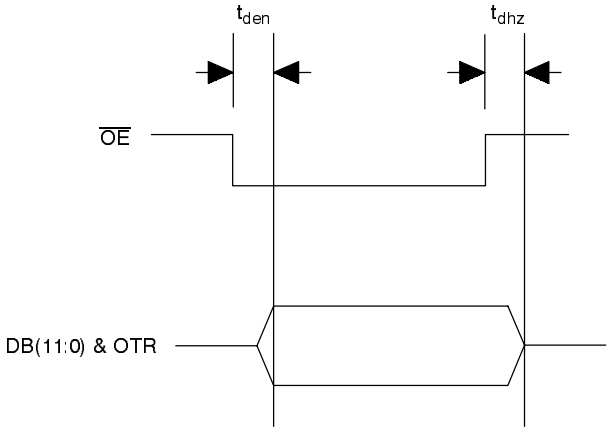
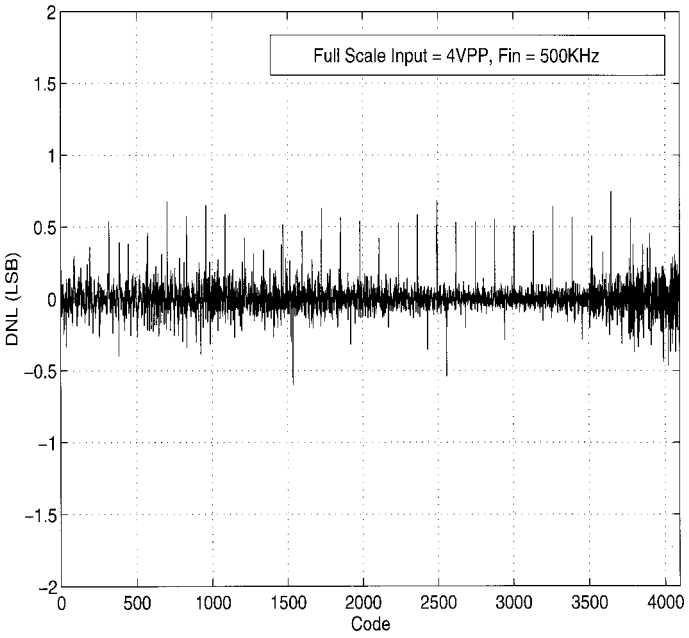
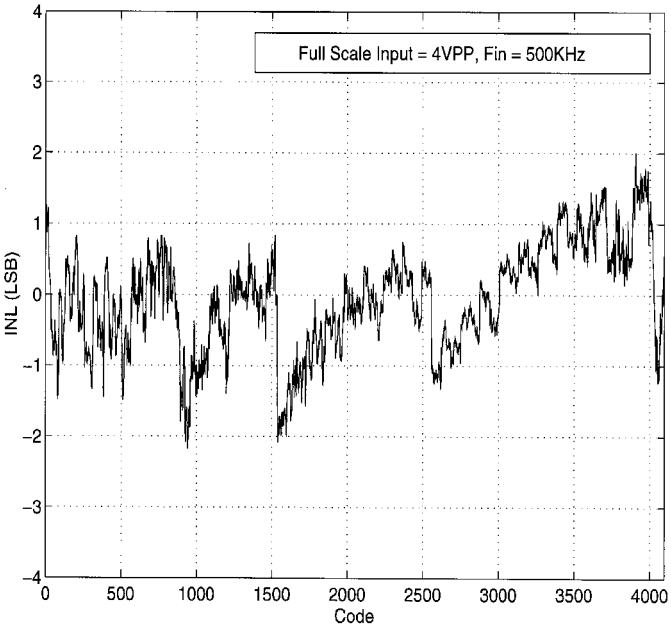


Figure 3. Data Delay and Data Enable Timing

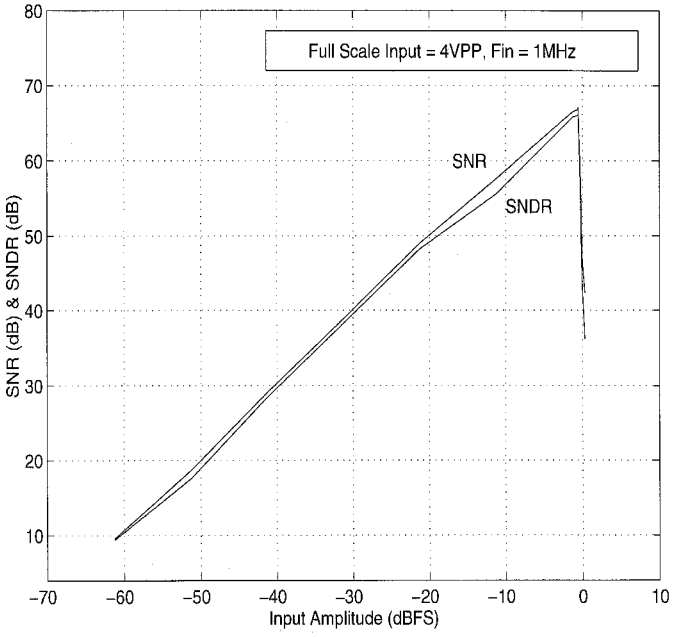
TYPICAL CHARACTERISTICS



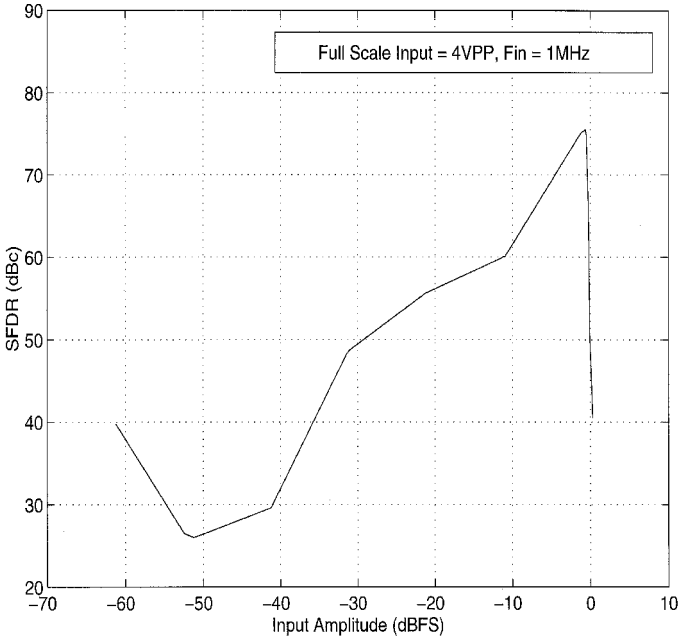
Graph 1. DNL vs. Code



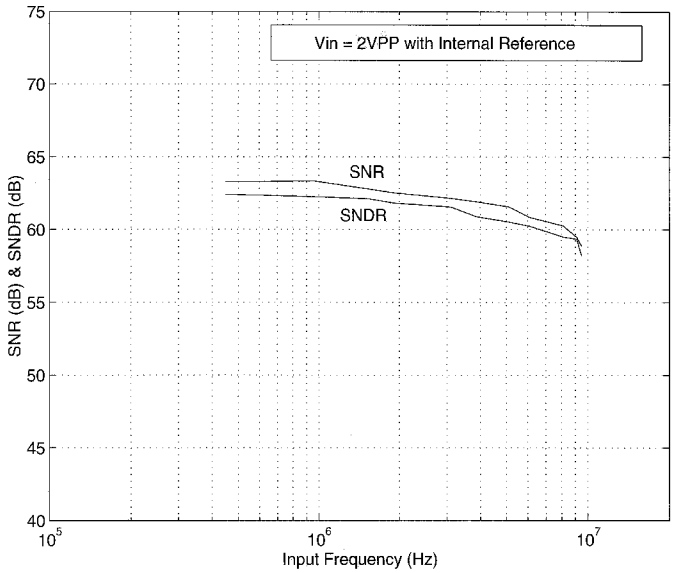
Graph 2. Best Fit INL vs. Code



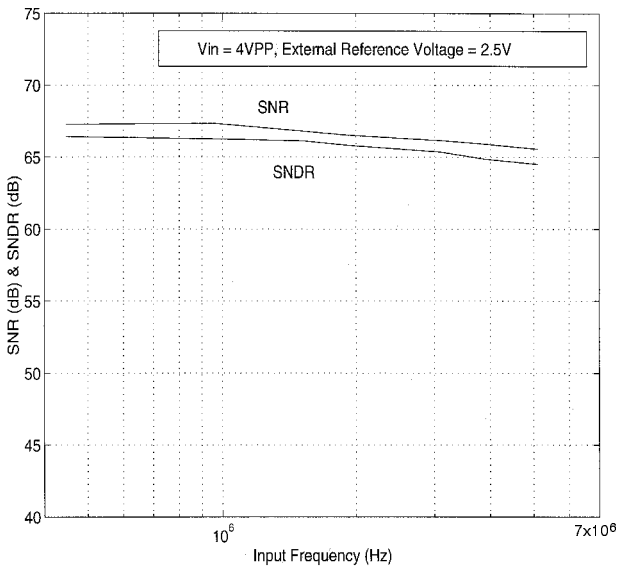
Graph 3. SNR and SNDR vs. Input Amplitude



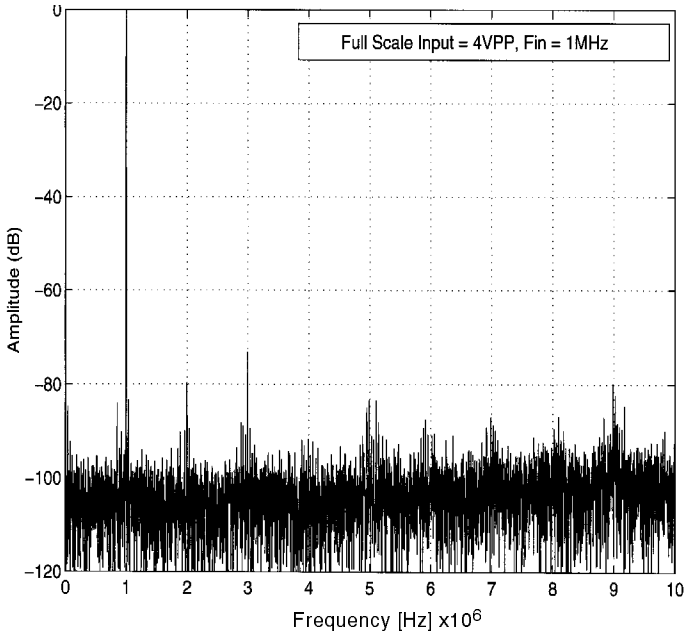
Graph 4. SFDR vs. Input Amplitude



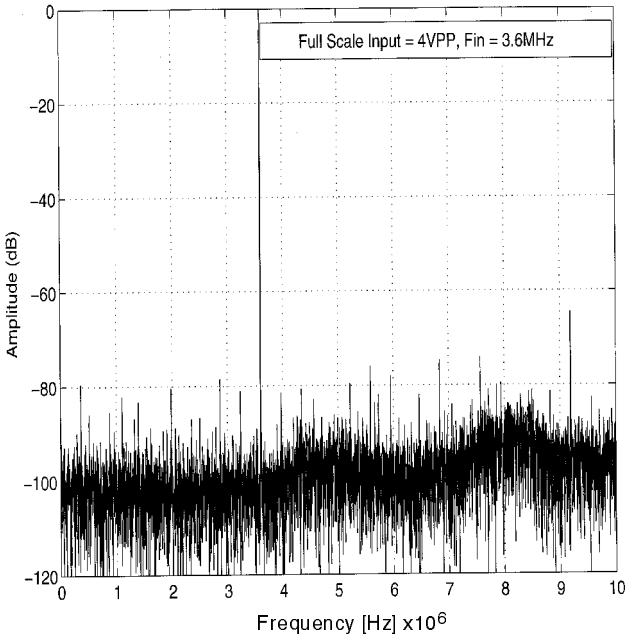
Graph 5. SNR and SNDR vs. F_{IN}, Internal Reference



Graph 6. SNR and SNDR vs. F_{IN}, External Reference



Graph 7. FFT, 20 MSPS F_{IN} = 1MHz



Graph 8. FFT, 20 MSPS F_{IN} = 3.6MHz

THEORY OF OPERATION

Analog Input (V_{IP} , V_{IN})

Internally, the XRD6622 is a fully differential part. However, the ADC can be easily configured to use single-ended input instead. Due to differential architecture of the ADC, using input differential signals will lead to better common-mode distortion and noise performance. The input has a wide common-mode compliance range and a very good common-mode rejection. *Figure 4* shows the simplified schematic of the input Track/Hold. The operation of switches is controlled by internally generated non-overlapping signals Φ1 and Φ2.

In track mode, capacitors CT1 and CT2 configured in series charge up to the input differential voltage, while the bottom plates of CT1 and CT2 are held at an internally generated bias voltage VB. During the hold time the charge stored in CT1 and CT2 will be transferred to hold capacitors CH1 and CH2. Consequently the output voltage represents the input voltage at the sampling moment. The equivalent circuit of the input Track/Hold stage is shown in *Figure 5*. Note that switch S0 does not exist physically. It is added to model virtual ground at the input of the Track/Hold Op Amp during hold time.

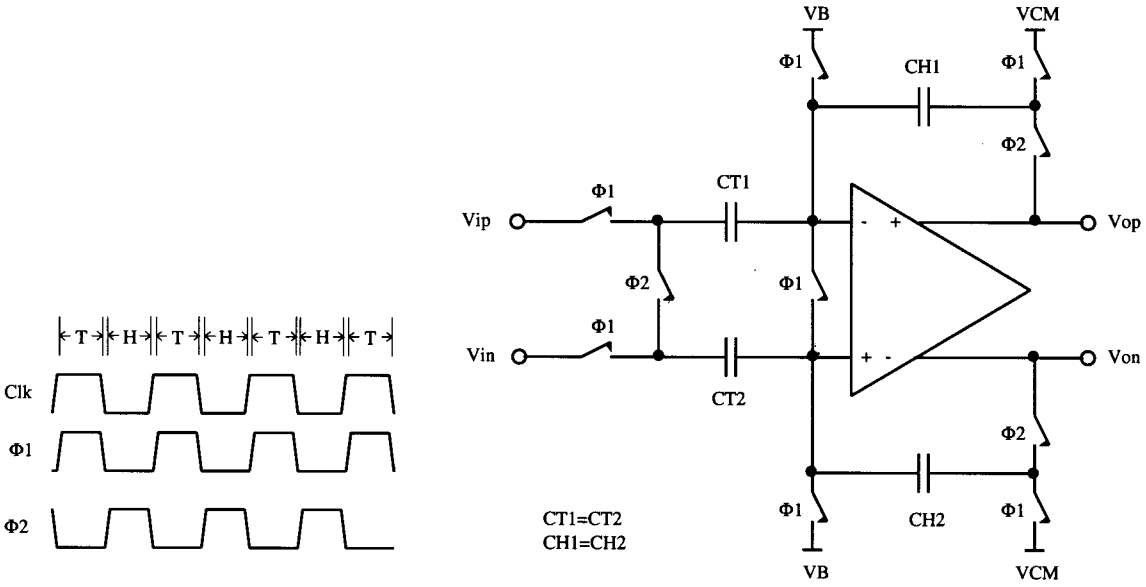


Figure 4. XRD6622 Simplified Block Diagram of Track/Hold Circuit

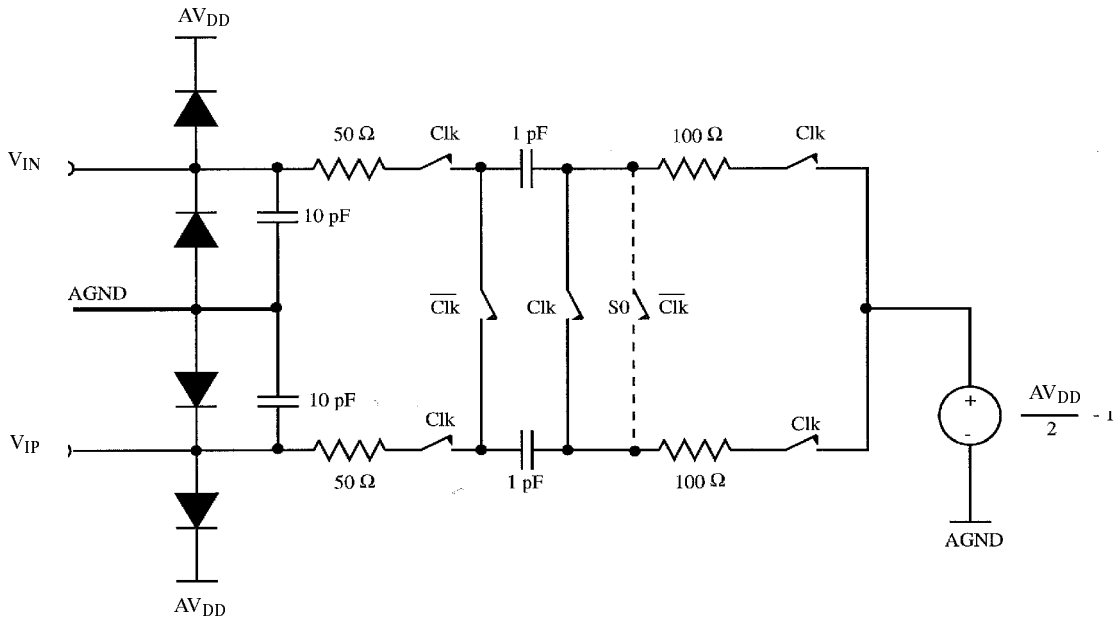


Figure 5. Simplified Input Circuit

Out of Range Indicator (OTR)

The out of range indicator is used to indicate a fault condition. This signal will go high if the input exceeds the conversion range of the ADC, i.e. the input is above $+V_{REF}/1.24$ or below $-V_{REF}/1.24$. This bit can be combined with the MSB to indicate if the input is too positive or too negative. This bit will also go high if the correction range of the digital correction logic is exceeded. This is typically caused by running the ADC with a Vref that is too small.

Output Enable ($\overline{OE}$)

This signal controls the tri-state drivers on the digital outputs DB11-DB0 and OTR. During normal operation $\overline{OE}$ should be held low so that all outputs are enabled. If $\overline{OE}$ is driven high DB11-0 and OTR go into high impedance mode. This control operates asynchronous to the clock and will only control the output drivers. The internal output registers will get updated independent of $\overline{OE}$ setting.

Power Down Control (PD's)

Depending on the package, the XRD6622 has a number of power down modes available. In the 32-pin package, the only control is $\overline{PD}$. Pulling $\overline{PD}$ signal low will disconnect the input clock, turn off all internal cells and set the output word DB11-0 and OTR to DGND. If high impendance outputs are desired in $\overline{PD}$ mode, $\overline{OE}$ should be pulled high. The turn on time from switching out of power down mode will be set by the time it takes for the internal V_{REF} buffer to charge up the external decoupling caps connected to Capp and Capn. Typically for 2.2µF decoupling caps this time will be about 30ms. In the 44-pin package, there are four more power down controls available for different internal cells. Typically these controls would be used only for debugging purposes. *Table 1* explains which cell each power down option controls.

Pin Name	Effected Cell
PD_{ADC}	The bias current to the core ADC is shut-down. The master bias generator, reference buffer and bandgap reference will still oper-ate.
PD_{RBuf}	The bias current to the reference buffer is shutdown. This allows for an external refer-ence buffer to be used.
PD_{BG}	The bias current and clock input to the chop-per stabilized bandgap reference is shut off. This reduces power supply noise from the F_{CLK}/20 chopper
PD_{ACLK}	The main input clock is shut off. The bandgap clock is unaffected.
$\overline{PD}$	PD_{BG}, PD_{ACLK} are activated and the output register clock is shut off.

Table 1. Power Down Controls

Power Supplies

Internally the XRD6622 contains several independent power supplies. One set of supplies is AV_{DD} and AGND. These supplies connect to all of the sensitive analog and digital circuitry. This circuitry includes the core of the ADC (ADC op-amps and comparators), the master bias generator, the bandgap reference, bandgap reference buffer, and master clock generator. The next supply is DV_{DD} and DGND. This supply is connected to the digital correction logic. OV_{DD} may be connected to a lower power supply (such as 3.3V or 3.0V) to simplify interfacing to lower voltage logic. DGND may also be lifted above AGND. All of the inputs to the ADC are relative to AV_{DD}. This was done to avoid generating non-50% duty cycle clocks with slow rise/fall time sampling clocks. RGND should be connected to AGND, (44 pin package only). This is the reference ground for V_{BG} and $Vref_{Ext}$.

Internally, the bulk node of all NMOS devices (i.e. the substrate) is connect to a separate supply line called SGND. This separate supply line is used to help isolate power supply coupling from AGND and DGND. In the 32-pin package, SGND is connected to AGND. DV_{DD} and DGND are connected only to the internal digital decode logic. OV_{DD} and OGND are connected only to the digital output drivers. Internally, there is also a shielding line that helps to isolate very sensitive nodes. This line is connected internally to AGND.

Figure 6 shows the power supply connection as it pertains to digital input pins.

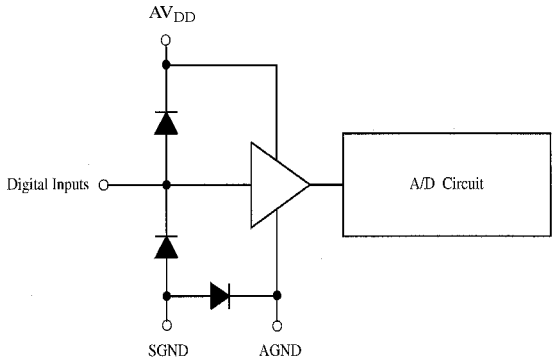


Figure 6. XRD6622 Power Supply Connection for Digital Inputs.

Logic Output Interface

The digital output drive circuitry of the XRD6622 is designed to operate from the analog and digital supplies. The OV_{DD} pin of the XRD6622 is a separate power supply dedicated to the logic output drivers. OV_{DD} is not connected internally to any of the other power supplies. *Figure 7* illustrates the power supply circuitry of the XRD6622.

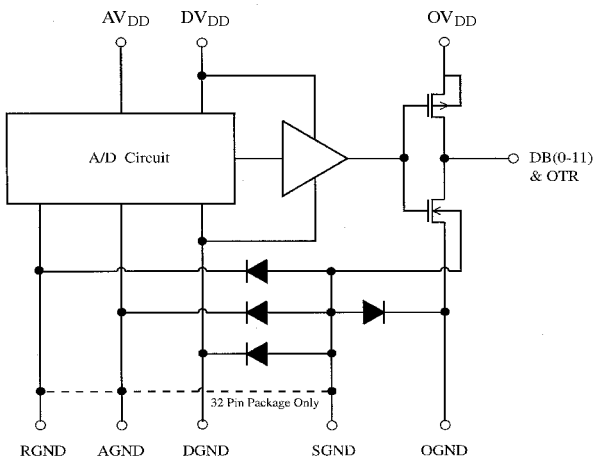


Figure 7. XRD6622 Power Supply Circuit Provides a Separate Supply Line for Digital Output Pins

OV_{DD} and OGND connected directly to the digital output pins. OGND is not common to the XRD6622 substrate. The XRD6622 substrate is common to the packages' SGND pins for the 44-pin QFP package and AGND pins for the 32-pin TQFP. Best Spectral performance is obtained with OV_{DD} lowered to 3.3V.

Reference Control (V_{BG}, $Vref_{Ext}$, Capp, Capn)

The XRD6622 includes an onboard chopper stabilized bandgap reference with a nominal output voltage of Vref. The bandgap will not function when the ADC is not clocked.

A high impedance output version of internal bandgap voltage is available on pin V_{BG}. This voltage must be buffered, and should be decoupled to RGND (AGND 32 pin package), before it is used. An external override control is available. If an input below approximately AV_{DD}-1V is applied to $Vref_{Ext}$ then the external applied voltage is used for Vref. This option allows the use of an alternate bandgap reference or the use of an external op-amp to gain up or to attenuate V_{BG} to change the full scale range of the ADC. V_{REFExt} should be pulled up to AV_{DD} to select the internal bandgap reference voltage.

V_{REF} (either externally applied or from the bandgap reference) is buffered by the reference buffer. This buffer has a nominal gain of 1/1.24 resulting in an input to the ADC of 1V when using the internal reference. A 1V input corresponds to a 2VPP full scale voltage on the ADC. The pins Capp and Capn connect to the output of the reference buffer and must be bypassed with capacitors. A parallel combination of a 2.2µF tantalum and a 0.1µF low inductance ceramic capacitor is recommended.

In the 44 pin package it is possible to shut off the reference buffer and connect an external buffer. The reference buffer is shut off by pulling PD_{RBUF} high. In this mode of operation, the external buffer must generate a differential reference voltage centered near $AV_{DD}/2$.

Digital Testing

As with any ADC that includes error correction, it is possible that a fault in the digital correction logic would not be detected with standard all codes testing. The XRD6622 includes a special mode that will guarantee 100% stuck-at-fault coverage. To initiate the test, V_{BG} should be pulled to AV_{DD} and a positive full scale input should be applied. The output code should be verified to be DB11=1, DB10-0=0. That, in combination with the standard all codes test, will ensure 100% stuck-at-fault coverage. This test is performed on all parts shipped.

Default Modes

Default settings are provided for all options through the use of internal 100kΩ equivalent pull-up or pull-down resistors. *Table 2* shows the default settings.

Pin Name	Default Setting
PD_{ADC}	SGND - Core of ADC is on
PD_{Rbuf}	SGND - Reference buffer is on
PD_{BG}	SGND - Bandgap reference is on
PD_{ACLK}	SGND - Two phase clock generator is running
$\overline{OE}$	SGND - Outputs are enabled
$\overline{PD}$	AV_{DD} - part is powered on

Table 2. Default Digital Control Settings

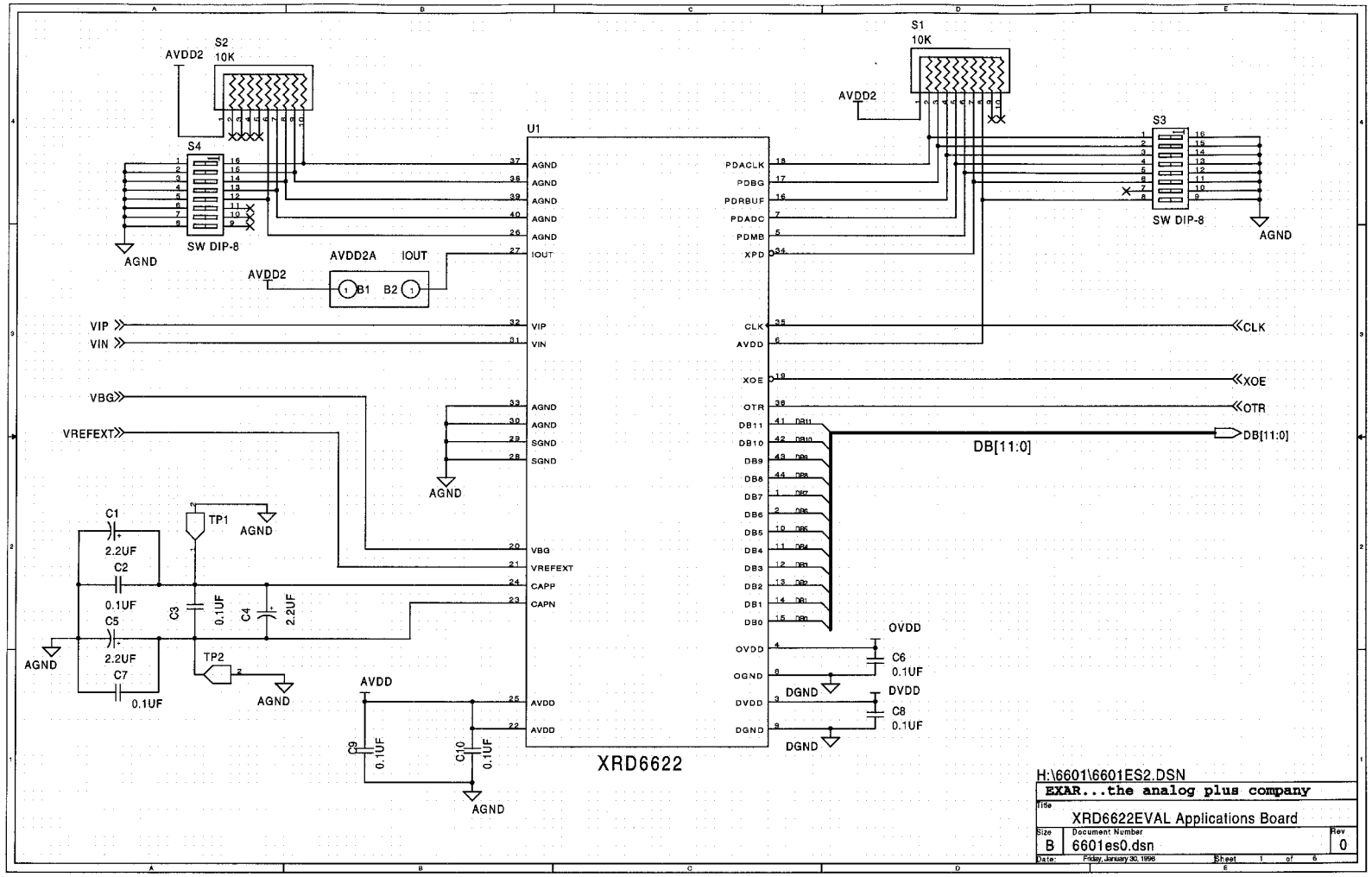


Figure 8. Application Schematic Sheet 1 of 6

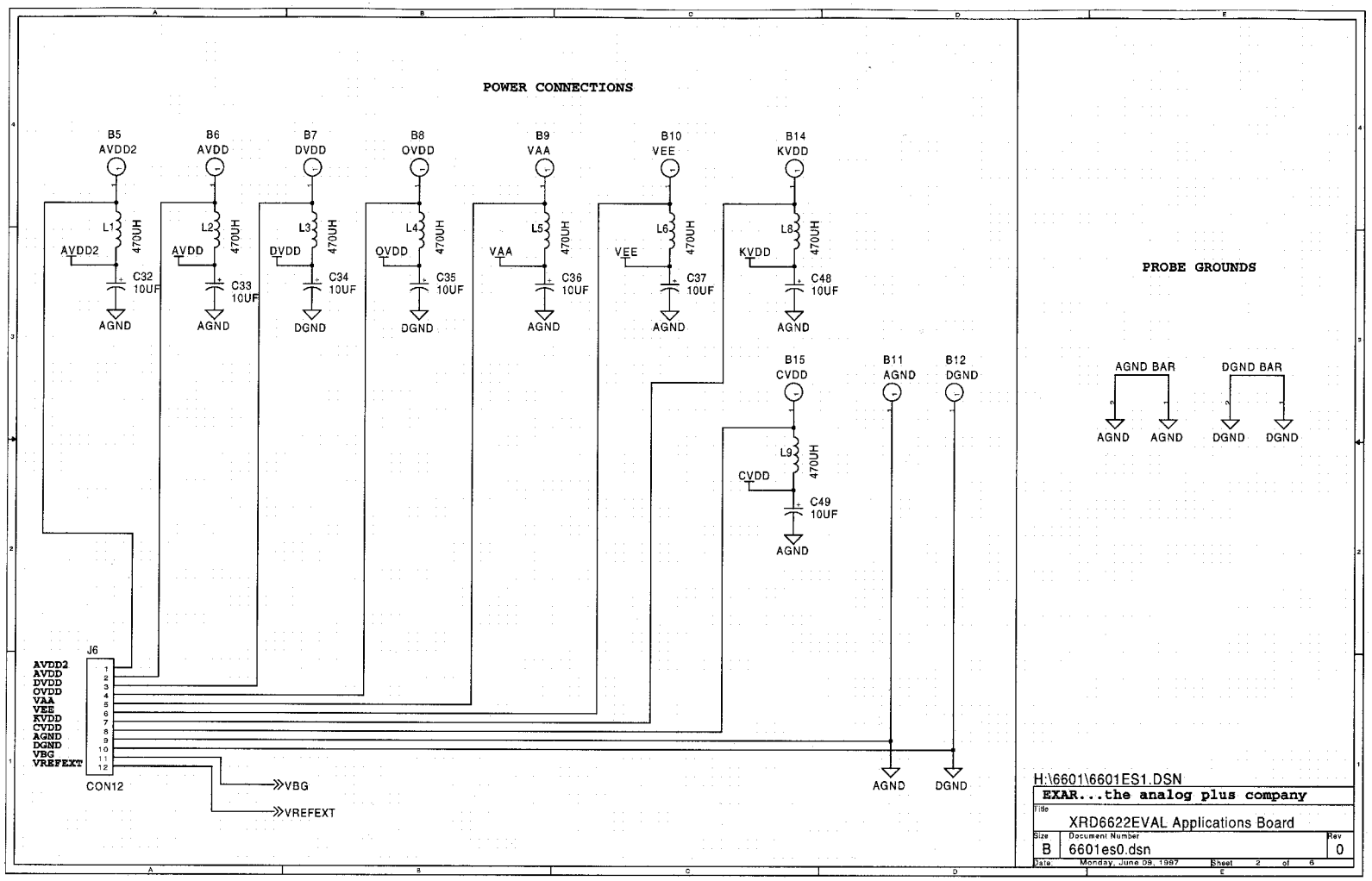


Figure 9. Application Schematic Sheet 2 of 6

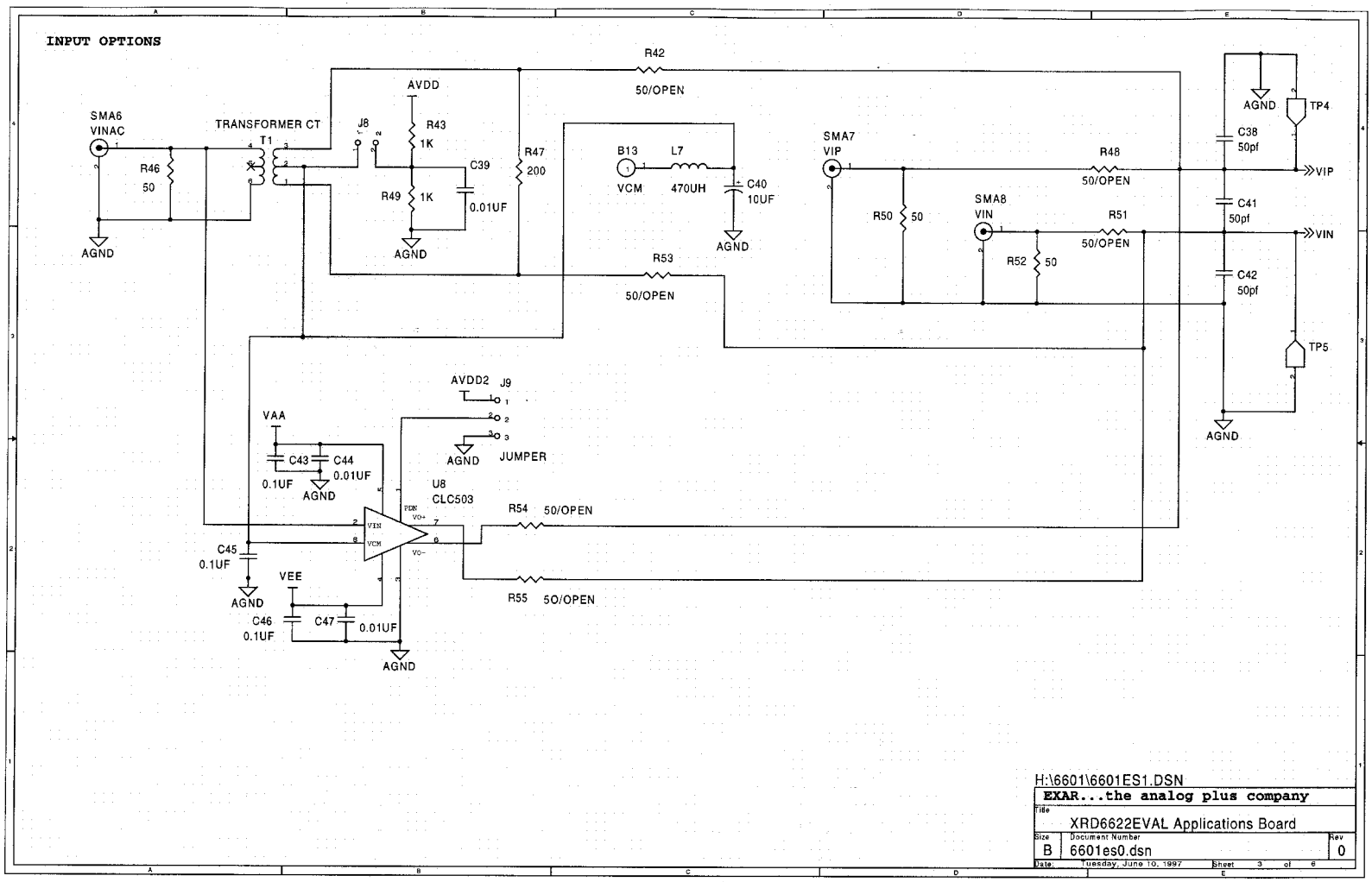


Figure 10. Application Schematic Sheet 3 of 6

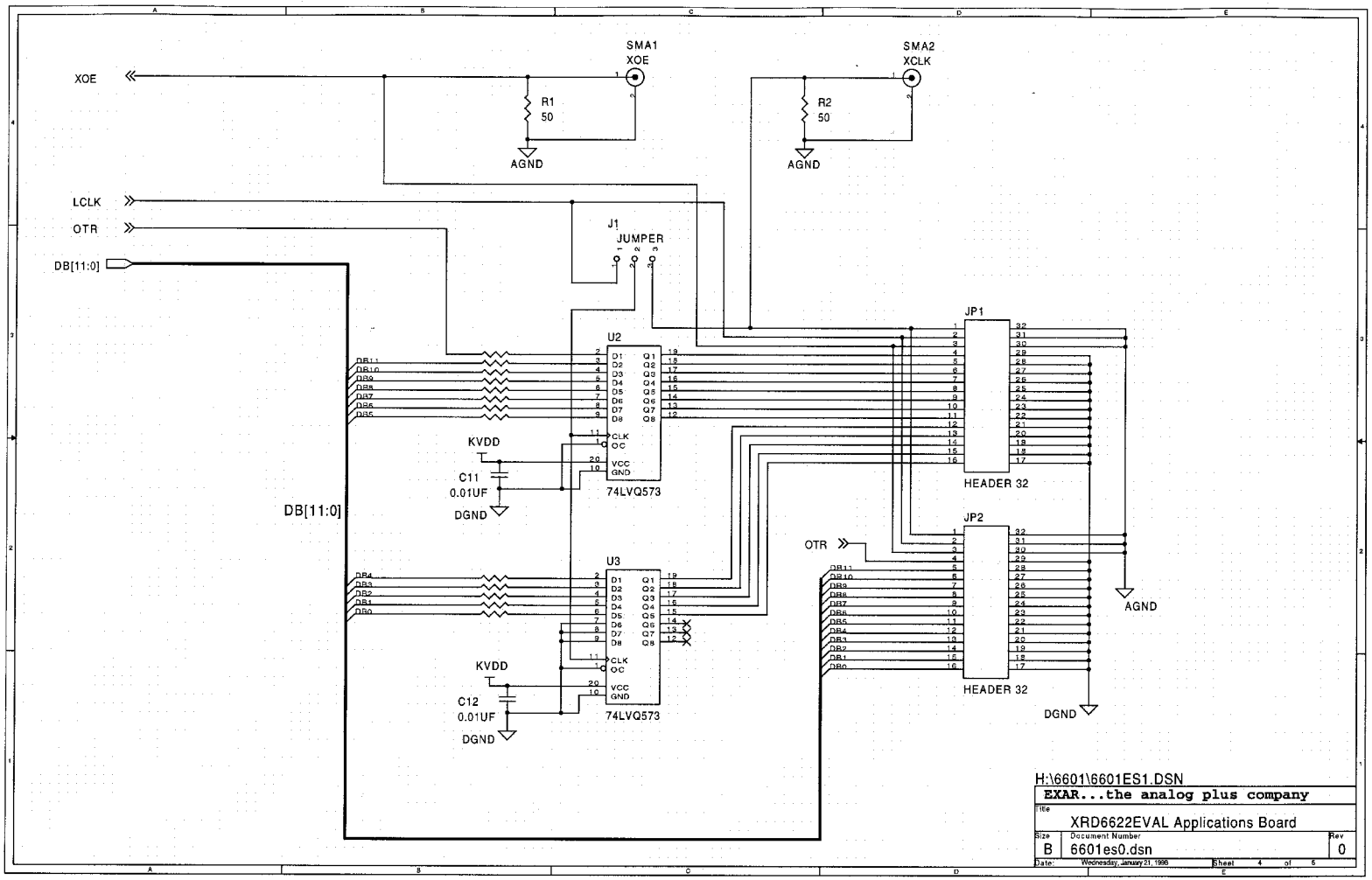


Figure 11. Application Schematic Sheet 4 of 6

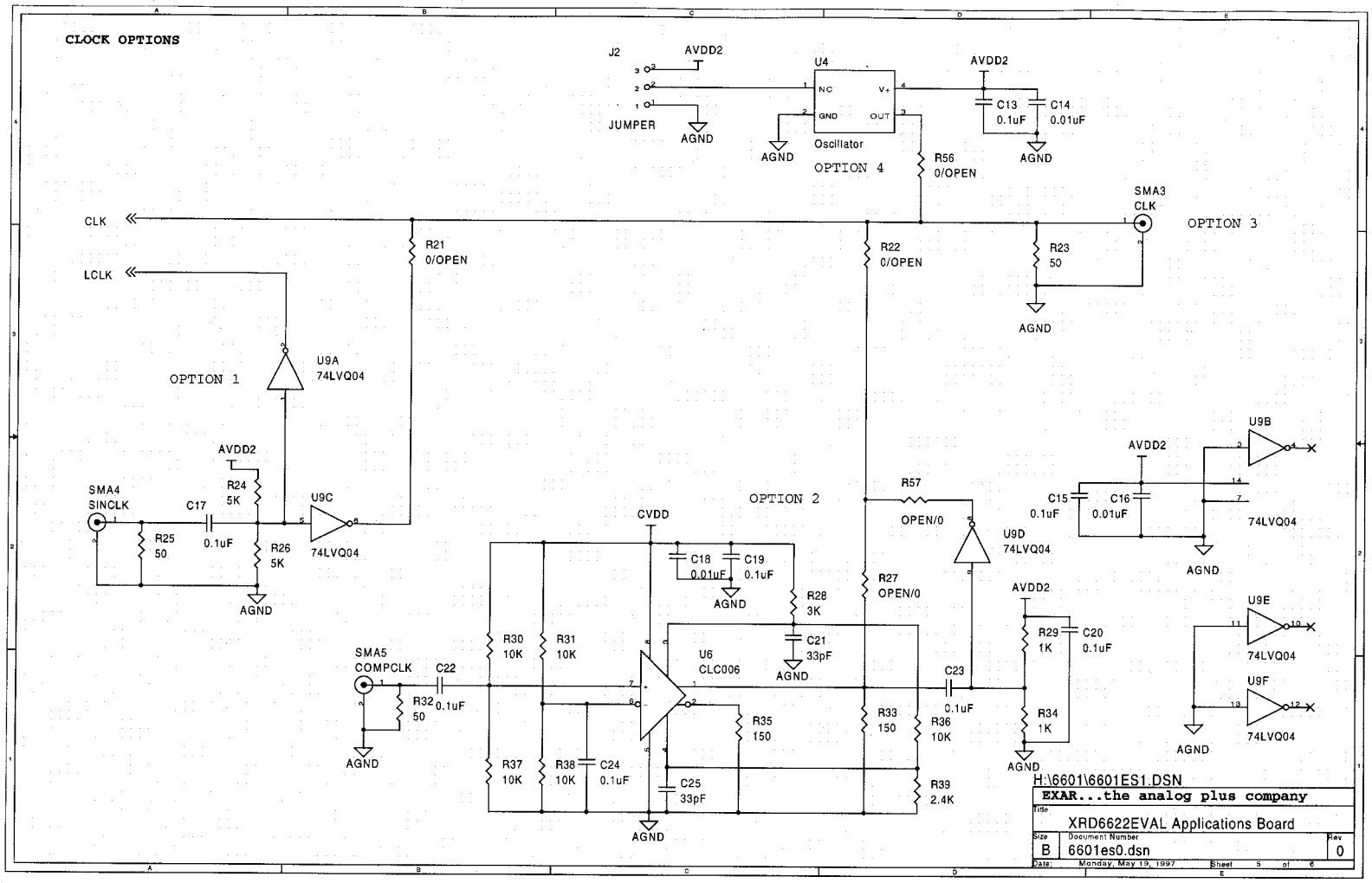


Figure 12. Application Schematic Sheet 5 of 6

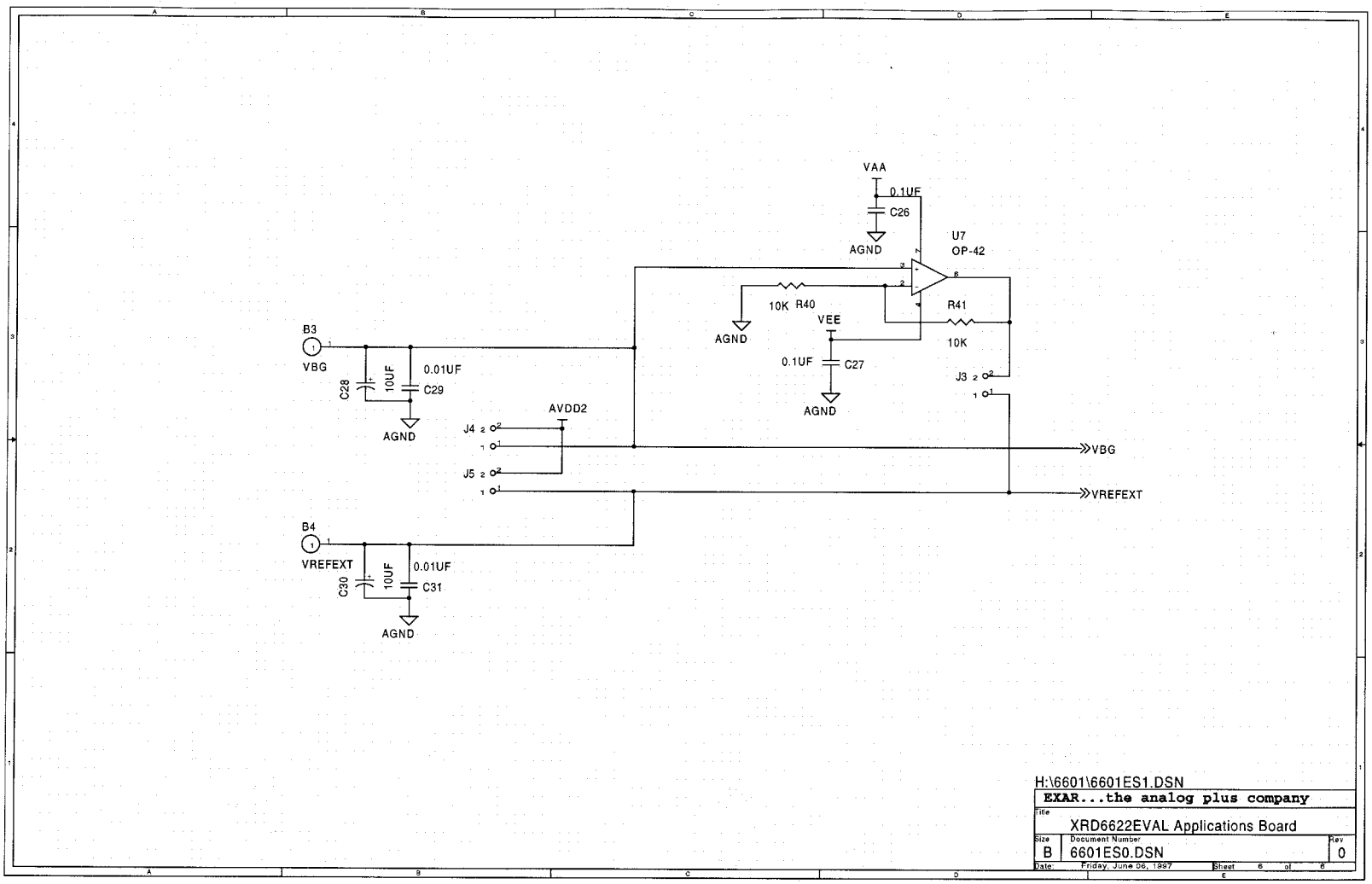


Figure 13. Application Schematic Sheet 6 of 6

Notes