

DESCRIPTION

The HYM5V32414A is a 4M x 32-bit EDO mode CMOS DRAM Module consisting of eight HY51V17404A in 24/26 pin TSOPII on a 72 pin Zig Zag Dual tabs glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM.

The HYM5V32414ATNG/ASLTNG are Gold plated socket type Small Outline Dual In-Line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- Low power dissipation
 - Max. self-refresh 13.2mW (SL-part)
 - Max. battery back-up 14.4mW (SL-part)
 - Max. CMOS standby 5.76mW (SL-part)
 - 14.4mW
 - Max. TTL standby 88.0mW
 - Max. operating

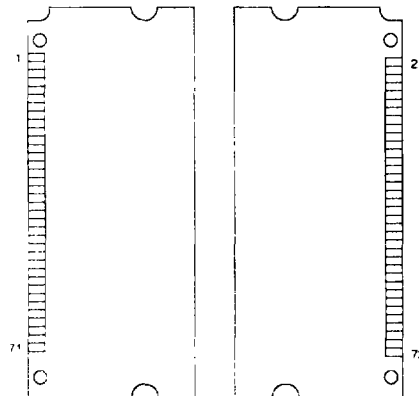
Speed	Power
60	3.46W
70	2.88W
80	2.59W

- Single power supply of 3.3V± 10%
- TTL compatible inputs and outputs
- Fast access time

Speed	tRAC	tCAC	tHPC
60	60ns	15ns	25ns
70	70ns	18ns	30ns
80	80ns	20ns	35ns

- EDO mode operation
- CAS-before-RAS, RAS-only, Hidden refresh and Self-Refresh
- 2048 refresh cycles / 256ms (SL-part)
- 2048 refresh cycles / 32ms

PIN CONNECTION



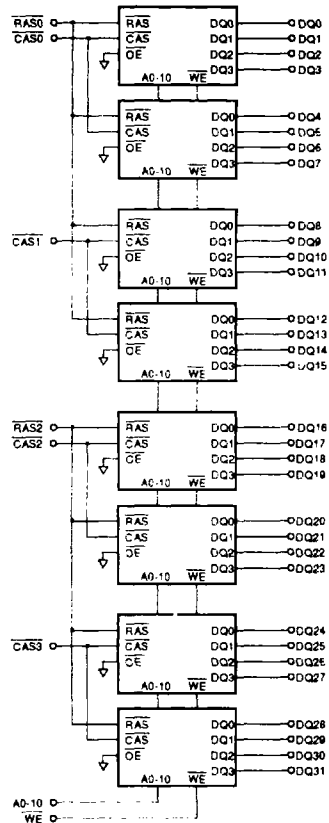
PIN DESCRIPTION

RAS0, RAS2	Row Address Strobe
CAS0-CAS3	Column Address Strobe
WE	Write Enable
A0-A10	Address Input
DQ0-DQ31	Data Input/Output
PD1-PD7	Presence Detect
Vcc	Power (+ 3.3V)
Vss	Ground

PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ16
2	DQ0	38	DQ17
3	DQ1	39	Vss
4	DQ2	40	CAS0
5	DQ3	41	CAS2
6	DQ4	42	CAS3
7	DQ5	43	CAS1
8	DQ6	44	RAS0
9	DQ7	45	NC
10	Vcc	46	NC
11	PD1	47	WE
12	A0	48	NC
13	A1	49	DQ18
14	A2	50	DQ19
15	A3	51	DQ20
16	A4	52	DQ21
17	A5	53	DQ22
18	A6	54	DQ23
19	A10	55	NC
20	NC	56	DQ24
21	DQ8	57	DQ25
22	DQ9	58	DQ26
23	DQ10	59	DQ28
24	DQ11	60	DQ27
25	DQ12	61	Vcc
26	DQ13	62	DQ29
27	DQ14	63	DQ30
28	A7	64	DQ31
29	NC	65	NC
30	Vcc	66	PD2
31	A8	67	PD3
32	A9	68	PD4
33	NC	69	PD5
34	RAS2	70	PD6
35	DQ15	71	PD7
36	NC	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PIN

PIN	-60	-70	-80
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	Vss	Vss	Vss
PD4	NC	NC	NC
PD5	NC	Vss	NC
PD6	NC	NC	Vss

PD7	REFRESH MODE
NC	Normal
VSS	Self Refresh

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 125	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-0.5 to 4.6	V
VCC	Voltage on VCC Relative to VSS	-0.5 to 4.6	V
IOS	Short Circuit Output Current	20	mA
Pd	Power Dissipation	4.4	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	3.0	3.3	3.6	V
VIH	Input High Voltage	2.0	-	VCC+ 0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC + 1.0, All other pins not under test= VSS		-80	80	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	tRC= tRC (min.)	60 70 80	-	960 800 720	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	16	mA	
ICC3	VCC Supply Current, RAS-only refresh	tRC= tRC (min.)	60 70 80	-	960 800 720	mA	1,3
ICC4	VCC Supply Current, EDO mode	tHPC= tHPC (min.)	60 70 80	-	800 720 640	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	SL-part	-	8 3.2	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	60 70 80	-	960 800 720	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (SL-part only)	tRC= 125μs, CAS= CBR cycling or 0.2V WE= VCC-0.2V A0-A10= VCC-0.2V or 0.2V DQ0-DQ31= VCC-0.2V, 0.2V, or open	tRAS ≤ 300ns tRAS ≤ 1μs	-	2.8 4.8	mA	1,4,5
ICC8	VCC Supply Current Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V OE & WE & A0-A10= VCC-0.2V or 0.2V DQ0-DQ31= VCC - 0.2V, 0.2V or open			2.4	mA	5
VOL	Output Low Voltage	IOL= 2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -2mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1, ICC3, ICC4 and ICC6 depend on output loading. Specified values are obtained with the output open.
3. ICC is specified as average current. For ICC1, ICC3 and ICC6, address can be changed maximum two times while RAS= VIL. For ICC4, address can be changed maximum once while CAS= VIH.
4. Only tRAS(max.)= 1μs is applied to refresh of battery backup but tRAS(max.)= 10 μs is applied to normal functional operation.
5. ICC5(max.)= 3.2mA, ICC7 and ICC8 are applied to SL-part only (HYM5V32414ASLTNG).

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 3.3V± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM5V32414A N-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tRHCP	RAS Hold Time from CAS Precharge	35	-	40	-	45	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	3	-	3	-	3	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	3	15	3	18	3	20	ns	5
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (EDO Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	RAS Hold Time	15	-	18	-	20	-	ns	
16	tCSH	CAS Hold Time	45	-	50	-	55	-	ns	
17	tCAS	CAS Pulse Width	11	10K	14	10K	17	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	17	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	12	-	14	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	12	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	50	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	50	-	55	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	twCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM5V32414A N-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	40	-	45	-	59	-	ns	8
42	tRWD	RAS to WE Delay Time	80	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	50	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	n	
47	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	8
48	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
49	tWRH	WE to RAS Hold time (CBR Cycle)	10	-	10	-	10	-	ns	
50	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	μs	
51	tRPS	RAS Precharge Time (Self Refresh Cycle)	90	-	110	-	130	-	ns	
52	tCHS	CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
53	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
54	tREZ	Output Buffer Turn-off Delay (RAS)	3	15	3	18	3	20	ns	5,15
55	tWEZ	Output Buffer Turn-off Delay (WE)	3	15	3	18	3	20	ns	5
56	tWPE	WE Pulse Width for Output Disable	5	-	8	-	10	-	ns	
57	tWED	WE to Data Delay Time	15	-	18	-	20	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 \overline{RAS} cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} -only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{RAS} = V_{SS}$ during power-up, the HYM5V32414A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that \overline{RAS} and \overline{CAS} track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. Refer to the HY51V17404A data sheet for detailed information.
4. Measured at $V_{OH} = 2.4V$ and $V_{OL} = 0.4V$ with a load equivalent to 1 TTL loads and 100pF. ($V_{OH} = 2.0V$, $V_{OL} = 0.8V$)
5. $t_{CEZ}(\max.)$, $t_{OEZ}(\max.)$, $t_{REZ}(\max.)$ and $t_{WEZ}(\max.)$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in late write or read-modify-write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min.)$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD}(\max.)$ limit insures that $t_{TRAC}(\max.)$ can be met. $t_{RCD}(\max.)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max.)$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\max.)$ limit insures that $t_{TRAC}(\max.)$ can be met. $t_{RAD}(\max.)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max.)$ limit, then access time is controlled by t_{AA} .
11. Measured with the specified current load and 100pF.
12. A burst of 2048 \overline{CAS} -before- \overline{RAS} refresh cycles must be executed within 32ms after exiting self refresh (for SL-part).
13. If $t_{CWD} \geq t_{WCS}(\min.)$, $t_{RWD} \geq t_{RWD}(\min.)$, $t_{AWD} \geq t_{AWD}(\min.)$ and $t_{CPWD} \geq t_{CPWD}(\min.)$, the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until \overline{CAS} goes back to V_{IH}) is indeterminated.
14. In \overline{CAS} before \overline{RAS} self refresh mode.
 In case of using distributed \overline{CAS} before \overline{RAS} refresh, refresh 2048 times during a 256ms after reset
 In case of using burst \overline{CAS} before \overline{RAS} refresh, refresh 2048 times during a 32ms after reset
 In case of using \overline{RAS} only refresh, refresh against all refresh address during 32ms after reset
15. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes to high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.

CAPACITANCE

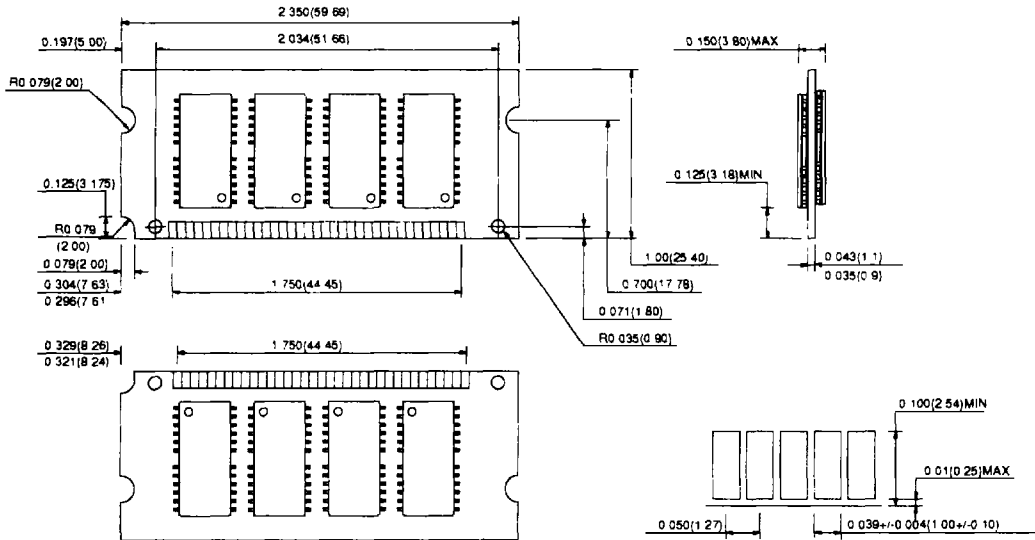
($T_A = 25^\circ C$, $V_{CC} = 3.3V \pm 10\%$, $V_{SS} = 0V$, $f = 1MHz$, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	64	pF
CIN2	Input Capacitance (\overline{WE})	-	70	pF
CIN3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	40	pF
CIN4	Input Capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	-	30	pF
CDQ	Data Input/output Capacitance (DQ0-DQ31)	-	15	pF

PACKAGE INFORMATION

72 pin Small Outline Dual In-line Memory Module (NG ; Gold plated)

UNIT INCH(mm)
TOLERANCE +/-0.005(0.13)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V32414 ATNG	60/70/80		SO-DIMM	Gold
HYM5V32414 ASLTNG	60/70/80	SL-part	SO-DIMM	Gold