silicon systems®
A TDK Group Company

SSI 34P3401
Read Channel w/Adaptive Threshold Qualifier
Target Specification

January 1996

DESCRIPTION

The SSI 34P3401 device is a high performance BiCMOS single chip read channel IC that contains all the functions necessary to implement a complete zoned recording disk drive system. Functional blocks include a pulse detector with adaptive threshold qualifier, programmable filter, 2-burst servo capture, time base generator, and data synchronizer. Clock rates up to 53 MHz can be programmed by digital commands without external component switching.

The SSI 34P3401 allows complete flexibility in read channel configuration. Essentially all critical parameters can be programmed by a microprocessor via a bi-directional serial port and a bank of internal registers. Thus, a low component count and low cost zoned recording system can be implemented.

The SSI 34P3401 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

GENERAL

- **53 Mbit/s raw data rate**
- **Bi-directional serial port for access to internal registers**
- **Complete zoned recording application support**
- **Low power operation (TBD mW typical @ 53 MHz and 5V)**
- **Programmable power management (Sleep mode < 1 mW)**
- **Power supply range (4.5 to 5.5V)**
- **Small footprint 64-pin TQFP package**

AGC AND PULSE DETECTOR

- **Temperature compensated, exponential control AGC**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low drift AGC hold circuitry**
- **Adaptive threshold qualifier for data extraction**
- **Traditional window qualifier for timing extraction**
- **Programmable pulse qualification threshold level**
- **CMOS $\overline{\text{RDIO}}$ signal output for servo timing support**
- **Internal LOW-Z and fast decay timing for rapid transient recovery and AGC acquisition**
- **Fast decay mode is self-timed for optimal AGC recovery**
- **0.5 ns max. pulse pairing with sine wave input**
- **Independent window voltage qualification threshold in servo & data modes**
- **Independent qualification thresholds for data and timing extraction**

SERVO CAPTURE

- **2-burst servo capture with A and B output**
- **Internal servo burst hold capacitors**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 9 to 27 MHz**
- **Programmable boost of 0 to 26 dB**
- **Programmable group delay equalization (up to 30% change in group delay)**
- **Independent cutoff frequency setting in data mode and servo mode**
- **Boost setting available in data mode and servo mode**
- **Matched normal and differentiated outputs**
- **±15% fc accuracy**
- **Less than 1% total harmonic distortion**

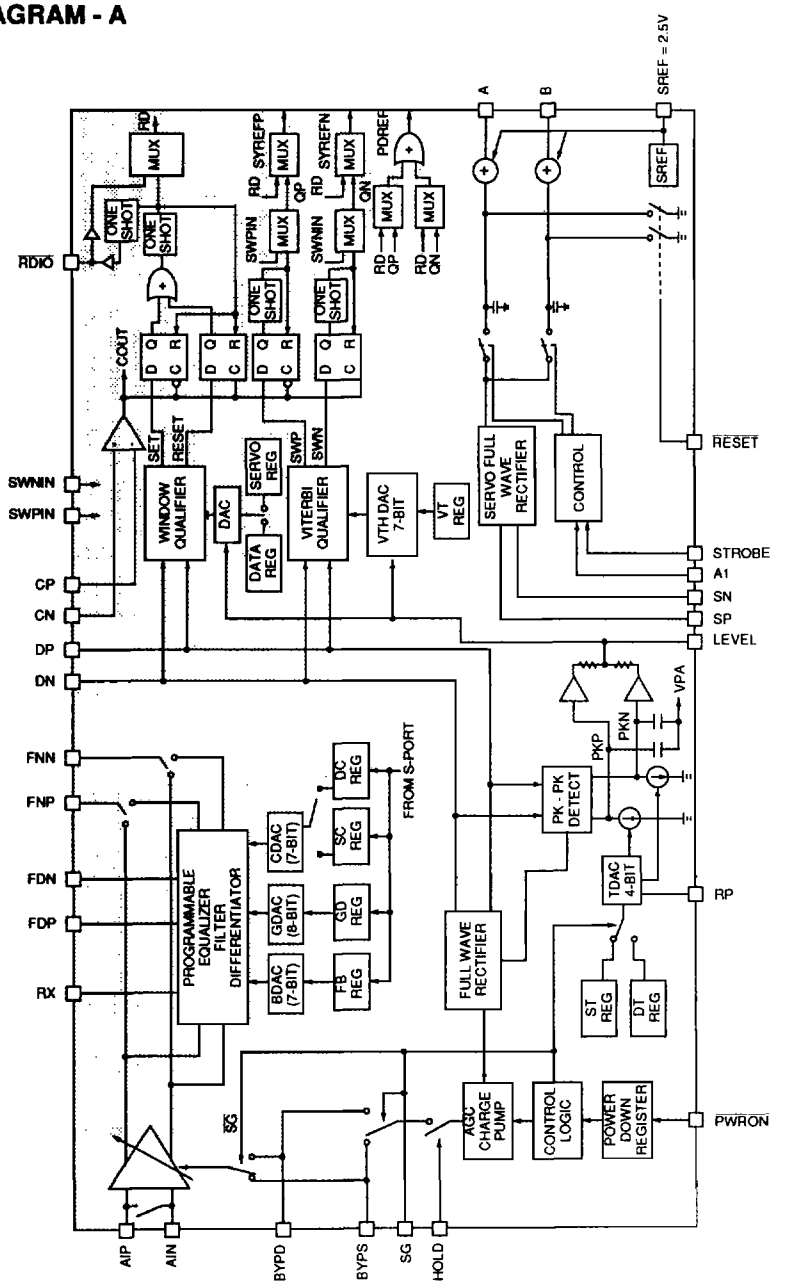
(continued)

9

The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

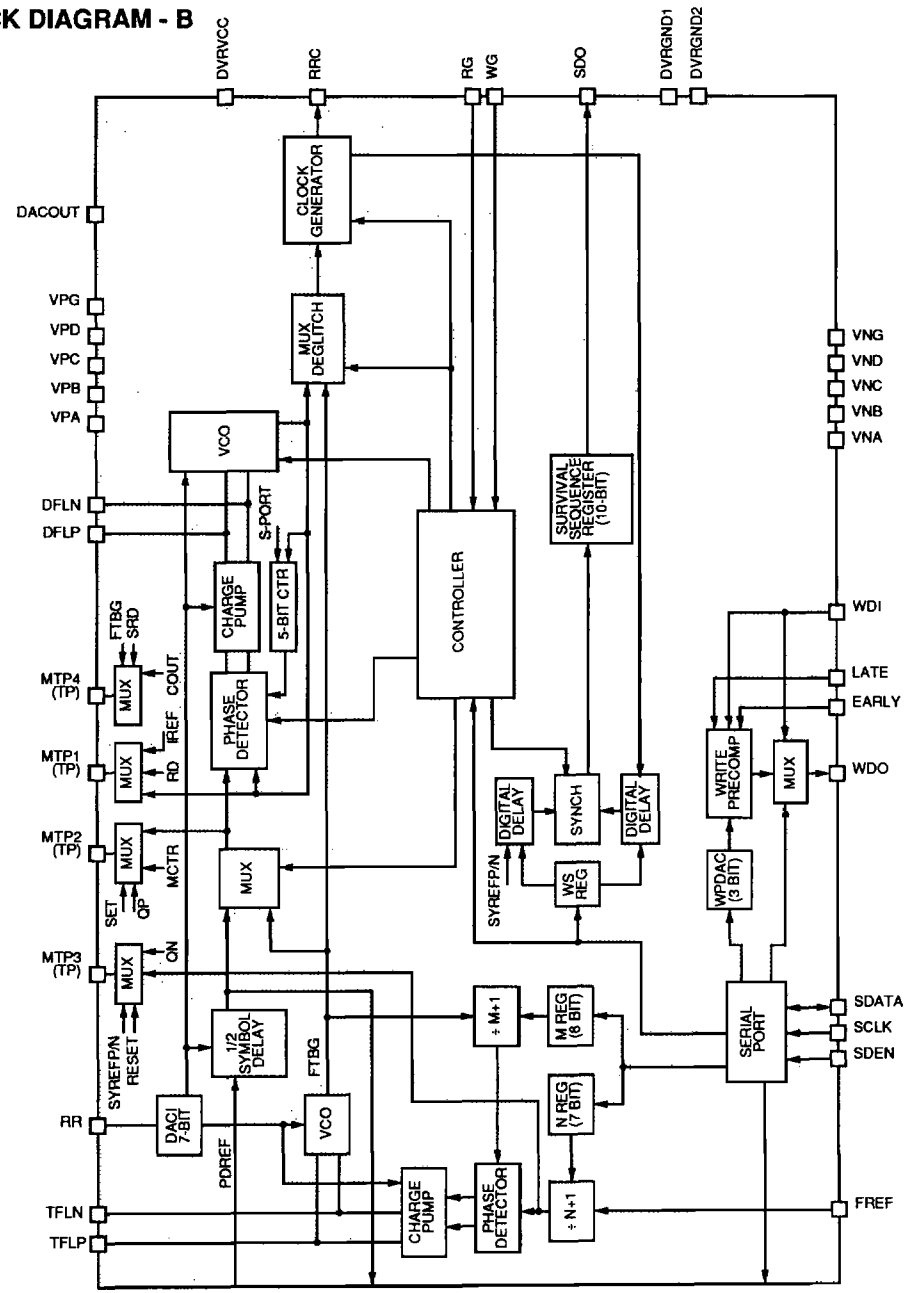
SSI 34P3401
Read Channel
w/Adaptive Threshold Qualifier

BLOCK DIAGRAM - A



The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

BLOCK DIAGRAM - B



9

The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

SSI 34P3401
Read Channel
w/Adaptive Threshold Qualifier

FEATURES (continued)

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 106 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SYNCHRONIZER

- Fully integrated data synchronizer
  - no external delay lines or active components required
  - no external active PLL components required
- Selectable PLL input from adaptive threshold qualifier or traditional window qualifier
- Selectable data synchronizer input from adaptive threshold qualifier or traditional window qualifier
- Fast PLL acquisition phase lock loop
  - zero phase restart technique
  - programmable phase detector gain gear shift
- Programmable decode window symmetry
  - window shift control ± 30% of decode window
  - includes delayed read data and VCO reference monitor points
- Programmable write precompensation
- External/Internal write precomp control
- PLL and data detection circuits capable of operating with d = 0 encoding

Target Specification: The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

No responsibility is assumed by Silicon Systems for use of this product nor for any infringements of patents and trademarks or other rights of third parties resulting from its use. No license is granted under any patents, patent rights or trademarks of Silicon Systems. Silicon Systems reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that the data sheet is current before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

©1996 Silicon Systems, Inc.