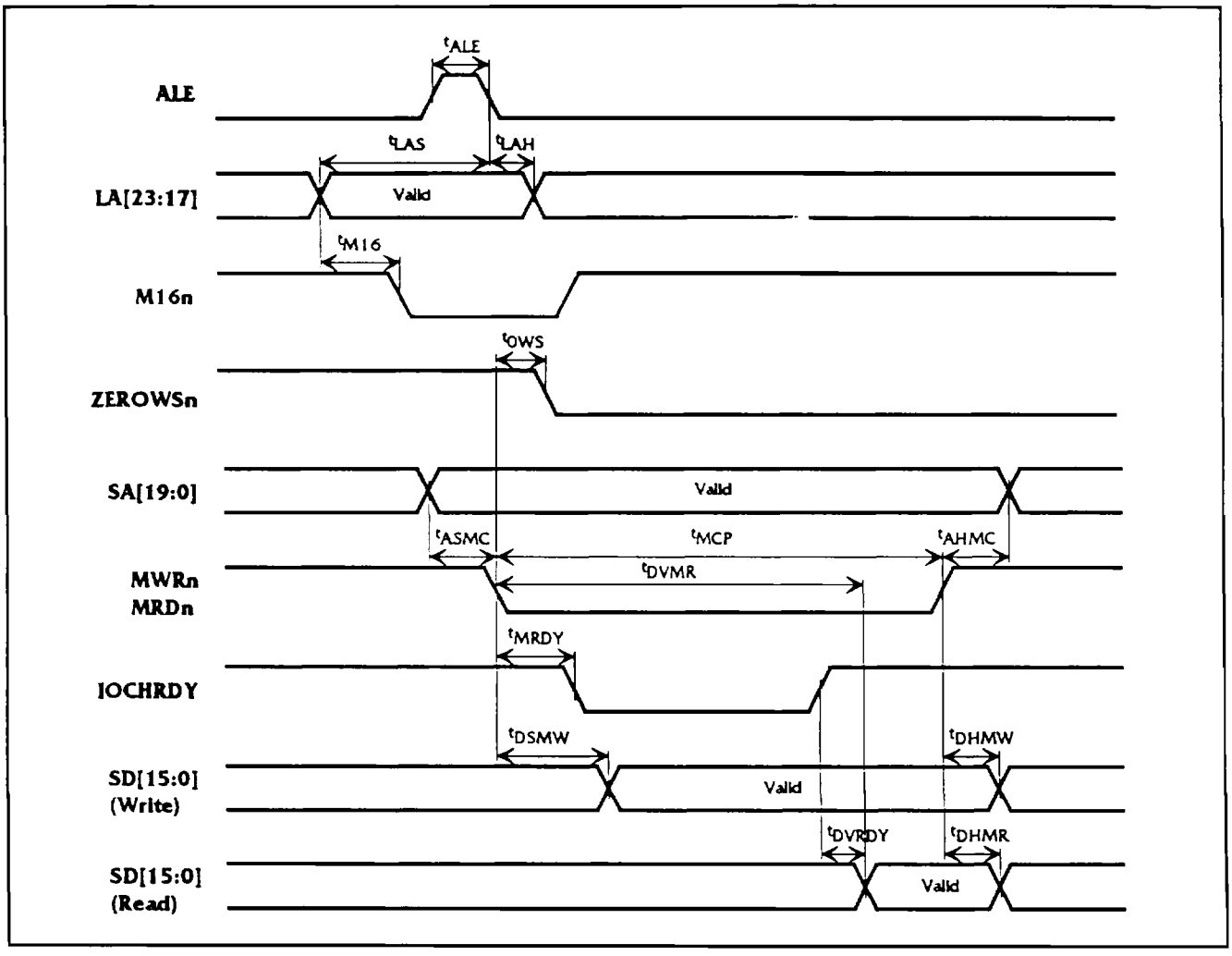
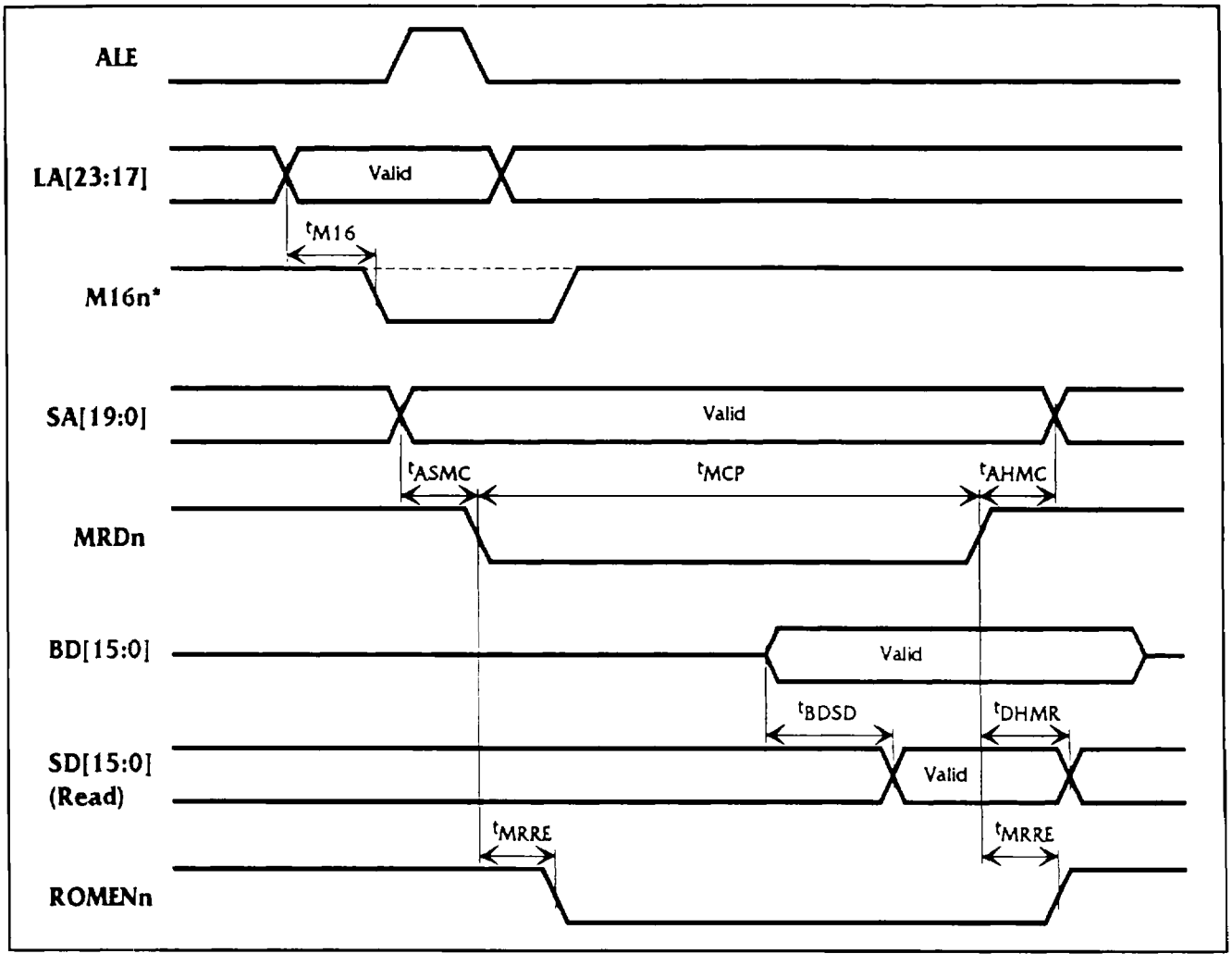
Signal Timing

Video Memory Cycle Timing



Symbol	Parameter	Min (ns)	Max (ns)
tALE	ALE Active to Inactive	40	
tLAS	LA[23:17] Setup to Falling Edge of ALE	15	
tLAH	LA[23:17] Hold from Falling Edge of ALE	5	
tM16	M16n Active from Valid LA[23:17]		40
tOWS	ZEROWSn Delay from Command		25
tASMC	SA[16:0] Setup to Memory Command Active	25	
tMCP	Memory Command Pulse Width	165	
tAHMC	SA[16:0] Hold from Memory Command Inactive	20	
tDVMR	Read Data Valid from MRDn Active (0 Wait State)		65
tMRDY	RDY Inactive from Memory Command Active		30
tDSMW	Write Data Setup to MRWn Active	-45	
tDHMW	Write Data Hold from MWRn Inactive	15	
tDVRDY	Read Data Valid from RDY Active		5
tDHMR	Read Data Hold from MRDn Inactive	0	

Video ROM Cycle Timing

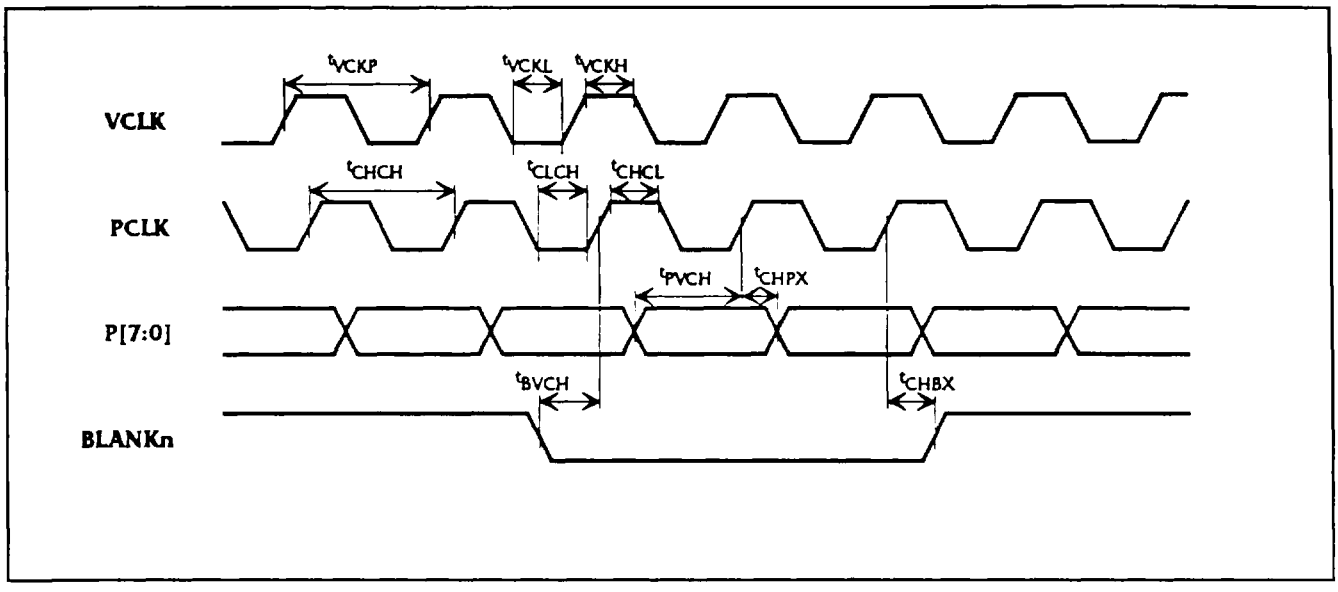


* M16n remains high when the Bus Control Register bit 4 or Configuration Register 1 bit 0 is set to 0.

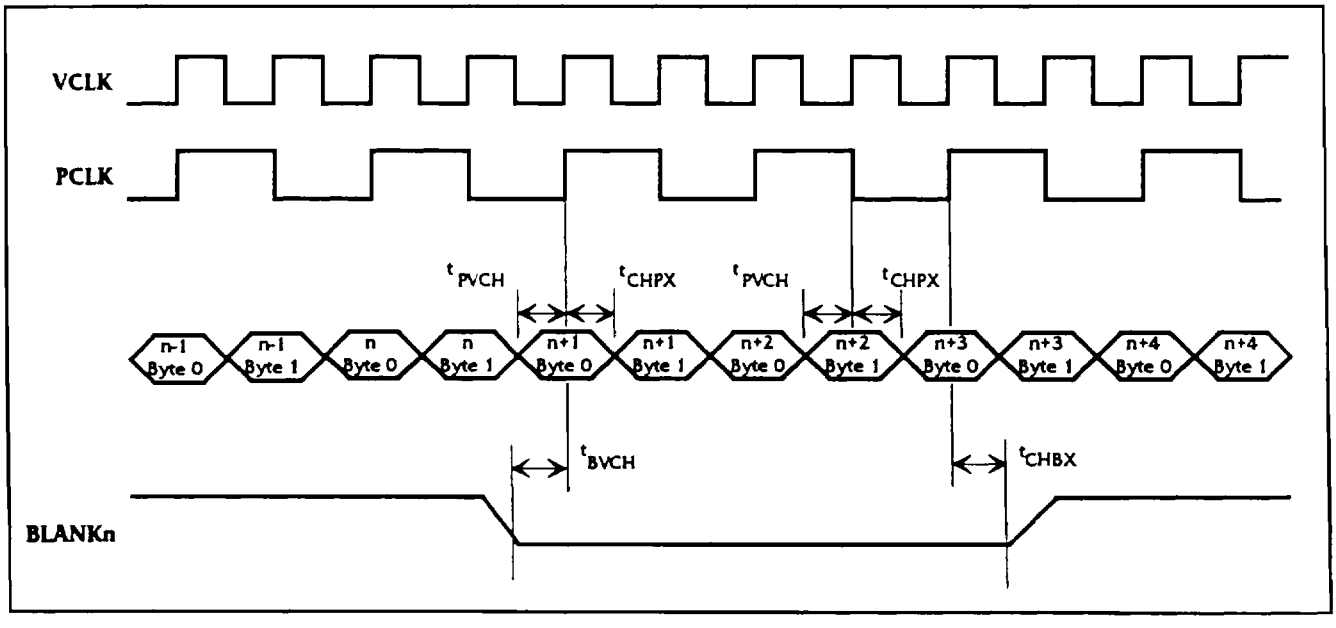
Symbol	Parameter	Min (ns)	Max (ns)
tM16	M16n Active from Valid LA[23:17]		40
tASMC	SA[16:0] Setup to Memory Command Active	25	
tMCP	Memory Command Pulse Width	165	
tAHMC	SA[16:0] Hold from Memory Command Inactive	20	
tDHMW	Write Data Hold from MWRn Inactive	15	
tDHMR	Read Data Hold from MRDn Inactive	0	
tBDSD	BD[7:0] Valid to SD[15:0] Valid		35
tMRRE	ROMENLn Delay from MRDn		25

Video Pixel Timing

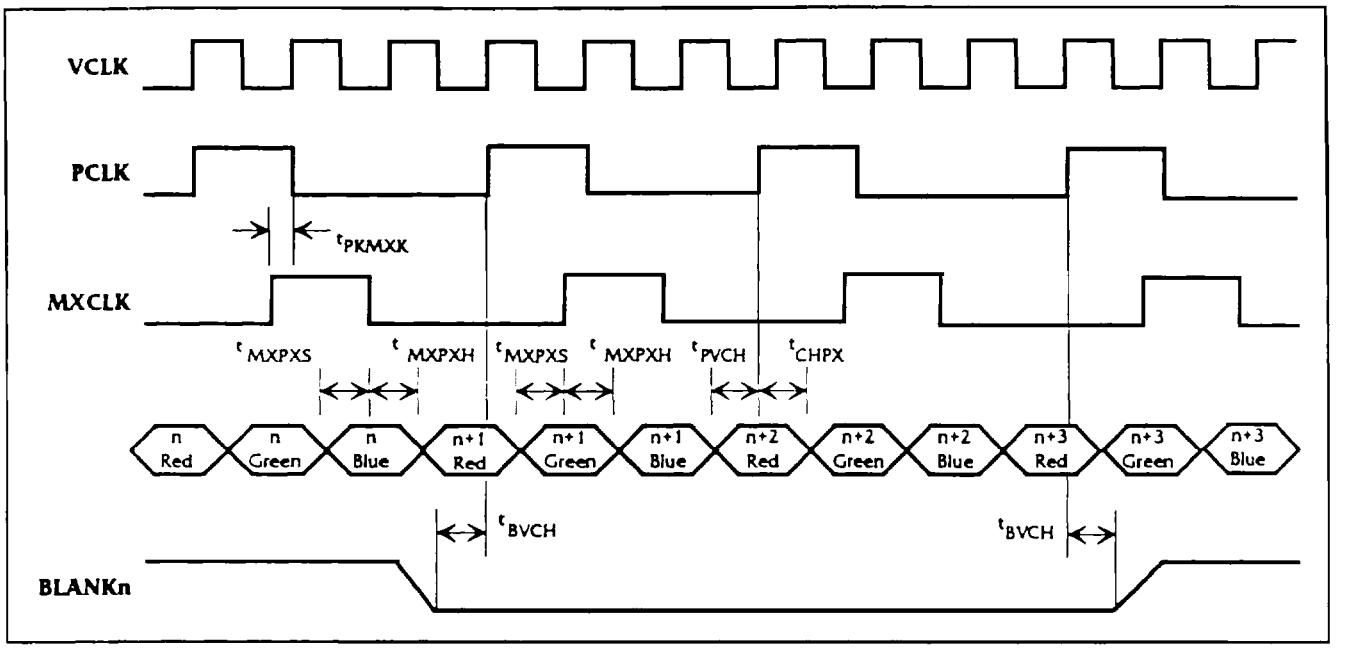
Type 0 DAC



Type 1 DAC -15/16 Bit Color



Type 1 & Type 2 DAC - True Color

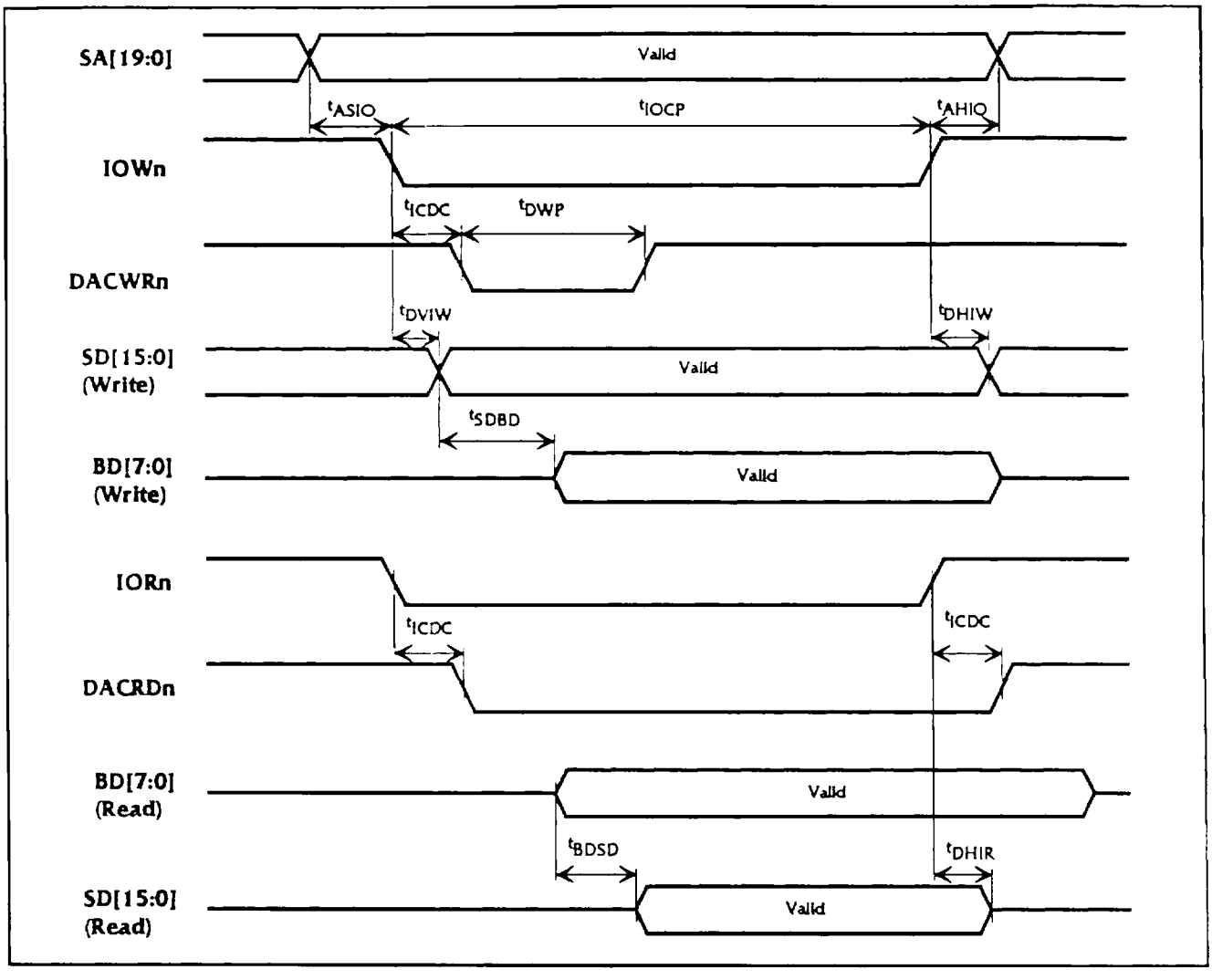


Video Pixel Timing

Type 0, Type 1 and Type 2 DAC Timing

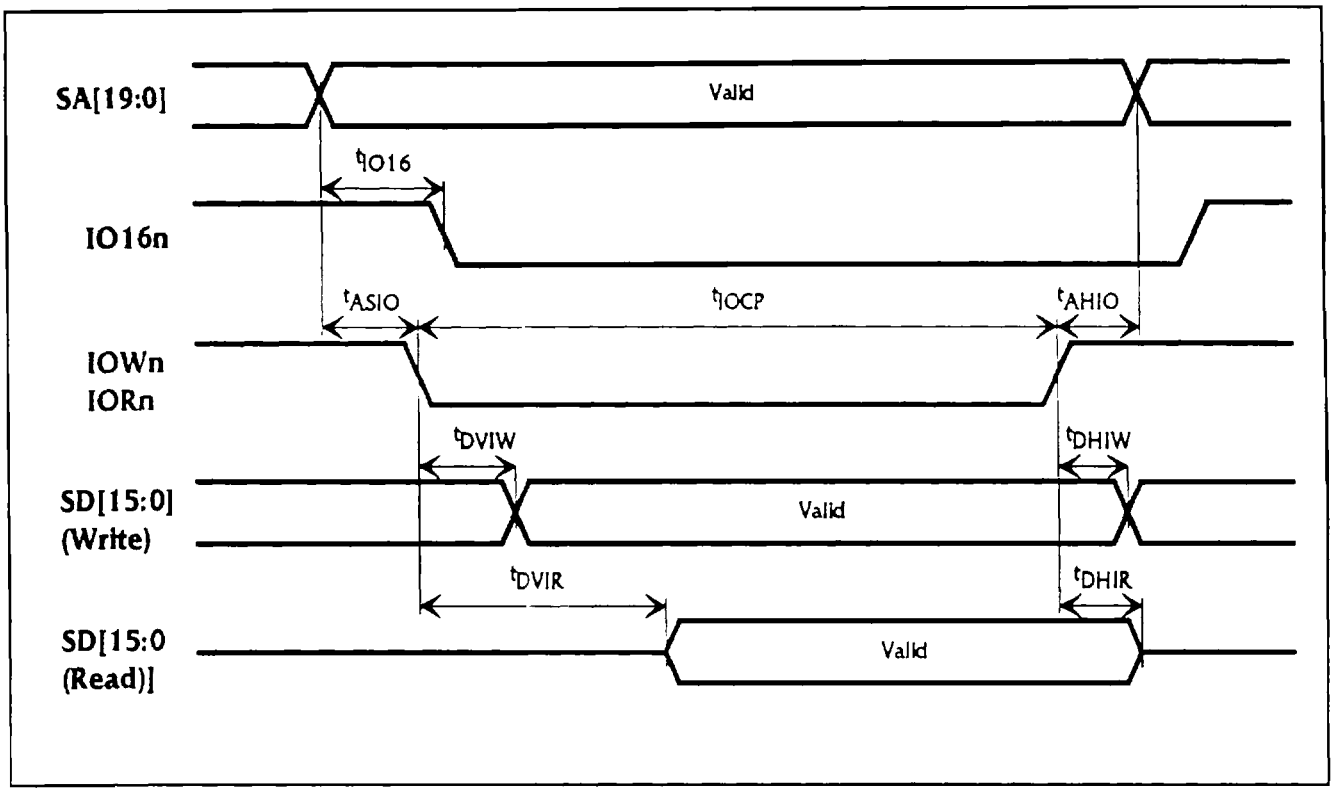
Symbol	Parameter	Min (ns)	Max (ns)
tVCKP	Video Input Clock Period	12	
tVCKH	VCLK Width High	6	
tVCKL	VCLK Width Low	6	
tCHCH	Pixel Clock Period	12	
tCHCL	PCLK Width High	tVCKH-1	
tCLCH	PCLK Width Low	tVCKL-1	
tPVCH	Pixel Word Setup Time	3	
tCHPX	Pixel Word Hold Time	3	
tBVCH	Blankn Setup Time	3	
tCHBX	Blankn Hold Time	3	
tMXPXS	Mux Clock Setup Time	3	
tMXPXH	Mux Clock Hold Time	3	
tPKMXK	Pixel Clock to Mux Clock Delay	2	

Video DAC I/O Timing



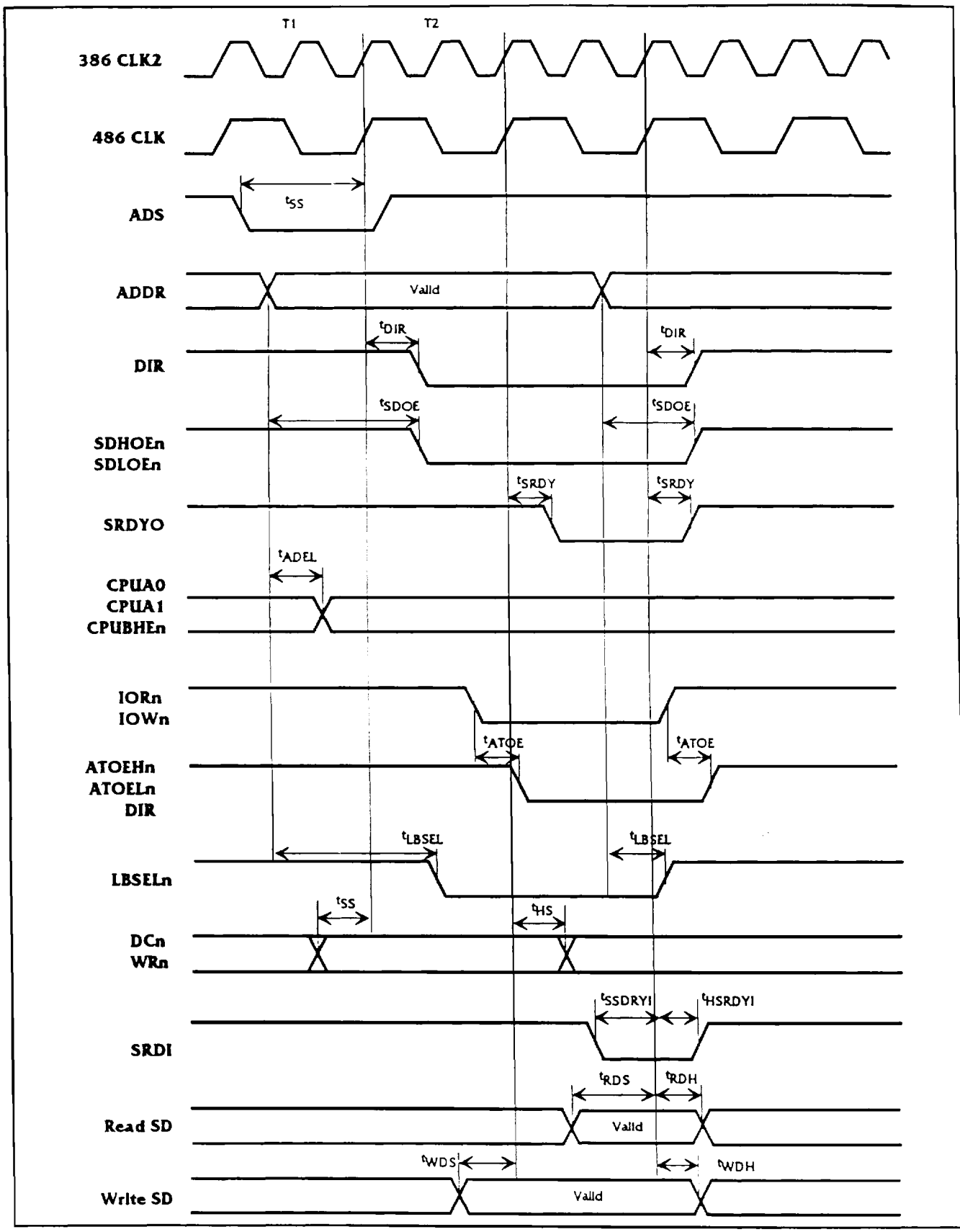
Symbol	Parameter	Min (ns)	Max (ns)
tASIO	SA[16:0] Setup to I/O Command Active	25	
tAHIO	SA[16:0] Setup from I/O Command Inactive	30	
tIOCP	I/O Command Pulse Width	115	
tDVIW	Write Data Valid from IOWn Active	-55	
tDHIW	Write Data Hold from IOWn Inactive	15	
tDHIR	Read Data Hold from IORn Inactive	0	
tICDC	DAC Command Delay from I/O Command		25
tDWP	DACWRn Pulse Width	70	
tSDBD	SD[7:0] Valid to BD[7:0] Valid		50
tBDSD	BD[7:0] Valid to SD[15:0] Valid		35

Video I/O Access Timing



Symbol	Parameter	Min (ns)	Max (ns)
tIO16	IO16n Active from Valid SA[15:0]		60
tASIO	SA[16:0] Setup to I/O Command Active	25	
tAHIO	SA[16:0] Hold from I/O Command Inactive	30	
tIOCP	I/O Command Pulse Width	115	
tDVIW	Write Data Valid from IOWn Active	- 55	
tDHIW	Write Data Hold from IOWn Inactive	15	
tDVIR	Read Data Valid from IORn Active		70
tDHIR	Read Data Hold from IORn Inactive	0	

Local Bus Interface Timing



Local Bus Interface Timing

Symbol	Parameter	Min (ns)	Max (ns)
tDIR	DIR Active from CPUCLK	6	25
tSDOE	SDHOEn, SDLOEn Active from Valid Address	6	15
tSRDY	SRDYn Active/Inactive from CPUCLK	6	15
tADEL	CPU A0, A1, BHEn Valid from BE0-3n		see Note 1
tATOE	ATOE Active from IOWRn/IORDn		20
tLBSEL	LBSELn Valid from SA		15
tSSRDYI	SRDYI Setup Time	5	
tHSRDYI	SRDYI Hold Time	3	
tSS	Status Setup Time	4	
tHS	Status Hold Time	4	
tRDS	Read Data Setup Time	12	
tRDH	Read Data Hold Time	7	
tWDS	Write Data Setup Time	7	
tWDH	Write Data Hold Time	5	

Note 1: This delay depends on the necessary external PAL. Please refer to the tables below for PAL speed requirements.

PAL Interface for 80386DX CPU

Local Bus Frequency	PAL 16L8
20 MHz	15 ns
25 MHz	15 ns
33 MHz	10 ns
40 MHz	7 ns

PAL Interface for 80486 CPU

Local Bus Frequency	PAL 16L8
20 MHz	15 ns
25 MHz	15 ns
33 MHz	10 ns

DRAM Interface Timing & Memory Refresh Timing

SYMBOL	PARAMETER	Min (ns)	Max (ns)
tMP	Memory Clock Period	22	25
tMCKR	Memory Clock Rise/Fall		2.5
tRC	Random Rd/Wr Cycle Time	7tMP	
tRP	RASn Precharge Time	3tMP	
tRAS	RASn Pulse Width	4tMP	
tCSH	CASn Hold Referenced to RASn	4tMP	
tAR	Column Address Hold Ref. to RASn	4tMP	
tRAL	Column Address to RASn Lead Time	2tMP	
tASR	Row Address Setup Time	1tMP	
tRAH	Row Address Hold Time	1tMP	
tRSH	RASn Hold Referenced to CASn	1tMP	
tASC	Column Address Setup Time	1tMP	
tCAH	Column Address Hold Time	1tMP	
tCP	CASn Precharge Time	1tMP	
tCAS	CASn Pulse Width	1tMP	
tPC	Fast Page Mode Cycle Time	2tMP	
tRAC	Access Time from RASn		4tMP
tCAC	Access Time from CASn		1tMP
tAA	Access Time from Col. Addr. (MA)		2tMP
tCPA	Access Time from CASn Precharge		2tMP
tRWL	WExxn to RASn Lead Time	1tMP	
tWCR	WExxn Hold Ref. to RASn	4tMP	
tWCS	WExxn Setup to CASn	0tMP	
tWCH	WExxn Hold Ref. to CASn	1tMP	
tCWL	WExxn to CASn Lead Time	1tMP	
tWP	WExxn Pulse Width	1tMP	
tDHR	MD Hold Ref. to RASn	4tMP	
tDS	MD Setup to WExxn	1tMP	
tDH	MD Hold to WExxn	1tMP	
tCSR	CASn Setup to RASn (Ref. Cycle) (2)	1tMP	
tCHR	CASn Hold to RASn (Ref. Cycle) (2)	2tMP	

Notes:

1. Refresh Cycles are implemented as CASn before RASn REFRESH cycles.
2. Write cycles are implemented as EARLY WRITE cycles.

DC Specification

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V

Stresses above those listed may cause permanent damage to the OTI-087. These specifications are stress ratings only and do not apply to operational use. Functional operation of this device at these or any other conditions above those indicated in this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: T_A=0°C to 70°C, V_{DD}=5V +/-5%, V_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Conditions
Voh	Output Voltage High	2.4		V	Ioh=400 uA
Vol	Output Voltage Low		.4	V	Iol=24 mA, Note 1,2
Vol	Output Voltage Low		.4	V	Iol=12 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=10 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=8 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=4 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=2 mA, Note 1
Vih	Input Voltage High	2	VCC+0.5	V	TTL, Note 3
Vil	Input Voltage Low	-0.5	0.8	V	TTL, Note 3
Iil	Input Leakage Current	-10	10	uA	
Oil	Output Leakage Current	-10	10	uA	
ICC	Operating Supply Current		125	mA	
CI	Input Capacitance		8	pF	
Co	Output Capacitance		8	pF	
Clo	I/O Capacitance		8	pF	

Notes:

1) Output Current (Iol) Capabilities:
   - 24mA: SD[15:0] with slew control.
   - 8mA: SRDY, RASLn, RASHn, CASAn, WEAn, WEBn, MA01[0], MA23[0], HSYNC, VSYNC, LBSELn, BLANKn, P[7:0], PCLK
   - 4mA: BD[7:0], MA01[8:1], MA23[8:1], MD[31:0]
   - 2mA: CSEL[3:0], DACRn, RACWn, ROMENLn

2) Open Drain (open collector) Outputs:
   - 24mA: IOCHRDY, CINTn, IO16n, M16n, ZEROWSn

3) Input Structures:
   - TTL: All