- Versatile Multiplexing Interface Allows Lower Pixel Bus Rate
- High Level of Integration Provides Lower System Cost and Complexity
- Direct VGA Pass-Through Capability
- Directly Interfaces to TMS34010/TMS34020 and Other Graphics Processors
- Triple 8-Bit D/A Converters
- 66-, 85-, 110, and 135-MHz Versions
- 256-Word Color Palette RAM
- Palette Page Register
- On-Chip Voltage Reference
- RS-343A-Compatible Outputs
- TTL-Compatible Inputs
- Standard MPU Interface
- Pixel Word Mask
- On-Chip Clock Selection
- True Color (Direct Addressing) Mode
- Directly Interfaces to Video RAM
- Supports Split Shift Register Transfers
- Software Downward-Compatible With INMOS IMSG176/8 and Brooktree™ Bt476/8 Color Palettes
- TIGA™ Software-Standard Compatible
- CMOS Technology
- Data Manual Available†

description

The TLC34075A video interface palette (VIP) is designed to provide lower system cost with a higher level of integration by incorporating all the high-speed timing, synchronizing, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, 8-, and 4-bit pixel buses to be accommodated without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. Data can be split into 1-, 2-, 4-, or 8-bit planes. The TLC34075A is software-compatible with the INMOS IMSG176/8 and Brooktree Bt476/8 color palettes.

The TLC34075A features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard. The TLC34075A also provides a true-color mode in which 24 (3 by 8) bits of color information are transferred directly from the pixel port to the DACs. This mode of operation supplies an overlay function using the 8 remaining bits of the pixel bus.

The TLC34075A has a 256-by-24 color lookup table with triple, 8-bit video, D/A converters capable of directly driving a doubly terminated, 75-Ω line. Sync generation is incorporated on the green output channel. HSYNC and VSYNC are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette page register provides the additional bits of palette address when 1-, 2-, or 4-bit planes are used. This allows the screen colors to be changed with only one MPU write cycle.

Clocking is provided through one of four or five inputs (three TTL- and either one ECL- or two TTL-compatible) and is software selectable. The video and shift clock outputs provide a software-selected divide ratio of the chosen clock input.

The TLC34075A can be connected directly to the serial port of VRAM devices, eliminating the need for any discrete logic. Support for split shift-register transfers is also provided.

The TLC34075A is an optimized version of the original TLC34075 video interface palette. Because all of the critical speed paths have been strengthened on the device, a slightly higher supply current specification is required. The new specification also includes revised SCLK/VCLK timing and a clock-counter reset function.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE
			PLASTIC CHIP CARRIER (FN)
0°C to 70°C	66 MHz	8 Bits	TLC34075-66AFN
	85 MHz	8 Bits	TLC34075-85AFN
	110 MHz	8 Bits	TLC34075-110AFN
	135 MHz	8 Bits	TLC34075-135AFN

functional block diagram

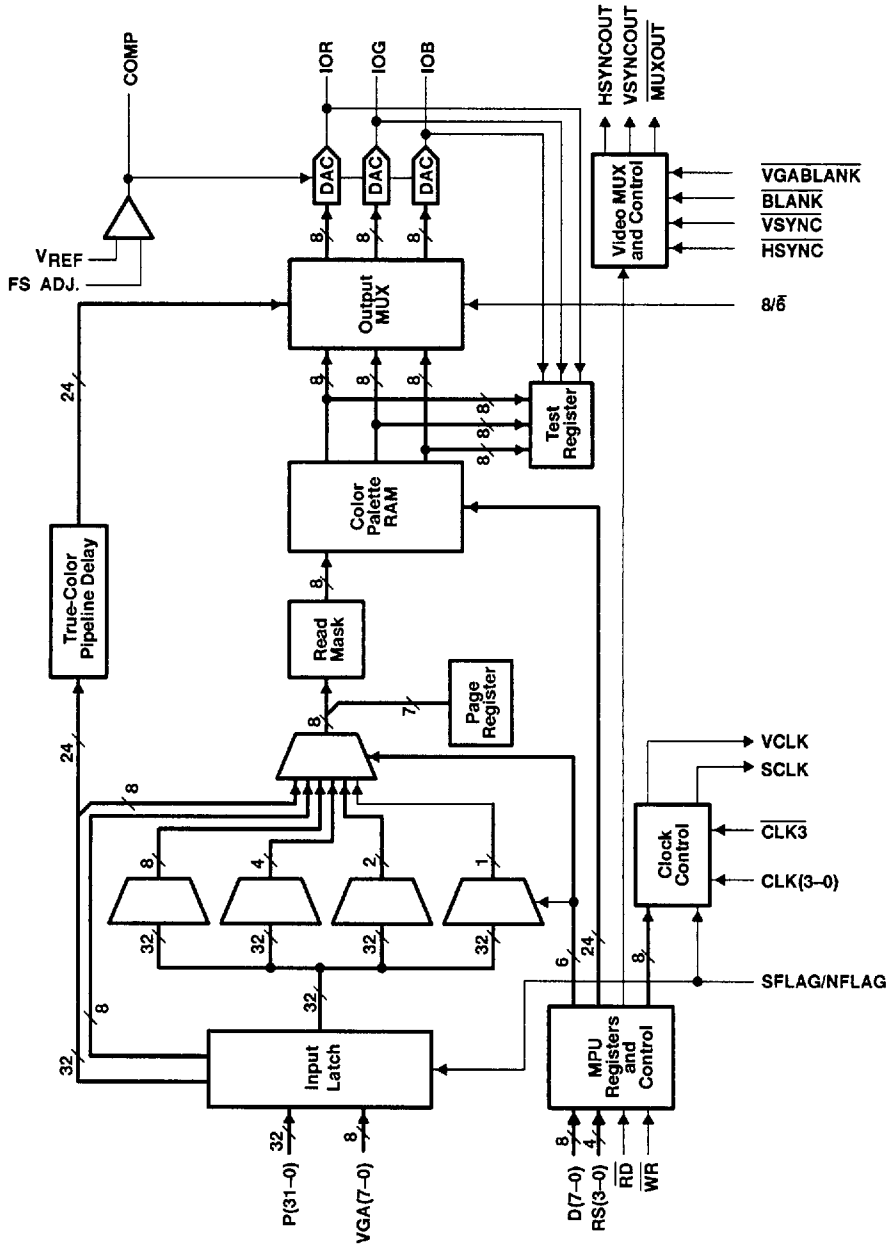

Figure 1. Functional Block Diagram