

HAF1003(L), HAF1003(S)

Silicon P Channel MOS FET Series
Power Switching

HITACHI

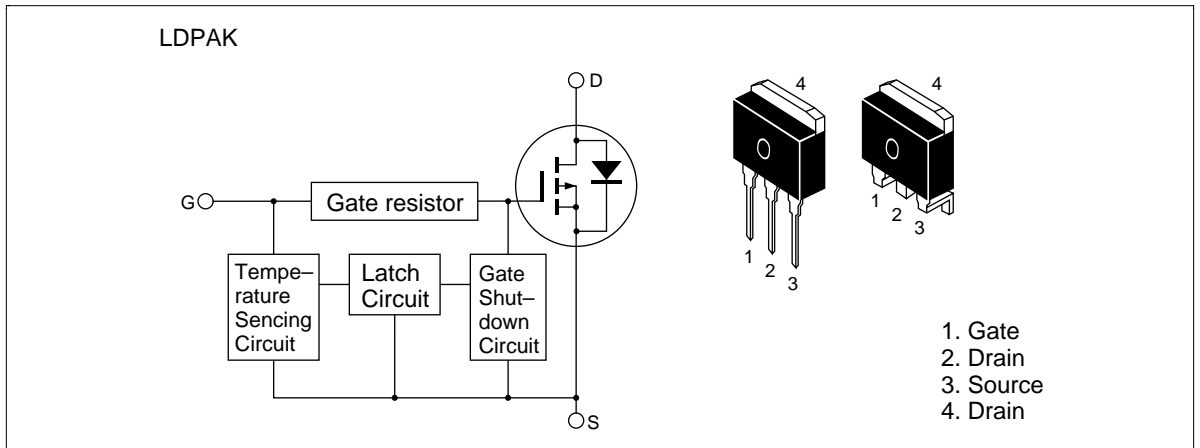
ADE-208-626B (Z)
3rd. Edition
July 2000

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc.

Features

- Logic level operation (-4 to -6 V Gate drive)
- High endurance capability against to the short circuit
- Built-in the over temperature shut-down circuit
- Latch type shut-down operation (Need 0 voltage recovery)

Outline



HAF1003(L), HAF1003(S)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS}	-16	V
Gate to source voltage	V _{GSS}	2.5	V
Drain current	I _D	-18	A
Drain peak current	I _{D(pulse)} ^{Note1}	-36	A
Body-drain diode reverse drain current	I _{DR}	-18	A
Channel dissipation	Pch ^{Note2}	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW ≤ 10ms, duty cycle ≤ 1 %
2. Value at Tc = 25°C

Typical Operation Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	-3.5	—	—	V	
	V _{IL}	—	—	-1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	-100	μA	Vi = -8V, V _{DS} = 0
	I _{IH2}	—	—	-50	μA	Vi = -3.5V, V _{DS} = 0
	I _{IL}	—	—	-1	μA	Vi = -1.2V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)1}	—	-0.8	—	mA	Vi = -8V, V _{DS} = 0
	I _{IH(sd)2}	—	-0.35	—	mA	Vi = -3.5V, V _{DS} = 0
Shut down temperature	T _{sd}	—	175	—	°C	Channel temperature
Gate operation voltage	Vop	-3.5	—	-12	V	

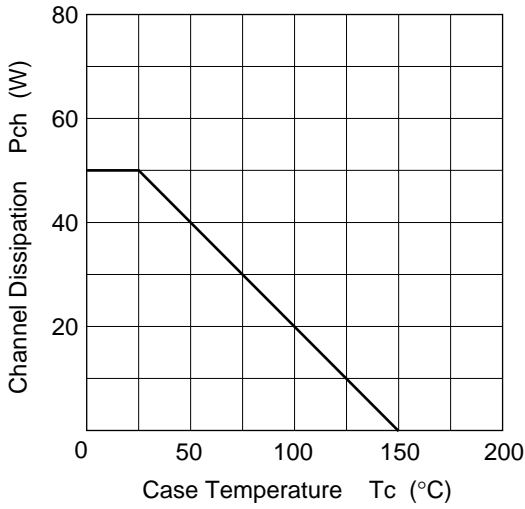
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	-6	—	—	A	$V_{GS} = -3.5V, V_{DS} = -2V$
Drain current	I_{D2}	—	—	-10	mA	$V_{GS} = -1.2V, V_{DS} = -2V$
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10mA, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-16	—	—	V	$I_G = -300\mu A, V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	2.5	—	—	V	$I_G = 100\mu A, V_{DS} = 0$
Gate to source leak current	I_{GSS1}	—	—	-100	μA	$V_{GS} = -8V, V_{DS} = 0$
	I_{GSS2}	—	—	-50	μA	$V_{GS} = -3.5V, V_{DS} = 0$
	I_{GSS3}	—	—	-1	μA	$V_{GS} = -1.2V, V_{DS} = 0$
	I_{GSS4}	—	—	100	μA	$V_{GS} = 2.4V, V_{DS} = 0$
Input current (shut down)	$I_{GS(op)1}$	—	-0.8	—	mA	$V_{GS} = -8V, V_{DS} = 0$
	$I_{GS(op)2}$	—	-0.35	—	mA	$V_{GS} = -3.5V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.1	—	-2.25	V	$I_D = -1mA, V_{DS} = -10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	80	110	m Ω	$I_D = -9A, V_{GS} = -4V$ ^{Note3}
Static drain to source on state resistance	$R_{DS(on)}$	—	52	60	m Ω	$I_D = -9A, V_{GS} = -10V$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	5.3	11	—	S	$I_D = -9A, V_{DS} = -10V$ ^{Note3}
Output capacitance	C_{oss}	—	700	—	pF	$V_{DS} = -10V, V_{GS} = 0$ $f = 1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	8.7	—	μs	$I_D = -9A, V_{GS} = -5V$
Rise time	t_r	—	44.5	—	μs	$R_L = 3.3\Omega$
Turn-off delay time	$t_{d(off)}$	—	4	—	μs	
Fall time	t_f	—	4.6	—	μs	
Body-drain diode forward voltage	V_{DF}	—	-0.9	—	V	$I_F = -18A, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	140	—	ns	$I_F = -18A, V_{GS} = 0$ $diF/dt = 50A/\mu s$
Over load shut down operation time ^{Note4}	t_{os1}	—	3	—	ms	$V_{GS} = -5V, V_{DD} = -16V$
	t_{os2}	—	1.5	—	ms	$V_{GS} = -5V, V_{DD} = -24V$

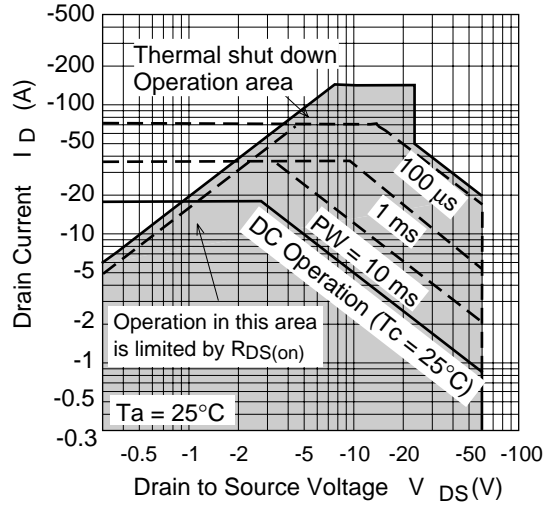
Note: 3. Pulse test

4. Including the junction temperature rise of the over loaded condition.

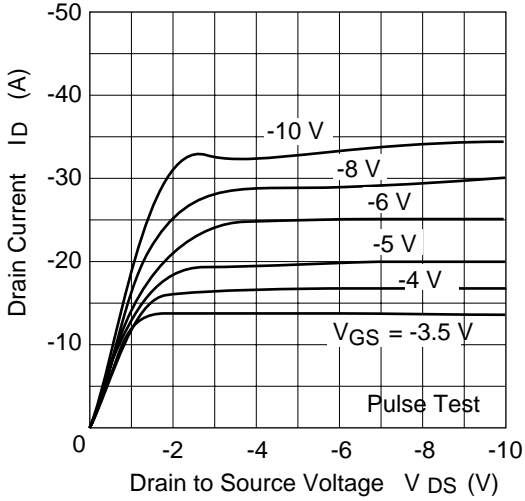
Power vs. Temperature Derating



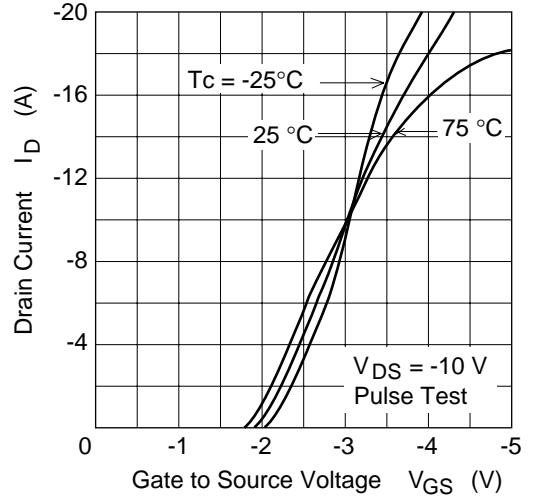
Maximum Safe Operation Area



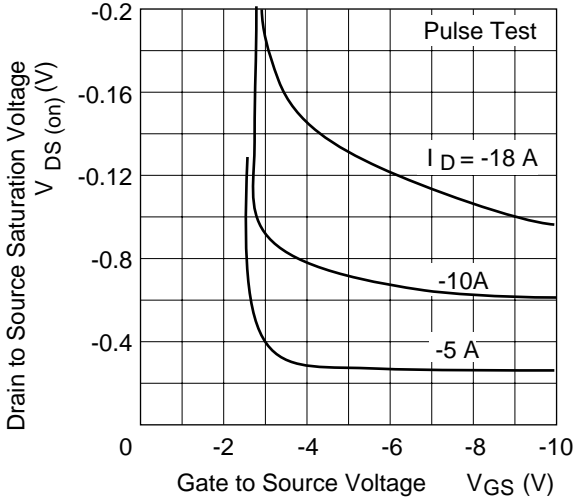
Typical Output Characteristics



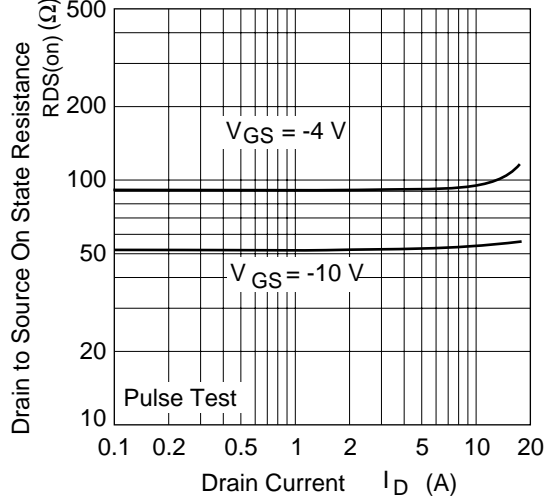
Typical Transfer Characteristics



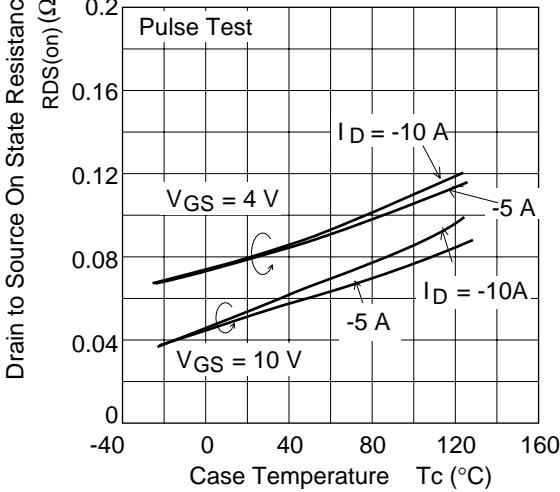
Drain to Source Saturation Voltage vs. Gate to Source Voltage



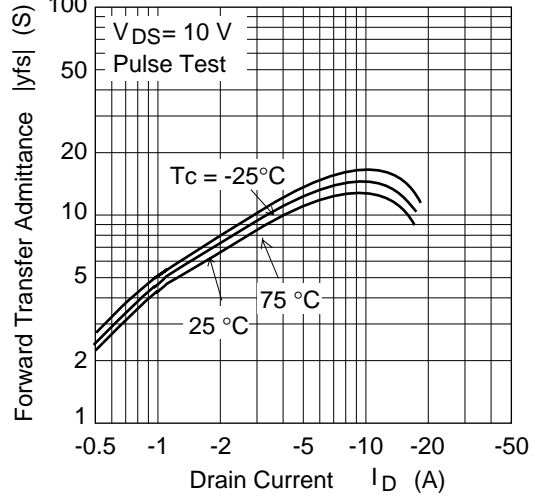
Static Drain to Source State Resistance vs. Drain Current

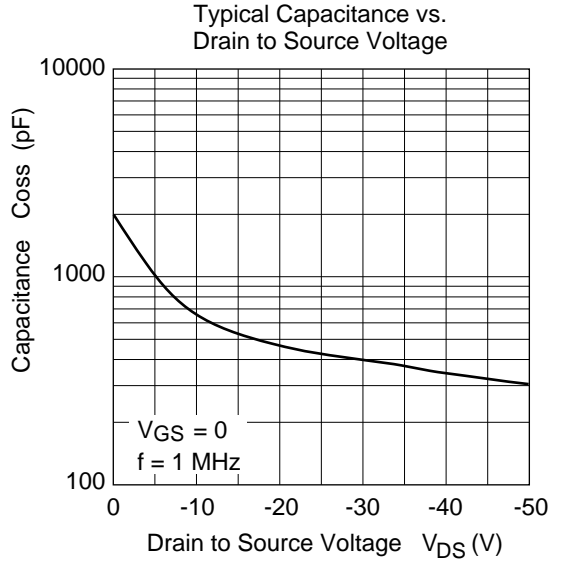
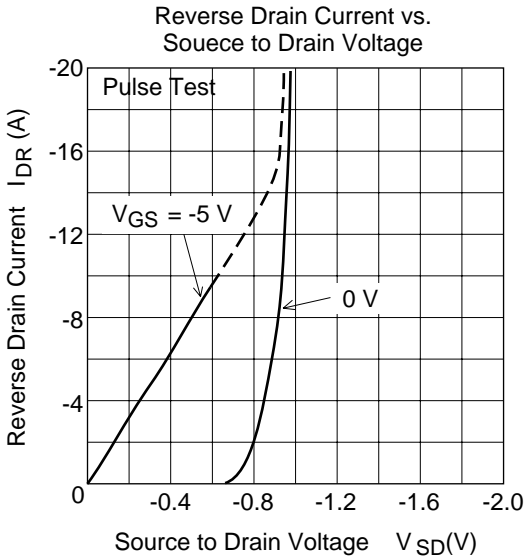
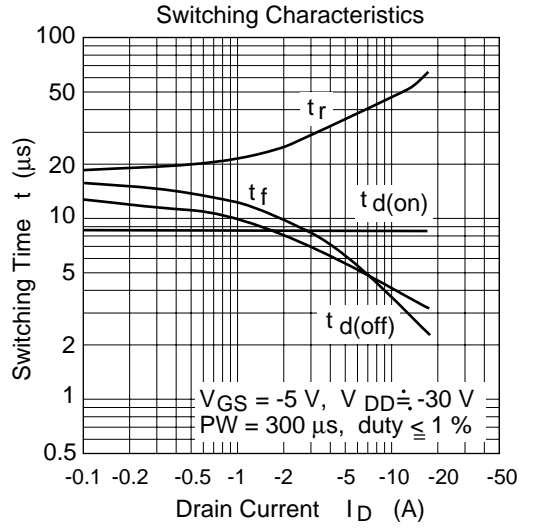
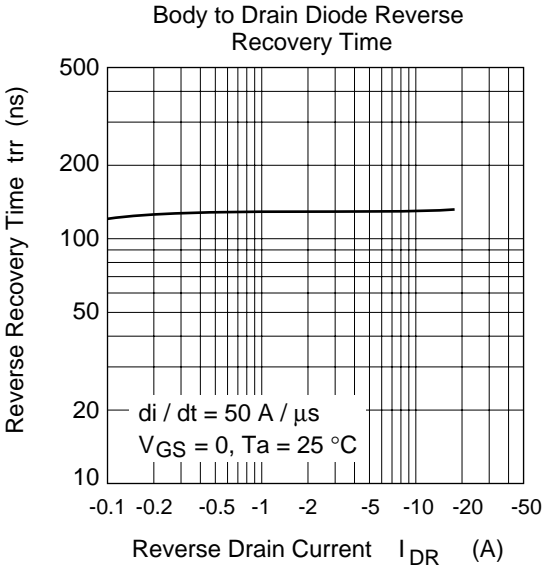


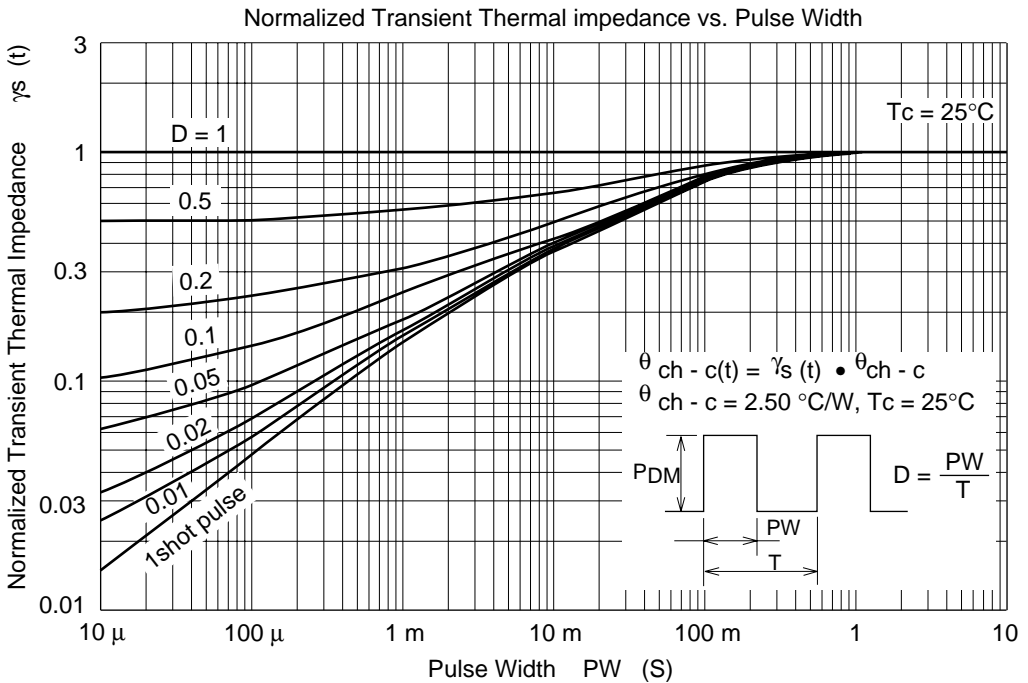
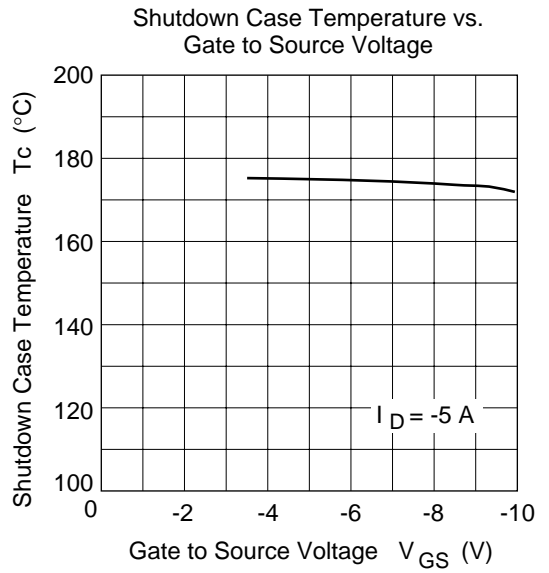
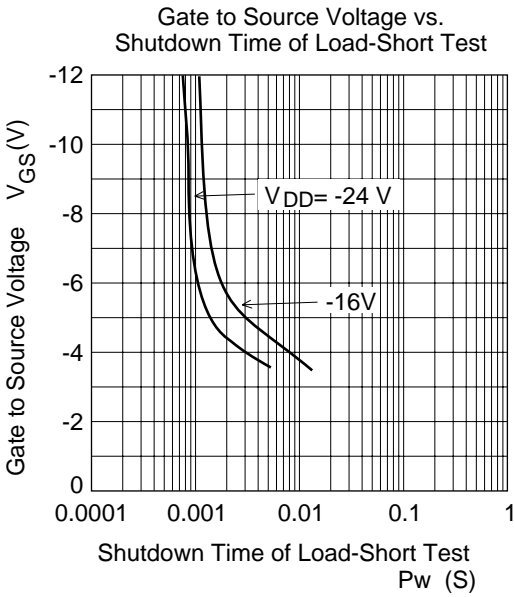
Static Drain to Source on state Resistance vs. Temperature



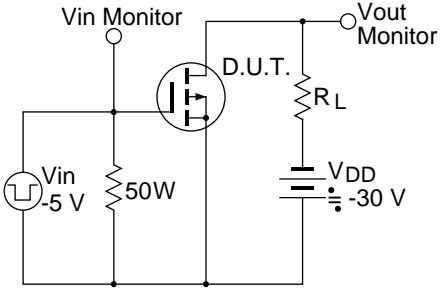
Forward Transfer Admittance vs. Drain Current



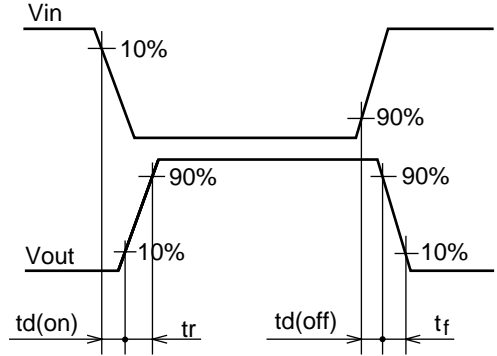




Switching Time Test Circuit

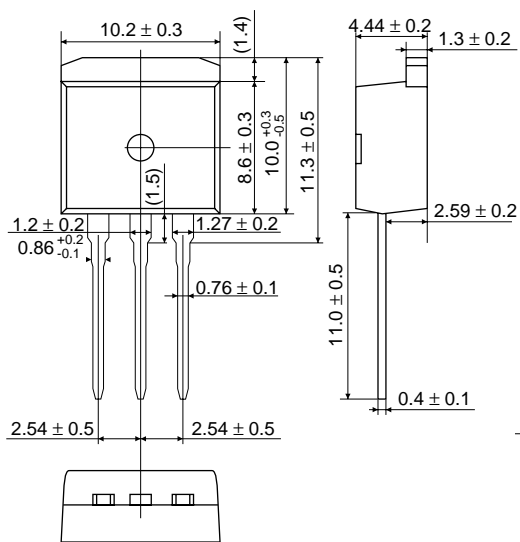


Waveform

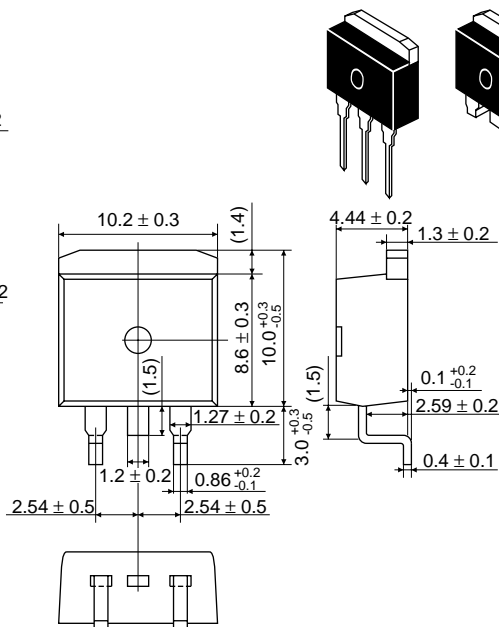


Package Dimensions

Unit: mm



Ⓛ type



Ⓢ type

Hitachi code	LDBAK
EIAJ	-
JEDEC	-

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : <http://semiconductor.hitachi.com/>
Europe : <http://www.hitachi-eu.com/hel/ecg>
Asia : <http://www.hitachi.com.sg/grp3/sicd>
Japan : <http://www.hitachi.co.jp/Sicd/indx.htm>

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher StraÙe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3rd Flr, Hung Kuo Building, No.167,
Tun Hwa North Road, Taipei (105)
Taiwan
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180
Telex: 23222 HAS-TP

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7th Flr, North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Copyright © Hitachi, Ltd., 2000. All rights reserved. Printed in Japan.
Colophon 1.0