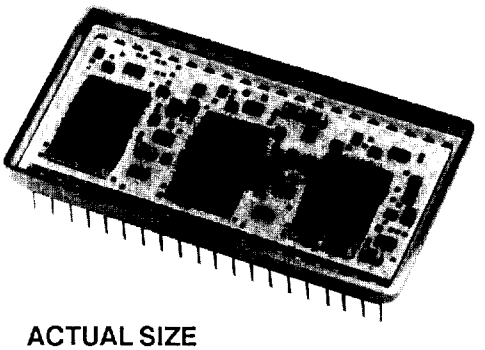
NATEL

HRD1346

3-Channel, Single Package 16-Bit Resolver-to-Digital Converters Microprocessor Compatible, 5 V-dc Only

Features

- ✓ **3 Channels in One Package** (40-Pin TDIP Hybrid)
- • **1.3 Arc-minute Accuracy**
- ✓ **Independent Tracking Converters**
- ✓ **True Single Supply . . . 5 Volts Only** (prevents ground loop problems)
- ✓ **50 mW Power Dissipation** (3 channels total)
- • **High Speed 3-State Enable** (HCT Type) 50 ns max (get on and off the bus fast)
- • **High Output Drive** (HCT Type) 10 LSTTL min
- ✓ **Analog Velocity Outputs**
- ✓ **Reference Synthesizers** (for improved dynamic accuracy)
- • **Wide Range of Signal Voltage Options** (0.5 V -- 90V-rms)
- • **Three Independent BIT Outputs (Built-In-Test)**
- • **High Tracking and Wide Bandwidth Option**
- • **8- and 16-Bit Microprocessor Compatible**
- • **On-Chip Channel Decoder** (no bus contention)
- • **MIL-STD-883 Processing is Available**



ACTUAL SIZE

Applications

Avionics systems
Antenna monitoring
Servo systems
Coordinate conversion
Fire control systems
Axis rotation
Engine controllers
Industrial control systems
Simulation
Robotics
Machine tool control systems
Solar panel control systems

Description

The **HRD1346** is the world's first 16-bit, 3-channel hybrid tracking Resolver-to-Digital converter. It contains three independent Type-II servo loop tracking converters in a single 40-pin TDIP while offering the industry's most advanced features. The **1346**, like other high performance Natel converters, operates from a single 5 V-dc power supply and consumes only 10 mA of current. This amounts to only 17 mW of power dissipation per channel, which not only makes the Natel **1346** run cool, but results in less strain on the user's power supply and higher component and system MTBF. The **1346** is fully compatible with 8- and 16-bit microprocessors and has a high frequency option with higher tracking speed and wider bandwidth. Additional standard superior features include Built-In-Test, an anti-180° false lock-up circuit, reference synthesizer, and independent high-quality analog velocity outputs.

Each channel of the **1346** is a Type-II tracking converter with zero velocity lag error. Internal reference synthesizers permit improved dynamic accuracy by reducing the effects of "speed voltages" at high rotational speeds. The accuracy of the converters are maintained with signal-to-reference phase shifts of up to ±45°. Anti-180° false lock-up circuits are used to assure that the converters do not get locked into an angle 180° from the true angle when a step function of 180° is applied.

Transferring data from the **1346** is eased through the use of a transparent latch with three-state outputs configured as two independently enabled 8-bit bytes. Not only does this allow data to be read without interrupting converter tracking, it also permits memory-mapped data interface and control with most popular 8- and 16-bit microprocessors and single-board computers. Each channel is selected onto the common data outputs by the use of two address control lines, "A0" and "A1".

Three independent Built-In-Test (BIT) outputs are available from the **1346**. The BIT feature provides a logic "1" when the tracking error exceeds ±1°. Monitoring of converter dynamics is facilitated through the availability of analog signals corresponding to converter tracking velocity. The velocity outputs are high-quality characterized analog signals that can be used instead of a mechanical tachometer in many servo and control systems.

Theory of Operation

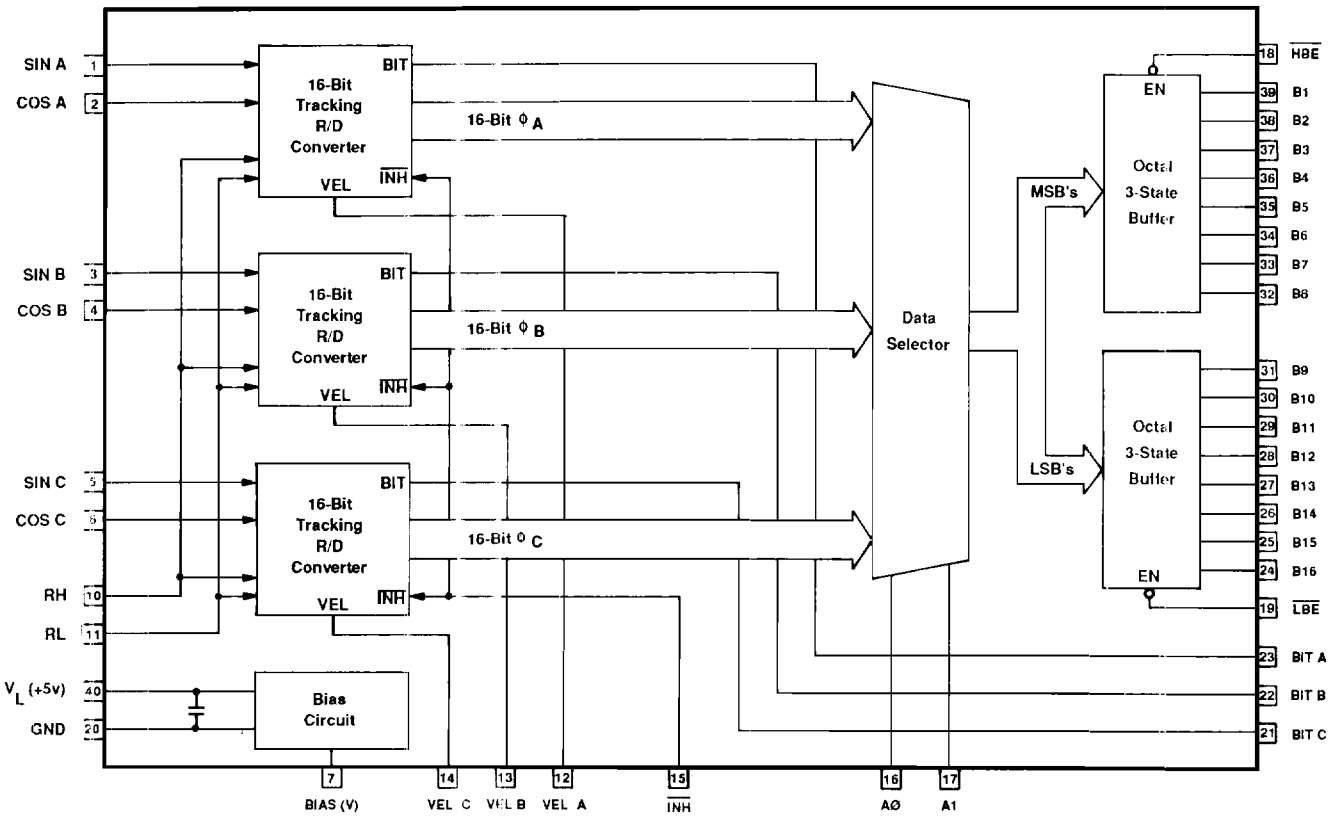


FIGURE 1 1346 Block Diagram

The operation of **Model 1346** is illustrated in the functional Block Diagram of Figure 1. The **1346** consists of three independent high-gain Type-II tracking converters exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle (ϕ) and the resolver input angle (θ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage according to the following trigonometric identity:

$$\text{"e"} = \sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

When the error voltage goes to null, $\sin(\theta - \phi)$ is zero, which makes the angle θ equal to the angle ϕ. Thus, the digital output represents the input shaft angle. Once synchronized, the output angle always tracks the input shaft angle without any lag error for constant velocity input.

A description of the internal operation of the "16-Bit tracking R-to-D converter" follows.

The resolver input signals $\sin\theta$ and $\cos\theta$ are applied to a solid state control transformer. The output of the SSCT goes to an error amplifier. The output is applied to a phase-sensitive demodulator that is used to determine the polarity (phase) of the error signal with respect to reference signal. Instead of using the external reference signal (RH, RL) as applied to the converter, **Model 1346** generates an improved reference internally. The reference synthesizer obtains this improved reference from $\sin\theta$ and $\cos\theta$ signals and uses the external reference for coarse phase determination only.

Use of the improved reference for demodulation allows the **Model 1346** to better reject quadrature components in the error signal. The demodulated error signal is applied to an integrator/filter which, in addition to ripple and noise filtering, provides the first integration required for the Type-II servo loop. The integrator/filter is also used for appropriate gain and phase compensation for loop stability (optimized for low over-shoot and fast settling time). A wide dynamic range bi-directional VCO performs a voltage-to-frequency conversion whose pulses or counts are accumulated in a 16-bit up-down counter. The up-down counter performs the second integration in the Type-II loop. The input to the VCO inherently provides an analog indication of the digital output rate of change (velocity). The "Inhibit Input" ($\overline{\text{INH}}$) provides a means of holding the digital output steady during data transfer, while allowing the converter to continuously track the input angle. A more detailed description of converter operation can be found in the data sheet for **Natel Model HSD/HRD1046**.

The "Data Selector" selects the digital output corresponding to either Channel A, Channel B, or Channel C in response to the A0,A1 logic inputs. The "3-state buffer" output is split into two 8-bit bytes to allow interfacing on both 8- and 16-bit data bus systems. The BIT A, B, C outputs provide independent fault indication for each respective channel.

Reference Synthesizer

To maintain the highest accuracy under both static and dynamic conditions, the **1346** utilizes a "reference synthesizer" (one per channel) to correct for a phase difference between the signal and reference input of up to ±45°.

Conventional tracking Resolver-to-Digital converters use a phase-sensitive demodulator to detect the phase and amplitude of the error voltage, sin $(\theta - \phi)$. One of the functions of the demodulator is to reject quadrature components in the error signal (e). A phase-sensitive demodulator rejects any quadrature signal (signal 90° out of phase) only if the resolver input and its reference are exactly in phase. Zero degree phase shift between reference and signal inputs is not practical in most applications using Resolver-to-Digital converters. Quadrature signal voltage can results from any of the following:

- dynamic resolver "speed voltages," a quadrature signal that is proportional to the shaft rotational speed
- resolver "null voltages"
- capacitive coupling between resolver lines
- differential phase shift in resolver lines

This quadrature voltage will cause angular error as a variable offset if there is a phase difference between input signals and reference. For example, for a 400-Hz resolver with a 30° phase shift rotating at 2.5 rps (900°/sec), the dynamic error due to speed voltage would be 0.17° or 10 arc-minutes!

Natel's **Model 1346** greatly reduces the effects of this error by creating a synthetic reference. The sine and cosine voltages are combined to obtain an in-phase internal reference. Together with the external reference voltage (to determine phase) this improved reference is used for demodulating the error voltage.

No 180° False Lock-up

An additional feature of the **Model 1346** eliminates "false 180° digital output readings," during instantaneous 180° input step changes. "180° false lock-up" can occur in most Resolver-to-Digital converters whenever the resolver input angle is "electronically switched" or stepped from one angle to another by 180°. This occurrence is most common in applications where the input is being supplied by a Digital-to-Resolver converter and the MSB (180° BIT) is turned "ON" or "OFF".

The reason this occurs in most Resolver-to-Digital converters is because the solid-state control transformer (SSCT) used in the conversion process can produce two (2) "nulls" at the error output "e" for a given digital feed-back angle. This is easily understood by trigonometric indentity

$$\sin [(\theta - \phi) + 180] = -\sin (\theta - \phi)$$
$$= \sin (\theta - \phi)$$

when
$(\theta - \phi) =$ zero

Since error output "e" is a sine function (see theory of operation) this creates a possibility of a second null and the converter locking-up 180° away from the true angle.

Natel's **Model 1346** gets around this problem by continuously monitoring sin θ and cos θ signals and comparing the phase relationship with the digital output angle and reference input (RH, RL). When a 180° input step is applied, the internal BIT-detect circuit is activated, which forces an error in the converter loop to move the digital output angle to the correct reading. As soon as the digital output is properly phased with the shaft angle input, this "intentional error" is removed from the converter loop.

Built-In-Test (BIT)

A BIT signal (pins 21, 22, and 23) provides an over-velocity or fault indication output signal. The error voltage of the converter is monitored continuously, and when the tracking error exceeds approximately 1° (over-velocity or failure), a logic "1" signal is generated to indicate invalid data. Under normal operation the BIT output is at logic "0". Possible conditions that will cause the BIT output to show fault indication are:

- Power-turn-on – BIT output will return to logic "0" when the converter synchronizes to correct input angle ±1°
- Step-input – instantaneous input changes greater than ±1° until the converter synchronizes
- Over velocity condition
- Excessive shaft angle modulation
- Reference voltage disconnected
- Loss of signal – all signal lines are disconnected
- Converter malfunction – any converter failure which prevents synchronization to the input angle

Note that the BIT output has ≥50% duty cycle logic "1" when reference lines or signal lines are disconnected. The cycle frequency is synchronous with the carrier frequency when either the signal or reference (but not both) is missing.

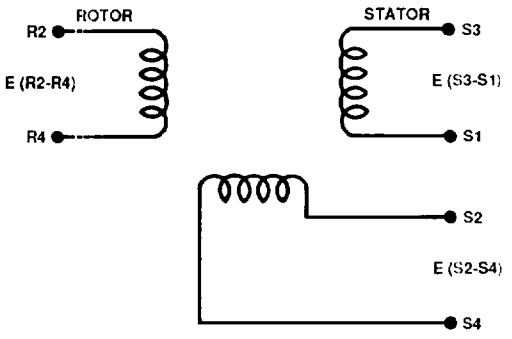
True Single-Supply 5 V-dc Operation

One of the most outstanding features of the **Model 1346** is the single +5 V-dc power supply requirement. This feature simultaneously eliminates both unwanted "ground loop" problems and allows the elimination of ± 15 V-dc power supplies in all-digital systems.

Without the single supply operation, systems that use separate analog and digital grounds for ±15 V-dc and +5 V-dc power, as many systems do, would be faced with potential ground loop problems. The result is usually excess noise on either the analog or digital supplies, which limits the effectiveness of single-point grounding schemes. These ground loops would be present with a converter that used both ±15 V-dc and digital +5 V-dc power because the analog (±15 V-dc) and digital (+5 V-dc) power supplies are referenced to different grounds while multiple supply converters have only a single internal ground. The **1346** takes the agony out of these difficult systems problems by operating entirely within the digital power and ground rails of your system.

All internal circuitry is designed to operate with power supply voltage of as low as 4.5 V-dc. This is made possible by using high signal-to-noise ratio amplifiers and a unique design approach incorporated into a custom LSI chip. No performance specification is sacrificed due to the single 5 V-dc operation. In fact, the **1346** offers the most advanced design features ever available in any Resolver-to-Digital converter.

Resolver Connections and Phasing



$V_{max} = E\ (R2\text{-}R4) \times K$

K = Resolver Transformation Ratio

θ = Resolver Shaft Angle

$E_{S3\text{-}S1} = V_{max} \sin\theta$

$E_{S2\text{-}S4} = V_{max} \cos\theta$

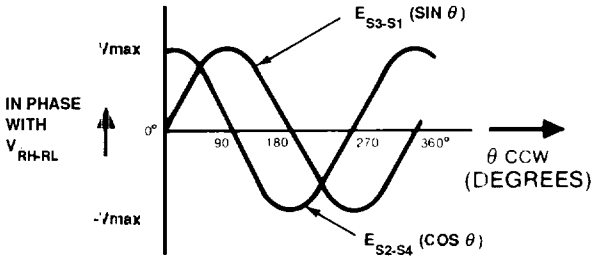


FIGURE 2 Resolver Conventions

$V_{L\text{-}L}$ INPUT	CR1-CR4
11.8 V-rms	1N6049A OR 1.5KE27CA
26 V-rms	1N6057A OR 1.5KE56CA
90 V-rms	1N6070A OR 1.5KE200CA

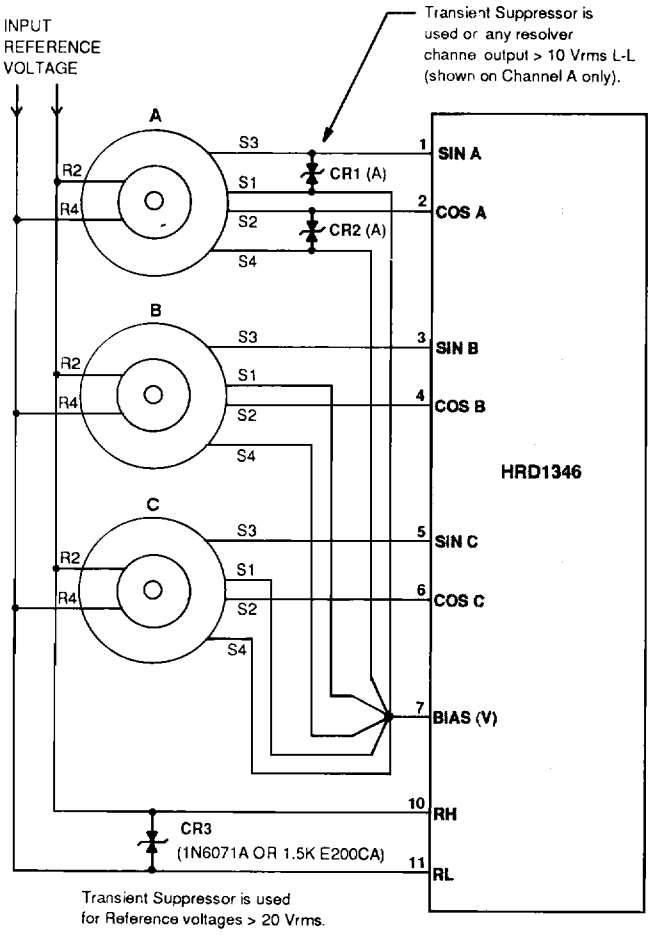


FIGURE 3 Resolver Connections

Connections of resolver(s) to the **HRD1346** are shown in Figure 3. Standard resolver "conventions" as applicable are shown in Figure 2. Resolvers normally contain a "rotor" winding (reference input) and two "signal" windings (sin and cos outputs). The sin(S3-S1) and cos(S2-S4) resolver outputs are signals which are proportional to the "product" of the "sin", "cos" (respectively) of the shaft angle θ and the reference voltage (R2,R4 or RH, RL), multiplied by the resolver transformation ratio (K). The reference input to the resolver (carrier signal) is essentially modulated by the shaft angle, producing "modulated" sin and cos outputs. The waveforms in Figure 2 represent the "demodulated" sin and cos outputs of the resolver, which essentially shows the amplitude relationship (in phase or out of phase) of the sin and cos outputs with respect to the reference input.

Resolvers are typically connected as shown in Figure 3. The "bias" (V) connection at Pin 7 serves as the "signal low" or "return" for the sin and cos resolver signals. Bias (V) is an internally generated "analog gnd" with a nominal output voltage of 2.15 V-dc. For optimum accuracy, it is best to tie the signal returns separately to common point close to Pin 7 of the **HRD1346**. The sin and cos pins are balanced resistive inputs, with the exception of the "direct" 0.5 V-rms input option, which is a voltage follower buffer input. The reference pins (RH,RL) are true differential resistive inputs, therefore either RH or RL inputs can be tied to power supply ground or left floating, depending on the source of the reference. When the nominal operating A.C. voltage levels on the signal and/or reference inputs to the **HRD1346** exceed 10 V-rms, it is recommended that transient voltage suppressors be installed. Resolvers are highly inductive and can generate or couple transients many times greater than their normal signal voltages and can easily exceed the absolute maximum ratings. Suggested transient suppressors as shown in Figure 3 (or equivalent) should be used if high voltage transients are expected.

Pin Designations

V_L	Power Supply Voltage Logic Voltage 5 V-dc ±10%
GND	Power Supply Ground Digital Ground
B1 - B16	Parallel Output Data Bits – B1 is MSB = 180 degrees B16 is LSB = 0.0055 degree
SIN A COS A SIN B COS B SIN C COS C	Input Analog Signals A = channel A inputs B = channel B inputs C = channel C inputs
RH, RL	Reference Voltage Input
VEL A VEL B VEL C	Velocity Output – dc analog voltage proportional to rotational speed of the input shaft angle. Output is referenced to bias voltage (V)
BIAS (V)	Bias Voltage – Internally generated reference voltage, serves as signal return for sin/cos inputs and reference ground for the velocity outputs
A0 A1	Output Data Select Controls – Selects desired data at B1 through B16 to represent "Channel A", "Channel B", or "Channel C" angle information
$\overline{INH}$	Inhibit Function – A logic "0" freezes the digital angular output of all Resolver-to-Digital channels. Internal loop keeps tracking the analog input. For continuous operation this pin may be left unconnected. Internal pull-up will apply V_L to the pin.
BIT A BIT B BIT C	Built-In-Test – A "1" output indicates that output is not tracking the input analog signal within ±1°.

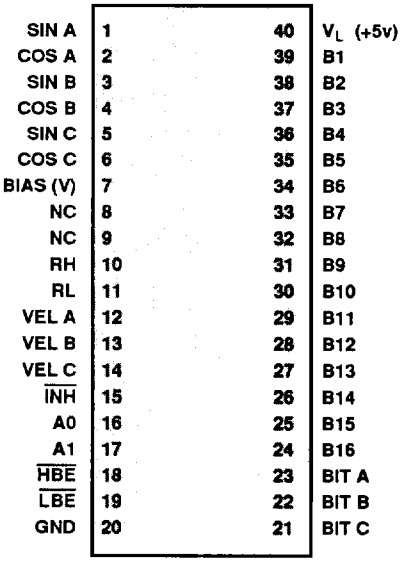


FIGURE 4 HRD1346 Pin Assignments

$\overline{HBE}$	High Byte Enable – Data bits B1 through B8 are enabled (low-impedance state of 3-state output) when $\overline{HBE}$ is set to a logic "0". When $\overline{HBE}$ is set to a logic "1" (or left floating), the data bits B1 through B8 are disabled (high-impedance state of 3-state output).
$\overline{LBE}$	Low Byte Enable – Data bits B9 through B16 are enabled when $\overline{LBE}$ is set to a logic "0". When $\overline{LBE}$ is set to a logic "1" (or left floating), the data bits B9 through B16 are disabled (high-impedance state of 3-state output).

Absolute Maximum Ratings

Signal Inputs	Twice Normal Voltage
Reference Input	Twice Normal Voltage or 150 V-rms (whichever is less)
Supply Voltage (V_L)	+6.5 V-c
Digital Inputs	−0.3 V-cc to V_L
Storage Temperature	−65°C to −135°C

When installing or removing the converter from printed circuit boards or sockets, it is recommended that the power supplies and input signals be turned off. Decoupling capacitors are recommended on the power supply V_L. A 1 μF tantalum capacitor in parallel with 0.01 μF ceramic capacitor should be mounted as close to the supply pin (40) as possible.

Specifications

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Output Resolution			
	16-bits (0.33 arc-minutes)		Note 2
Accuracy			
	±5.2 arc-minutes (Option S) ±2.6 arc-minutes (Option H) ±1.3 arc-minutes (Option V)	Accuracy applies over the full operating temperature range, ±10% frequency variation and includes hysteresis	Note 1
Reference Input			
Voltage	0.1 to 0.6 V-rms 1.0 to 10.0 V-rms 4.0 to 35.0 V-rms 20.0 to 130.0 V-rms	signal = 0.5 V-rms (Option 5) signal = 1–7 V-rms (Options 0, 3, 4, 6, 7, 8) signal = 11.8 or 26 V-rms (Options 1, 2) signal = 90 V-rms (Option 9)	Note 1
Frequency	1800 to 3000 Hz (Option 2) 700 to 3000 Hz (Option 8) 360 to 1000 Hz (Option 4) 47 to 1000 Hz (Option 6)	2000 Hz Models (400 Hz BW) 800 Hz Models (200 Hz BW) 400 Hz Models (100 Hz BW) 60 Hz Models (20 Hz BW)	Note 3
Input impedance (minimum)	RH-RL / Line-GND 1 megohm / 1 megohm 20 K ohm / 10 K ohm 80 K ohm / 40 K ohm 500 K ohm / 250 K ohm	(0.1 to 0.6 V-rms) Option 5 (1.0 to 10.0 V-rms) Option 0, 3, 4, 6, 7, 8 (4.0 to 35.0 V-rms) Option 1, 2 (20.0 to 130.0 V-rms) Option 9	Note 2
Common Mode Range (total peak voltage with respect to GND)	+1.2 to +3.1 V-dc ±15 V-dc ±50 V-dc ±250 V-dc	(0.1 to 0.6 V-rms) Option 5 (1.0 to 10.0 V-rms) Option 0, 3, 4, 6, 7, 8 (4.0 to 35.0 V-rms) Option 1, 2 (20.0 to 130.0 V-rms) Option 9	Note 3
Resolver Inputs			
Input Voltages	0.5 V-rms (Options 0, 5) 1.0 V-rms (Option 3) 2.0 V-rms (Option 4) 3.0 V-rms (Option 6) 5.0 V-rms (Option 7) 7.0 V-rms (Option 8) 11.8 V-rms (Option 1) 26.0 V-rms (Option 2) 90.0 V-rms (Option 9)	Accuracy is maintained with ±10% variation in signal voltages Inputs are with respect to the internal analog gnd "Bias" (V)	Note 1
Input Impedance	4000 ohms/volt ±10% 1 megohm min	With respect to "Bias" (V) Option 0, 5 (0.5 V-rms)	Note 2
Impedance Match	±1% max	Sin/Cos impedance match (except option 0, 5)	Note 3
Harmonic Distortion	10% max	Without degradation of accuracy	Note 3
Reference Synthesizer			
Phase-shift allowed between Input signals and Input reference	±45° guaranteed ±65° typical	Without any degradation of converter accuracy	Note 2
Digital Inputs		CMOS transient protected	
$\overline{HBE}$	Logic "1" Logic "0"	8 MSB's are in the high impedance state of 3-state output 8 MSB's are enabled	Note 1
$\overline{LBE}$	Logic "1" Logic "0"	8 LSB's are in the high impedance state of 3-state output 8 LSB's are enabled	Note 1
$\overline{INH}$	Logic "1" Logic "0"	Digital output follows analog input signal Output data latched in holding register (does not interrupt converter tracking loop)	Note 1
Channel Select (A0, A1)	A0 / A1 / Channel 0 / 0 / A 1 / 0 / B 0 / 1 / C		Note 1

Specifications Continued

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Inputs Continued		CMOS transient protected	
Voltage Levels Logic "0" Logic "1"	 −0.3 to +0.8 V-dc +2.4 to +5.0 V-dc	For V_L = 5 V-dc	Note 2
Input Currents $\overline{HBE}$, $\overline{LBE}$, A0, A1 $\overline{INH}$	 100 K ohm (typical) pull up to the power supply (V_L) −45 μA (typ), −90 μA (max) active pull up to the power supply (V_L)	 When not used, may be left unconnected	Note 3
Digital Outputs		CMOS Outputs	
Data Bits (B1-B16)	Natural Binary Angle	Positive logic (B1 = MSB = 180°)	
BIT (A, B, C)	Logic "0" Logic "1"	Digital output tracking analog input Fault indication (tracking > ±1° typical)	Note 1
Drive Capability Data Bits (B1-B16) Logic "0" sink Logic "1" source BIT A, B, C Outputs Logic "0" sink Logic "1" source	 10 LS TTL loads min +4.0 mA (min) @ 0.4 V −4.0 mA (min) @ 3.0 V 4 LS TTL loads min +1.6 mA (min) @ 0.4 V −1.6 mA (min) @ 3.0 V	For V_L = 4.5 V-dc, over full temperature range "HCT type" data outputs (B1-B16)	Note 3
HI-Z Output Leakage Data Bits (B1-B16)	±10 μA maximum	Output capacitance = approximately 10 pF	Note 3
Bias (V) Output	Typical, unless specified	Internal Analog Ground	
Voltage	1/2 (V_L − 0.7) ±10%	2.15 V-dc ±10% for 5 V-dc supply	Note 3
Drive Capability	±3 mA minimum	Short circuit current limited	Note 3
Velocity Outputs	Typical, unless specified	dc voltage referenced to bias (V)	
Polarity	Negative for increasing angle		Note 3
Scale Factor (Gain) @ 25°C	0.835 mV/deg/sec typical 1.22 mV/deg/sec typical 6.11 mV/deg/sec typical	800 Hz and 2000 Hz Models 400 Hz Models 60 Hz Models	Note 2
Temperature Coefficient Power Supply Dependence	±500 PPM/°C typical −1% per percent maximum		Note 3
Full Scale Output @ 25°C	1.5 V-dc @ 1800°/sec typical 1.1 V-dc @ 900°/sec typical 1.1 V-dc @ 180°/sec typical	800 Hz and 2000 Hz Models 400 Hz Models 60 Hz Models	Note 2
Linearity @ 25°C	±5% of full scale maximum ±2% of full scale maximum ±1% of full scale maximum	800 Hz and 2000 Hz Models 400 Hz Models 60 Hz Models	Note 2
Temperature Coefficient Power Supply Dependence	±200 PPM/°C typical −0.1% per percent maximum		Note 3
Output Noise Static Input Maximum tracking rate	 3 mV-rms typical 15 (30) mV-rms typical	 All Models For 2000, 800, 400 (60) Hz Models	 Note 3 Note 3
Output Offset at 25°C	±5 mV-dc typical ±20 mV-dc maximum	All Models	Note 2
Temperature Coefficient Power Supply Dependence	±30 μV/°C typical ±20 μV per percent typical		Note 3
Δ Gain vs Polarity	10% maximum	All Models	Note 2
Temperature Coefficient Power Supply Dependence	±200 PPM/°C typical −0.1% per percent maximum		Note 3
Drive Capability	±1 mA minimum	Short circuit current limited	Note 3

PARAMETER	VALUE	REMARKS	TEST LEVEL
Dynamic Characteristics	Typical, unless specified	Specified for power supply = +5 V-dc	
Velocity Constant (K_V)	∞	Type-II servo loop	Note 3
Tracking Rate (minimum)	1800°/sec 900°/sec 180°/sec	800 Hz, 2000 Hz Models 400 Hz Models 60 Hz Models	Note 1
Maximum Acceleration (typical)	1,600,000°/sec^2 400,000°/sec^2 100,000°/sec^2 4,000°/sec^2	2000 Hz Models 800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Acceleration Constant (nominal)	768,000 /sec^2 192,000 /sec^2 48,000 /sec^2 1,920 /sec^2	2000 Hz Models 800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Acceleration for 1 LSB error (LSB = 0.0055°) (nominal)	4.218°/sec^2 1.055°/sec^2 264°/sec^2 11°/sec^2	2000 Hz Models 800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Settling time to 1 LSB (for 179° step change)	125 ms maximum 150 ms maximum 300 ms maximum 1350 ms maximum	2000 Hz Models 800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Settling time to 1 LSB (small signal step < 1.4°)	15 ms maximum 25 ms maximum 50 ms maximum 250 ms maximum	2000 Hz Models 800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Converter Bandwidth	400 Hz typical 200 Hz typical 100 Hz typical 20 Hz typical	2000 Hz Models 800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Power Supply			
Voltage	5 V-dc ±10%	Without degradation in accuracy specification	Note 3
Current	20 mA typical, 40 mA maximum 10 mA typical, 20 mA maximum	800 Hz, 2000 Hz Models 400, 60 Hz Models	Note 1
Thermal Characteristics			
Junction Temperature Rise Above Case	1°C typical, 3°C maximum	For component with highest temperature rise	Note 3
Case Temperature Rise Above Ambient	2°C typical, 5°C maximum 10°C max (800, 2000 Hz Models)	Without any heat sink	Note 3
Power Dissipation	50 mW typical, 100 mW maximum 200 mW max (800, 2000 Hz Models)	For V_L = 5 V-dc	Note 3
Physical Characteristics			
Type	40-pin Hermetic Triple Dip		
Size	1.14 x 2.14 x 0.23 inch (29 x 54.4 x 5.9 mm)	3 Standoffs are added to the package to insulate it from the printed circuit board traces (Standoffs included in 0.23" height dimension)	Note 3
Weight	0.9 oz (26 g) maximum		

NOTE 1: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

NOTE 3: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

If your application requires 100% testing of any additional parameters of this specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

Digital I/O Characteristics and Timing

R_L = 200 KΩ Input t_r t_f = 20 ns V_L = 5 V-dc C_L = 50 pF

(Specifications apply over full operating temperature range.)

CHARACTERISTIC	LIMITS			UNITS	FIGURE
	MIN	TYP	MAX		
Inhibit to Data Stable (t_{PIDS})	0	700	1000	ns	5, 6
Inhibit to Data Update (t_{PIDU})	100	—	—	ns	5, 6
Inhibit Update Pulse Width (t_{IPW})	2.0	—	—	μs	6
3-State High Z to Low Z (t_{PHZL})	—	15	50	ns	7
3-State Low Z to High Z (t_{PLZH})	—	15	50	ns	7
Channel Select Time (t_{SEL})	—	150	300	ns	8
Output Transition Time (10%-90%) B1-B16	—	6	20	ns	—

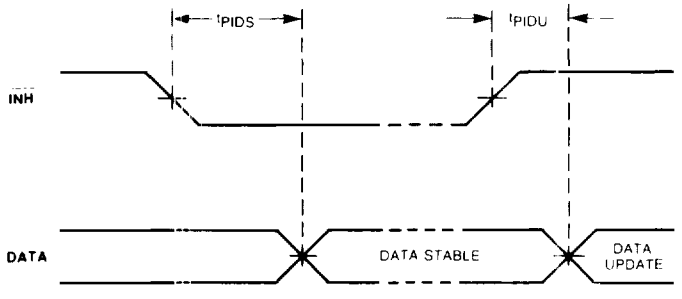


FIGURE 5 Inhibiting Output Data Update

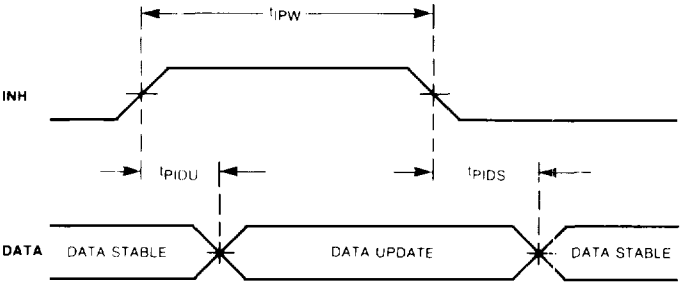


FIGURE 6 Enabling Output Data Update

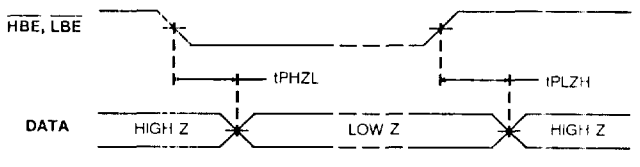


FIGURE 7 3-State Output Timing

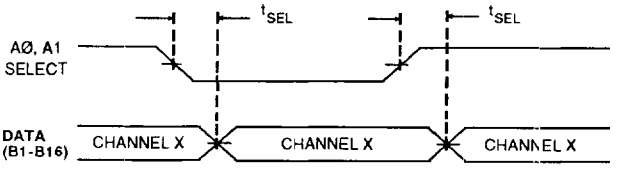


FIGURE 8 Channel Select Time

Data Transfer

Due to the nature of the Type-II servo conversion mechanism incorporated in the **1346**, the output data angle always tracks the resolver input shaft angle within the converter's rated maximum tracking rate (angular velocity) and bandwidth. Theoretically, for every 0.0055 degree of input angle change, there will be a corresponding data output change of one LSB. To prevent reading data during an output change or transition, $\overline{INH}$ input should be used.

The best method of data transfer (which is completely independent of input shaft angle change) is to use the inhibit ($\overline{INH}$) function to hold or freeze the current data output angle. Set the $\overline{INH}$ input to logic "0" . . . wait a minimum of 1 μs . . . transfer the data . . . return $\overline{INH}$ to logic "1" for a minimum of 2 μs. This method of asynchronous data transfer from the **1346** is shown in Figure 10 and Figure 11.

It should be noted that the $\overline{INH}$ control does not affect the conversion process . . . it only affect the transparent output latch. If the resolver angle input changes while an inhibit is applied ($\overline{INH}$ = "0"), the internal data angle (up-down counter output) will still track the input. Fresh output data (B1-B16) will be available within 2 μs after the $\overline{INH}$ input returns to logic "1" (un-inhibit), regardless of the previous $\overline{INH}$ logic "0" duration.

Since each converter channel is an independent "tracking type" converter, no external "start conversion" or "clock" signals are required. The digital angle output for each respective channel "continuously" tracks the corresponding resolver angle input. If the $\overline{INH}$ (inhibit) input is tied to logic "1", the data output (B1-B16) will continuously "track" the selected converter channel input. For "non-bus" and/or "no-clock" systems, the **1346** converter can be connected as shown in Figure 9 for "continuous data transfer".

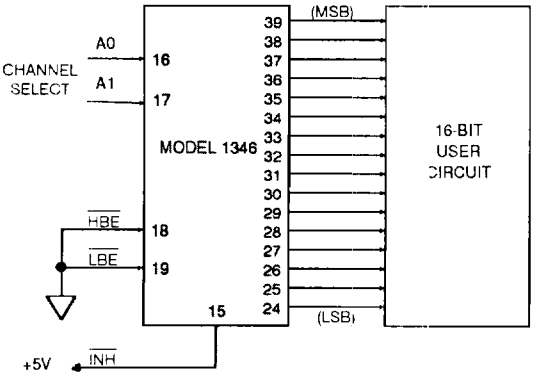
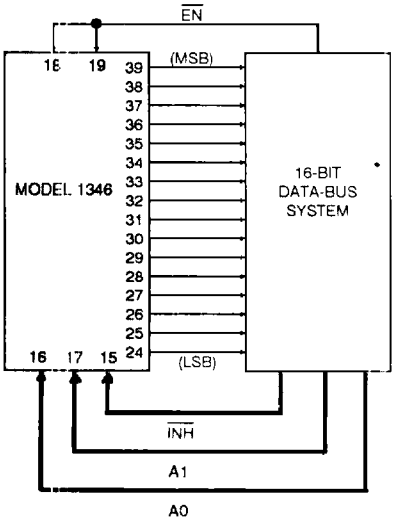


FIGURE 9 Continuous Data Transfer

Single-Byte Data Transfer on 16-Bit Data Bus



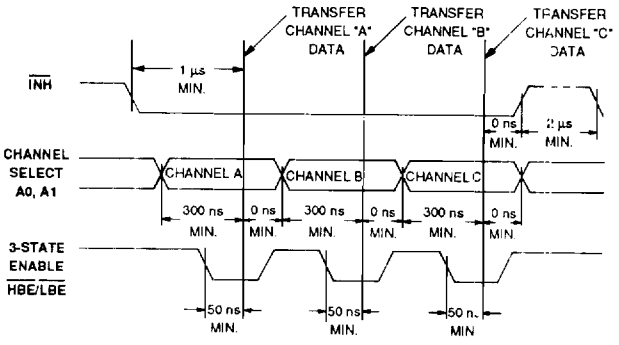


FIGURE 10 Digital Connections and Timing for Single-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from the **Model 1346** to a 16-bit 3-state data-bus system is shown in Figure 10. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 1 μs before transferring valid data.

2) Set A0 and A1 (Channel Select) to logic "0" (Channel A) for a minimum of 300 ns before transferring valid data.

3) Set $\overline{HBE}/\overline{LBE}$ to logic "0" (3-state enables) for a minimum of 50 ns before transferring valid data.

4) Transfer Channel "A" data.

5) Set A0 (Channel Select) to logic "1" (Channel B) for a minimum of 300 ns before transferring valid data.

6) Transfer Channel "B" data.

7) Set A0 to logic "0", A1 to logic "1" (Channel C) for a minimum of 300 ns before transferring valid data.

8) Transfer Channel "C" data.

9) Return $\overline{HBE}$/$\overline{LBE}$ to logic "1" at least 50 ns before the next device is put on the data bus.

10) Return $\overline{INH}$ to logic "1" no earlier than 0 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 2.0 μs to allow update of fresh accurate output data.

Notes:

- $\overline{INH}$ (inhibit) and A0, A1 (Channel Select) input function are independent from $\overline{HBE}$ and $\overline{LBE}$ (3-state) inputs.
- Converter "Channel Selection" (A, B, or C) can be done in any sequence.

Two-Byte Data Transfer on 8-Bit Data Bus

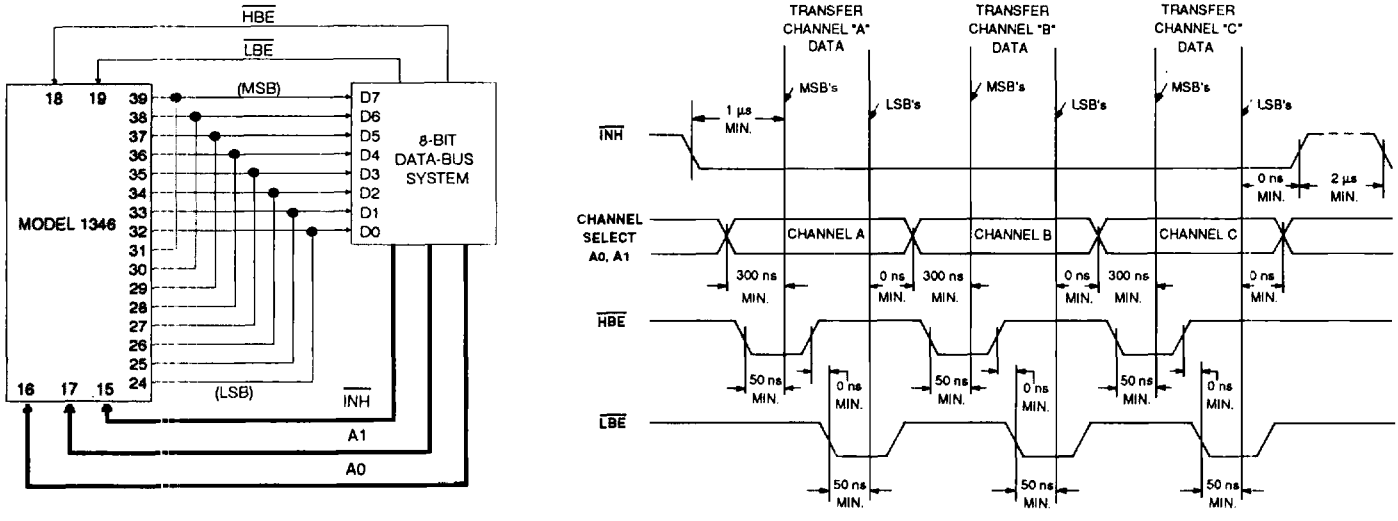


FIGURE 11 Digital Connections and Timing for Two-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from **Model 1346** to an 8-bit 3-state data-bus system is shown in Figure 11. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 1 μs before transferring valid data.

2) Set A0 and A1 (Channel Select) to logic "0" (Channel A) for a minimum of 300 ns before transferring valid data.

3) Set $\overline{HBE}$ (high-byte-enable) to logic "0" for a minimum of 50 ns before transferring valid data (MSB's).

4) Transfer MSB's.

5) Return $\overline{HBE}$ to logic "1".

6) Set $\overline{LBE}$ (low-byte-enable) to logic "0" for a minimum of 50 ns before transferring valid data (LSB's).

7) Transfer LSB's.

8) Return $\overline{LBE}$ to logic "1".

9 Set A0 to logic "1" (Channel B) for a minimum of 300 ns before transferring valid data.

10) Repeat steps 3 through 8.

11) Set A0 to logic "0" and A1 to logic "1" (Channel C) for a minimum of 300 ns before transferring valid data.

12) Repeat steps 3 through 8.

13) Return $\overline{INH}$ to logic "1" no earlier than 0 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 2.0 μs to allow update of fresh accurate output data.

Notes:

- $\overline{HBE}$ and $\overline{LBE}$ data bytes can be transferred in any sequence ($\overline{HBE}$ or $\overline{LBE}$ first). The timing requirements are the same for both $\overline{HBE}$ and $\overline{LBE}$ data byte enables.
- $\overline{INH}$ (inhibit) and A0/A1 (channel select) input functions are independent from $\overline{HBE}$ and $\overline{LBE}$ (3-state) inputs.
- Converter "Channel Selection" (A, B or C) can be done in any sequence.

HRD1346 incorporates a high gain, Type II, servo loop to provide accurate real-time Resolver-to-Digital conversion. Each converter channel is characterized for the following dynamic input angle conditions:

(1) Static Input Angle

(2) Constant Rate of Change of Input Angle Position (Constant Velocity)

(3) Constant Rate of Change of Input Angular Velocity (Constant Acceleration)

(4) Variable Rate of Change of Angular Velocity (Sinusoidal Modulation)

(5) Infinite Rate of Change of Angular Velocity (Step Input)

The **1346** accuracy specification applies for **Static (1)** and **Constant Velocity (2)** input conditions, as long as the maximum converter tracking rate is not exceeded.

For **Constant Acceleration (3)** of input angle, the digital output will lag the input by the following amount:

$$\text{Acceleration Lag (error)} = \frac{\text{Input Angle Acceleration}}{K_A}$$

The values of maximum tracking rate and acceleration constant (K_A) for different frequency options are given in the specification table (page 8). Note that the specified K_A is typical and is not a tightly-controlled parameter (converter K_A is analogous to the open-loop gain of an operational amplifier).

For **Sinusoidal Shaft Angle Modulation (4)**, the digital angle output will lag the input by the following amount:

$$\text{Sinusoidal lag (error p-p)} = \frac{2 \times \pi^2 \times \text{Amp (p-p)} \times Fo^2}{K_A}$$

Where: Amp (p-p) = peak-peak angle modulation level
Fo = modulation frequency (Hz)
K_A = converter acceleration constant

The Peak Rate (Velocity) for a given sinusoidal modulation is:

$$\text{Rate (degrees/sec)} = \pi \times \text{Amp (degrees p-p)} \times Fo\ (Hz)$$

For **Step Inputs (5)**, the digital angle output will respond as a function of the converter's Large Signal and Small Signal transient response.

The **Large Signal** transient response is dependent solely on the maximum velocity (ω_{max}) and the maximum acceleration (α_{max}) of which the converter is capable. The large signal parameters are defined in Figure 12. The synchronizing time (t_{sync}) for large signals can be partitioned into three distinct intervals. Acceleration time (t_{ACC}), Slew time (t_{SLEW}) and Overshoot time (t_{OS}).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The **Small Signal** settling time (t_S) is specified for step inputs of less than 1.4 degrees. For small signal steps the settling time is a function of the transient response of the converter.

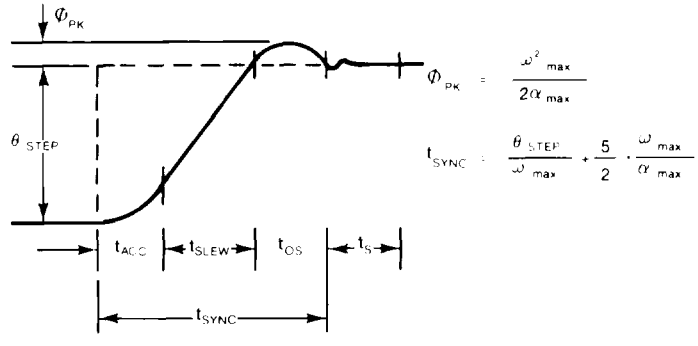


FIGURE 12 Large Signal (≥1.4°) Response Parameters

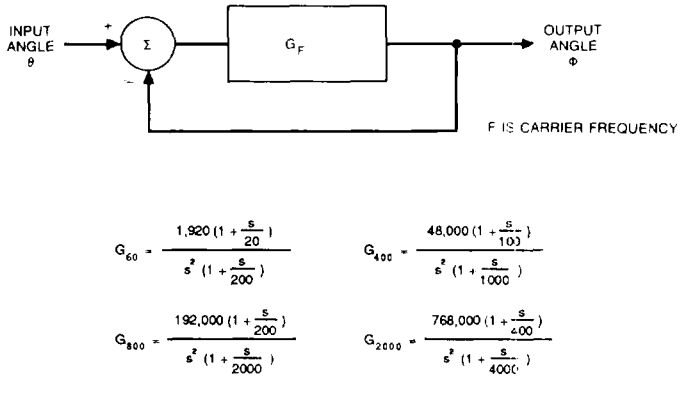


FIGURE 13 Transfer Functions for 1346

Transfer Function

The basic control loop model and transfer functions for 60 Hz, 400 Hz, 800 Hz and 2000 Hz models are shown in Figure 13. A more detailed model with corresponding transfer functions for both position and velocity output is shown in Figure 15. Typical values for transfer function parameters for different frequency options are shown in the table of Figure 14.

Transfer function parameters are determined by the specified frequency option of the converter. When a converter is operated at a frequency higher than that specified, these parameters remain the same. For some applications it may be advantageous to use a lower bandwidth converter operating at a higher carrier frequency.

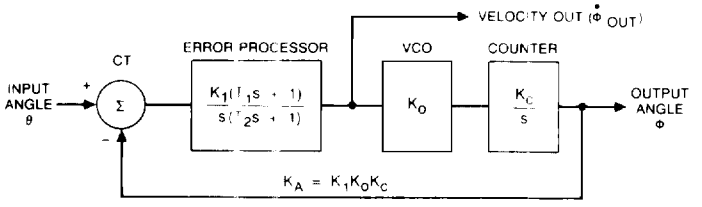
For example, to improve the position noise rejection, velocity output noise/ripple and velocity linearity, a 60 Hz frequency (option 6) could be used and operated at higher carrier frequencies such as 400 Hz.

For a better understanding of the dynamics of the **1346**, bode plots for converter gain and output phase for 60 Hz, 400 Hz, 800 Hz and 2000 Hz options are shown in Figures 17 and 18.

Results of actual performance of step responses for both large and small signal inputs performed on typical converters are shown in Figure 16.

PARAMETERS	UNITS	FREQUENCY OPTION			
		60 Hz	400 Hz	800 Hz	2000 Hz
K_A	sec^{-2}	1,920	48,000	192,000	768,000
K_O	$\frac{Counts}{Volt\text{-}Sec}$	29,800	149,000	218,000	218,000
K_C	$\frac{Radians}{Count}$	9.587×10^{-5}	9.587×10^{-5}	9.587×10^{-5}	9.587×10^{-5}
K_1	$\frac{Volts}{Radian\text{-}Sec}$	672	3360	9187	36747
T_1	ms	50.0	10.0	5.0	2.5
T_2	ms	5.0	1.0	0.5	0.25
K_OK_C	$\frac{Radians}{Volt\text{-}Sec}$	2.857	14.28	20.90	20.90

FIGURE 14 Transfer Function Parameters (Typical Values)



POSITION GAIN (OPEN LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{K_A(T_1s+1)}{s^2(T_2s+1)}$

VELOCITY GAIN (OPEN LOOP) $\frac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \frac{K_1(T_1s+1)}{s(T_2s+1)}$

POSITION GAIN (CLOSED LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{T_1s+1}{\frac{T_2s^3}{K_A} + \frac{s^2}{K_A} + T_1s + 1}$

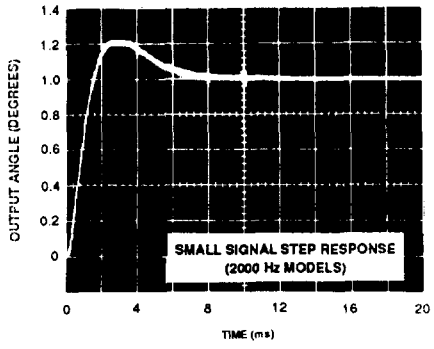
VELOCITY GAIN (CLOSED LOOP) $\frac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \frac{T_1s^2+s}{\frac{T_2s^3}{K_1} + \frac{s^2}{K_1} + T_1K_OK_Cs + K_OK_C}$

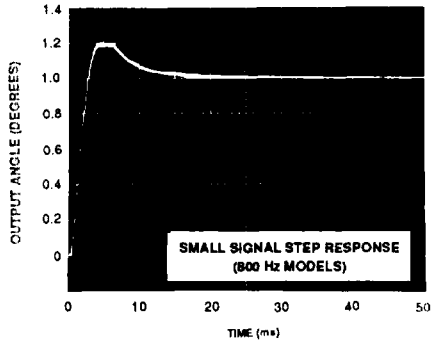
FIGURE 15 Detailed Transfer Function Model

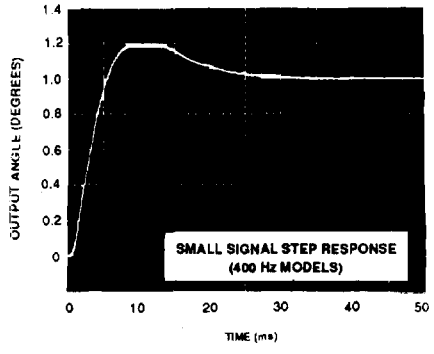
Step Response

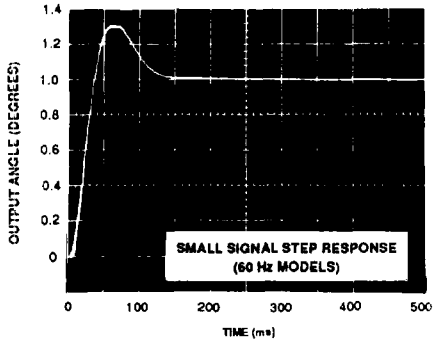
V_L = +5 V-dc, T_a = 25°C

Small Signal Input Step = 1.0 Degrees

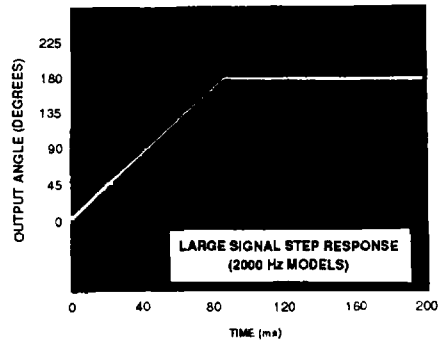


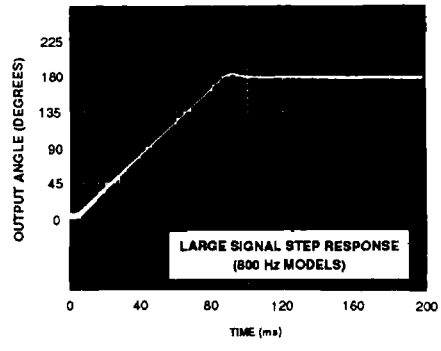


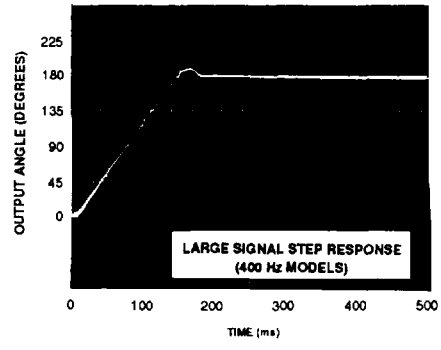




Large Signal Input Step = 179 Degrees







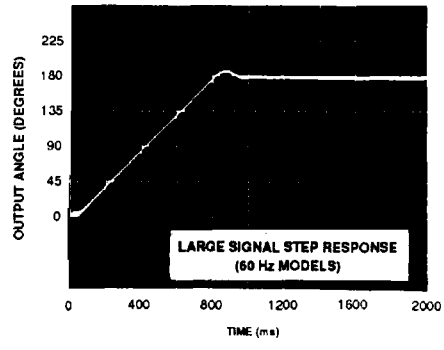


FIGURE 16 Small and Large Signal Step Response

Bode Plots

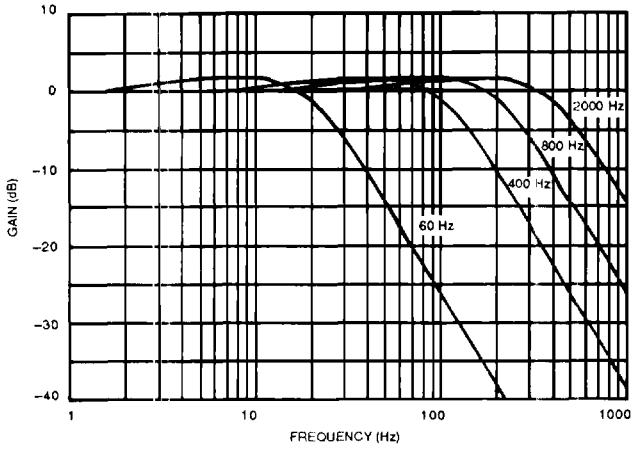


FIGURE 17 Gain Plot

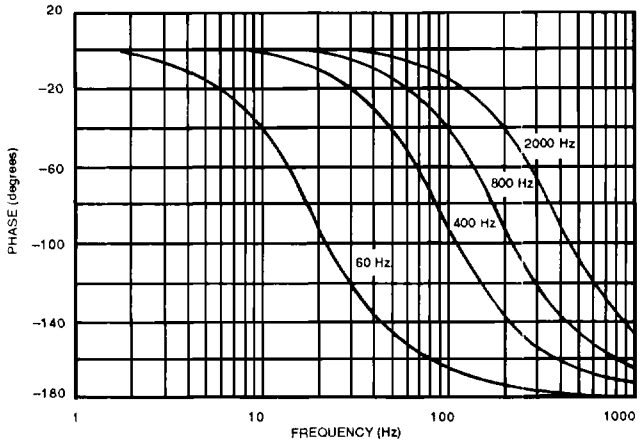


FIGURE 18 Phase Plot

Velocity Outputs

As a by-product of the conversion process, the **Model 1346** produces analog velocity signals. These analog signals have proven useful in various applications and are therefore brought out. The absolute value of these analog outputs is not critical to the overall conversion process. Therefore, unless otherwise specified, they are not closely controlled or characterized functions. These outputs are:

V (pin 7), Internal analog ground (Bias)

VEL_A (pin 12), velocity output channel A

VEL_B (pin 13), velocity output channel B

VEL_C (pin 14), velocity output channel C

VEL_A, VEL_B, VEL_C is a dc voltage proportional to the velocity of the digital output angle (thereby the input shaft angle). The voltage goes negative for increasing digital angle and goes positive for decreasing digital angle. At maximum tracking velocity, the output voltage is 1.1 volts-dc (1.5 volts-dc for 800 Hz and 2000 Hz models). Detailed specification for velocity functions are provided on page 7. Dynamic characteristics including open loop and closed loop transfer functions are provided on page 13.

"V", internal analog ground, also referred to as the"bias voltage" provides a reference point for all analog functions. The typical value of the bias voltage, V, is:

$$V = 1/2\ (V_L - 0.7\ \text{V-dc})$$

$$= 2.15\ \text{V-dc} \pm 10\%\ (\text{for } V_L = +5\ \text{V-dc})$$

All analog outputs have a minimum output drive of ±1 mA with respect to V (bias). For a power supply of +5 V-dc, the minimum output swing is ±1.1 V peak (±1.5 V peak for 800 Hz and 2000 Hz models) with respect to V (bias).

If a bipolar signal, with respect to power supply ground, is required for any analog output, a difference circuit, as shown in Figure 19, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed.

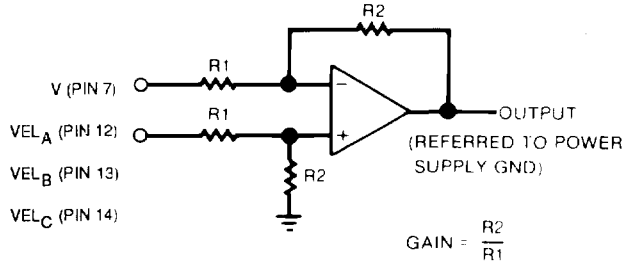
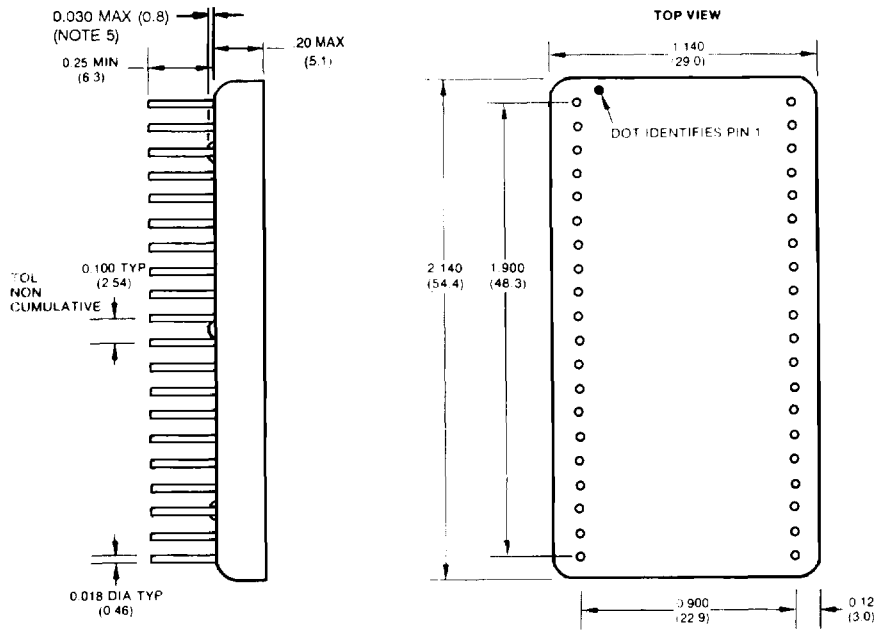


FIGURE 19 Difference Circuit for Bipolar Analog Outputs



TOLERANCES:
.XX = ±.01 (±.25)
.XXX = ±.005 (±.13)

NOTES:
1. CASE IS ELECTRICALLY FLOATING.
2. PINS ARE KOVAR WITH GOLD PLATING. (50 μINCH MIN.)
3. PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING.
4. DIMENSIONS SHOWN IN INCHES AND (MM).
5. STANDOFFS (3) CERAMIC OR GLASS.

MECHANICAL OUTLINE

Ordering Information

HRD1346 – T F I A

Temperature Range

1 = 0°C to + 70°C
2 = −25°C to + 85°C
3 = −55°C to + 125°C

Frequency (bandwidth)

2 = 200C Hz (400 Hz BW)
4 = 40C Hz (100 Hz BW)
6 = 6C Hz (20 Hz BW)
8 = 80C Hz (200 Hz BW)

Accuracy

S = ±5.2 arc-minutes
H = ±2.6 arc-minutes
V = ±1.3 arc-minutes

Input Signal/Reference

0 = 0.5 V-rms*/ 1 – 10 V-rms
1 = 11.8 V-rms / 4 – 35 V-rms
2 = 26 V-rms / 4 – 35 V-rms
3 = 1.0 V-rms / 1 – 10 V-rms
4 = 2.0 V-rms / 1 – 10 V-rms
5 = 0.5 V-rms*/ 0.5 V-rms*
6 = 3.0 V-rms / 1 – 10 V-rms
7 = 5.0 V-rms / 1 – 10 V-rms
8 = 7.0 V-rms / 1 – 10 V-rms
9 = 90.0 V-rms / 20 – 130 V-rms

*Direct (Buffered Input)

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- **3 arc-second accurate**, Programmable Dynamic Angle Simulator that includes 4 Related Instruments and is totally A.T.E. Programmable (L200).
- Hybrid (36-pin DDIP size) Synchro (Resolver)-to-Digital converters that operate from a **single +5V power supply** and offer excellent features such as BIT, AGC, low power dissipation and more (Models 1006, 1056, 1046 and 1044).
- 1.3 arc-minute accuracy, high power, Digital-to-Synchro converters that **do not require any DC power supplies** (Models 5031 and 5131).
- Second generation Four Quadrant Multiplying Sin/Cos DAC (HDSC2026).
- **2-channel** Digital-to-Sin/Cos Converter in a single 36-pin hybrid (HDSC2036).
- **2 -Speed, Single hybrid**, 22-Bit, microprocessor compatible, 0.0004 degree accuracy Synchro (Resolver)-to-Digital Converter that operates from a **single +5V power supply** (Model 1626).

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