

The documentation and process conversion measures necessary to comply with this revision shall be completed by 7 March 2012.

INCH-POUND

MIL-PRF-19500/708A  
7 December 2011  
SUPERSEDING  
MIL-PRF-19500/708  
1 April 2003

\* PERFORMANCE SPECIFICATION SHEET

DISPLAYS, DIODE, LIGHT EMITTING, SOLID STATE, RED, NUMERIC AND HEXADECIMAL, WITH ON BOARD DECODER/DRIVER TYPES 4N51, 4N52, 4N53, AND 4N54, JAN AND JANTX

This specification is approved for use by all Departments and Agencies of the Department of Defense.

- \* The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for hermetically sealed red numeric and hexadecimal light emitting diode, 4 X 7 dot matrix array displays. Two levels of product assurance are provided as specified in [MIL-PRF-19500](#).

- \* 1.2 Part identification number. The part identification number scheme is as follows:

JANQQ	XN	YY	X	X
JAN brand and quality level (see 1.3.1 of <a href="#">MIL-PRF-19500</a> )	Component designation (see 1.3.5 of <a href="#">MIL-PRF-19500</a> )	Identification number (see 1.3.6 of <a href="#">MIL-PRF-19500</a> )	Lead finish (see 1.2.4)	Luminous intensity code (see 1.2.5)

1.2.1 Device type. Device types are as follows:

<u>Device type</u>	<u>Function</u>
4N51	Numeric indicator "0-9", a "-" sign, test pattern, and right hand decimal point.
4N52	Numeric indicator "0-9", a "-" sign, test pattern, and left hand decimal point.
4N53	Numeric indicator "±1" overrange display with right hand decimal point.
4N54	Hexadecimal indicator "0-9" and "A-F".

1.2.2 Device quality level. The device quality levels are JAN and JANTX as defined in [MIL-PRF-19500](#).

1.2.3 Government certification mark. The certification mark JAN or the abbreviated prefix J indicates a performance specification item produced in full compliance with [MIL-PRF-19500](#) and herein.

\* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.daps.dla.mil/>.

\* 1.2.4 Lead finish. The lead finishes are as specified in 3.5. The lead finishes are designated by a single letter as follows:

<u>Finish letter</u>	<u>Lead finish</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate

NOTE: Finish letters are not be marked on the display or its packaging. This designation is provided for use in drawings, part lists, orders, or other documentation where lead finishes A, B, or C are all considered acceptable and interchangeable without preference.

\* 1.2.5 Luminous intensity code. Luminous intensity codes are as follows:

Luminous intensity code	Minimum luminous intensity (1)	Maximum luminous intensity (1)
	μcd	μcd
C	44	79
D	59	106
E	79	142
F	106	190
G	142	255
H	190	342
I	257	462
J	343	617
K	457	820
X	(2)	(2)

- (1) Test conditions are as specified in table I, subgroup 7.
- (2) The luminous intensity code "X" is not to be marked on the display or its packaging. This designation is provided for use in drawings, parts lists, orders, and other documentation. Where a luminous intensity code is required, it will be specified in the contract or order. (Due to the overlapping of the luminous intensity codes, it is recommended that the two adjacent categories be specified).

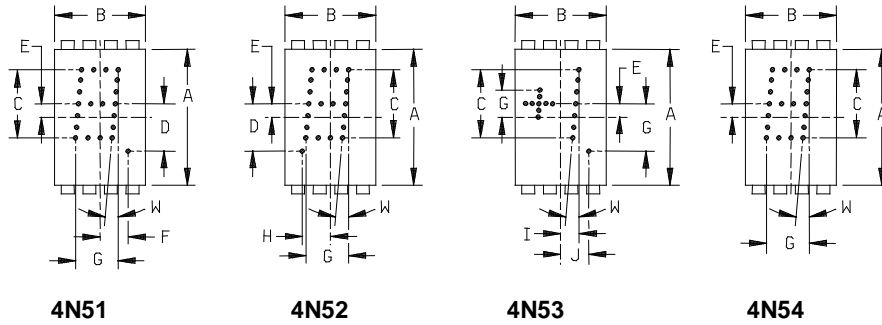
1.3 Physical dimensions. See figure 1.

1.4 Absolute maximum ratings.

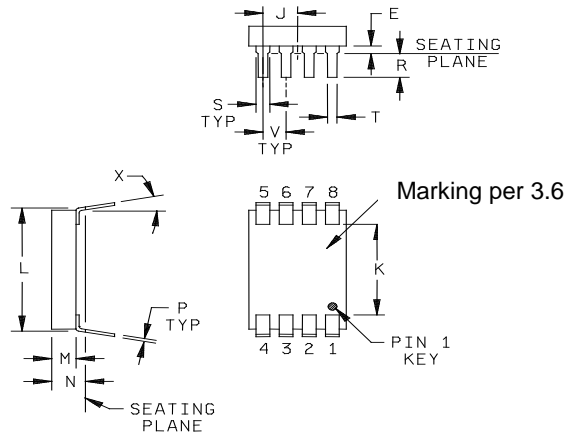
- Maximum total power dissipation
  - 4N51, 4N52, and 4N54 1/----- 935 mW.
  - 4N53 2/ ----- 320 mW.
- Logic supply voltage (V<sub>CC</sub>) 3/----- 7.0 V dc.
- Voltage applied to input logic pins ----- 7.0 V dc.
- Voltage applied to blanking input
  - 4N54----- V<sub>CC</sub>.
- Maximum solder temperature 4/----- 260°C.
- Operating temperature range 5/ ----- -55°C to +100°C.
- Ambient storage temperature ----- -65°C to +125°C.

1/ V<sub>CC</sub> = 5.5 V dc (numeral 5 lighted for all types. Decimal point lighted on 4N51 and 4N52).  
 2/ I<sub>F</sub> = 10 mA dc for each LED. (Current limiting resistors will be used.)  
 3/ Voltage greater than V<sub>CC</sub> or lower than -0.5 V dc shall not be applied to any input as the excessive voltage may damage the on-board integrated circuit. Recommended voltage is 4.5 to 5.5 V dc.  
 4/ t ≤ 5 seconds at .062 inch (1.57 mm) below seating plane.  
 5/ R<sub>ΘCA</sub> = 35°C/W maximum.

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.515	.545	13.08	13.84
B		.400		10.20
C	.275	.305	6.99	7.75
D	.205	.235	5.21	5.97
E	.045	.075	1.14	1.91
F	.105	.135	2.67	3.43
G	.175	.205	4.45	5.18
H	.125	.155	3.18	3.94
I	.060	.090	1.52	2.29
J	.135	.165	3.43	4.20
K	.385	.415	9.78	10.54
L	.585	.615	14.86	15.62
M	.095	.125	2.41	3.18
N	.155	.185	3.94	4.70
P	.009	.015	.23	.38
R	.120	.150	3.05	3.81
S	.035	.065	.89	1.65
T	.017	.023	.43	.58
V	.095	.105	2.41	2.67
W	4°	6°	4°	6°
X	0°	10°	0°	10°



Notes:

1. Dimensions are in inches.
- \* 2. Millimeters are given for general information only.

\* FIGURE 1 Physical dimensions.

1.5 Recommended operating conditions.

Enable pulse width <u>6/</u> - - - - -	100 ns minimum.
Set up time <u>6/ 7/</u> - - - - -	50 ns minimum.
Hold time <u>6/ 8/</u> - - - - -	50 ns minimum.
Enable pulse rise time <u>6/</u> - - - - -	200 ns maximum.

2. APPLICABLE DOCUMENTS

\* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

\* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

\* DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

\* DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

\* (Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or <https://assist.daps.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

\* 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

6/ See [figure 2](#) for timing diagrams of series logic.

7/ Minimum set-up time is the interval immediately preceding the positive going transition of the enable input, during which interval the data to be displayed will be maintained at the latch data inputs, to ensure its recognition.

8/ Minimum hold time is the interval immediately following the positive going transition of the enable input, during which interval the data to be displayed will be maintained at the latch data inputs, to ensure its continued recognition.

### 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

$I_{BH}$	Blanking input current "1" state.
$I_{BL}$	Blanking input current "0" state.
$I_{EH}$	Enable high level input current.
$I_{EL}$	Enable low level input current.
$I_{IH}$	Logic data input current "1" state.
$I_{IL}$	Logic data input current "0" state.
$t_{hold}$	Time data will be held after positive transition of enable input.
$t_{setup}$	Time data will be held before positive transition of enable input.
$t_{TLH}$	Enable input pulse rise time.
$V_B$	Voltage applied to blanking input.
$V_{BH}$	Blanking high voltage; display blanked.
$V_{BL}$	Blanking low voltage; display not blanked.
$V_{DP}$	Voltage applied to decimal point.
$V_E$	Voltage applied to enable input.
$V_{EH}$	Enable input high voltage; data not being entered.
$V_{EL}$	Enable input low voltage; data being entered.
$V_I$	Voltage applied to input logic.
$V_{IH}$	Logic data input voltage "1" state.
$V_{IL}$	Logic data input voltage "0" state.

$$\eta_v \quad \text{Luminous efficacy} \quad \frac{\text{luminous power}}{\text{radiant power}} = \text{Lumens/Watt.}$$

$\lambda_{PEAK}$  Peak wavelength.

$\lambda_d$  Dominant wavelength.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figure 1](#). Eutectic or epoxy die bonding may be used. When epoxy die bonding is used, the material, cure cycle, and other pertinent data shall be approved by the qualifying activity.

3.4.1 Terminal connections. The terminal connections and functions shall be as specified on [figures 1](#) and [2](#).

3.4.2 Truth tables. The truth tables and resultant displays of the binary data in the latches shall be as specified on [figure 2](#).

\* 3.5 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2). The lead finishes are designated by a single letter as follows:

<u>Finish letter</u>	<u>Lead finish</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate

NOTE: Finish letters are not to be marked on the display or its packaging. This designation is provided for use in drawings, part lists, orders, or other documentation where lead finishes A, B, or C are all considered acceptable and interchangeable without preference.

3.6 Marking. Marking shall be in accordance with MIL-PRF-19500 and as specified herein. At the option of the manufacturer, the marking may be on more than one line as shown by the following example:

JANTX4N51  
XX

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.4, 1.5, and table I herein.

3.8 Electrical test requirements. The electrical test requirements shall be table I, group A as specified herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

#### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.5).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and 4.4 herein.

4.2.1 Off-axis luminous intensity. Off-axis luminous intensity at 40 degrees from the normal shall be measured in accordance with 4.5.4. Two samples shall be required and the minimum acceptable value of off-axis luminous intensity shall be 50 percent of the on-axis luminous intensity.

4.2.2 Dimming range capability. This test shall demonstrate dimming range capability. Two samples shall be required and the dimming range shall be 1,000:1. Dimming range shall be measured in accordance with 4.5.6.

4.2.3 Display color and color uniformity. The purpose of this test is to determine that the color of the display falls visually within the required color range. Two displays shall be measured in accordance with 4.5.7 to determine dominant wavelength. Measurements shall fall between 625 and 660 nanometers for acceptable units.

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4.3 Screening (JANTX only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Conditions
1B	See 4.3.1.
2	Not required.
3A	Condition B (10 cycles) Dwell = $\geq 10$ minutes. Transfer time $\leq 5$ minutes.
4	10,000 G Y1, for 1 minute, minimum.
7A	Test condition G or H maximum leak rate = $5 \times 10^{-8}$ atm cm <sup>3</sup> /s.
7B	Test condition A, C, E, or F.
9	Subgroups 1 and 7 of table 1 herein.
10A	160 hours at T <sub>A</sub> = 100°C. See 4.3.2 and figure 3.
11	Subgroups 1 and 7 of table I herein.
13	$\Delta I_V = -20$ percent of group A value; $\Delta I_{IH1} = \pm 10$ $\mu$ A dc. $\Delta I_{CC1} = \pm 10$ mA dc; $\Delta I_{EH1} = \pm 13$ $\mu$ A dc.
16	External visual.

4.3.1 Internal visual (precap) inspection. Internal visual (precap) inspection shall be in accordance with method 2072 of MIL-STD-750, except crack rejection criteria shall be as follows:

- a. Any crack which extends into an active region or through a guard ring.
- b. Any crack that exceeds 1.0 mils in length inside the scribe grid or scribe line that points toward operating metallization or functional elements.
- c. Any crack that exceeds 5.0 mils in length.

4.3.2 Burn-in. The burn-in test circuits shall be as specified on figure 3. All displays shall be cooled in accordance with 4.5.1.

4.3.3 Visual and mechanical inspection. Displays shall be examined under a magnification between 3X and 10X with a field of view sufficiently large to contain the entire display. Displays that exhibit any of the following criteria shall be rejected:

- a. Lead identification, markings (content, placement, and legibility), materials, construction, and workmanship not in accordance with MIL-PRF-19500.
- b. Defects or damage resulting from manufacturing, handling, or testing.

- c. Visible evidence of corrosion, contamination or breakage (grossly bent or broken leads, cracked seals except for glass meniscus), and peeled, flaked, or blistered plating. (Discoloration of the finish shall not be cause for failure unless there is evidence of flaking, pitting, or corrosion).
- d. Leads that are not intact and aligned in their normal location, free of sharp or unspecified lead bends, and for ribbon leads, free of twist outside the normal lead plane.
- e. Leads that are not free of foreign material such as paint or other adherent deposits, or dust.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be subjected to and pass the requirements of group A1 and A2 inspection only (table E-VIB, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB of MIL-PRF-19500. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2. Delta requirements only apply to subgroups B3, B4, and B5. Electrical measurements (end-points) and delta requirements shall be after each step in 4.4.2.1 and shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B sample selection. Samples selected from group B inspection shall be chosen from an inspection lot that has been subjected to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and 4.4.3.1 herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2; delta requirements only apply to subgroup C6 (steady-state operation life testing). Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 herein; delta requirements only apply to subgroup C6.

4.4.3.1 Group C inspection, table E-VII (JANTX) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Condition</u>
C2	Omit thermal shock and terminal strength. Moisture resistance in accordance with 4.5.3.
C7	Not applicable.

4.4.3.2 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is subjected to and passes group A tests for conformance inspection. Testing of a subgroup using a single device type shall be considered as complying with the requirements for that subgroup.

4.4.4 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-PRF-19500.



4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Life test and burn-in cool down procedure. The displays shall be cooled to room temperature prior to the removal of bias. The interruption of bias for up to 1 minute for the purpose of moving the displays to cool down positions separate from the chamber within which life testing or burn-in was performed shall not be considered removal of bias. Alternately, the bias may be removed during cooling provided the case temperature of displays under test is reduced to a maximum of 35°C within 30 minutes after the removal of the test conditions.

4.5.2 Lead integrity. Each lead of each test display shall be bent inward through an angle sufficient to cause the lead to retain a permanent bend (after stress removal) of at least 15 degrees measured at the lead extremities. At the completion of the initial bend, the leads shall be returned to their approximate original position. This procedure shall be repeated for a total of three complete bends.

4.5.2.1 Failure criteria. After removal of the stress, any evidence of breakage, loosening, or relative motion between the lead (terminal) and the display body shall be considered a failure. Meniscus cracks shall not be cause for rejection.

4.5.3 Moisture resistance. Moisture resistance shall be conducted in accordance with method 1021 of MIL-STD-750. Initial conditioning shall be in accordance with 4.5.2 herein except that only one bend shall be required.

4.5.4 Axial luminous intensity.

4.5.4.1 Apparatus. The equipment for this measurement shall consist of a photo-meter designed to respond to incident luminous flux density. The output of the photo-meter shall be linearly related to luminous incidence over the range of levels encountered in calibration and measurement. The output may be a voltage or a current or may be rendered directly in the units of luminous incidence.

4.5.4.1.2 Spectral response. The relative response of the photometer shall be within  $\pm 6$  percent of the photopic luminous efficacy for all wavelengths within the spectrum of the device to be measured.

4.5.4.1.3 Receptance pattern. The off-axis receptance of the photometer shall be constant over a large enough angle so that it responds equally to light from all parts of the display to be measured. An effective plane of receptance (image of the detecting surface) shall be defined with respect to which the calibration can be performed.

4.5.4.2 Calibration of photometer (see figure 4). The photometer shall be calibrated with a National Institute of Standards and Technology (NIST) Detector Response Transfer Intercomparison Package (DRIP), an OSRAM FCR 6333 100W, 12V, 3300°K quartz tungsten halogen incandescent lamp or equivalent, and Omega Optical full blocking 10 nanometer bandwidth interference filters or equivalent. Peak transmission wavelengths shall be centered within the 550 nm to 730 nm range. The correlation factors derived by comparing the response of the photometer with the calculated photometric response of the NIST DRIP unit shall be used as the photometer calibration.

4.5.4.2.1 Calibration procedure. The equipment shall be mounted on an optical bench and a photo detector reference plane established. A baffle box shall be used to collimate the light and support the interference filters. The exit aperture shall be placed as close to the photo detectors as possible and shall form a spot of light of known area ( $A_0$ ) that underfills the active areas of the photometer and DRIP unit photo detectors. The distance between the quartz lamp filament and the reference plane shall be within 31.4 inch (800 mm) and 35.4 inch (900 mm).

4.5.4.2.2 Equipment calibration measurements and calculation. The quartz lamp shall be illuminated and one hour shall be allowed for stabilization. The photocurrent output in amperes of the NIST DRIP unit and the luminous incidence by the photometer in lumens per square meter shall be measured at the reference plane for each interference filter used. From the responsivity table supplied with the NIST DRIP unit, the DRIP responsivity at the peak wavelength shall be determined for each interference filter used. The radiometric incidence of the NIST DRIP unit at the peak wavelength of each interference filter shall be calculated as follows:

$$E_{e_o}(\lambda_p) = \frac{I_{p_o}(\lambda_p)}{A_o R_o(\lambda_p)}$$

where  $E_{e_o}(\lambda_p)$  = Radiometric incidence in watts/m<sup>2</sup> at peak wavelength of interference filter.

$I_{p_o}$  = Photocurrent in amperes at peak wavelength of interference filter.

$A_o$  = Illuminated active area of the detectors used during calibration, (m<sup>2</sup>).

$R_o$  = Responsivity in amperes per watt of the NIST DRIP unit at the peak wavelength of the specified interference filter.

Luminous efficacy in lumens per watt for each interference filter used shall be calculated as follows using 1 nanometer intervals across the filter transmission spectrum:

$$\eta_v = \frac{683 \int T_{FILTER}(\lambda) \bar{y}(\lambda) d\lambda}{\int T_{FILTER}(\lambda) d\lambda}$$

where  $\eta_v$  = luminous efficacy in lumens/watt.

$T(\lambda)$  = relative spectral transmission of an interference filter.

$\bar{y}(\lambda)$  = 1931 luminosity function (CIE photopic curve).

The photometer correlation factor at the peak wavelength for each interference filter shall be calculated as follows:

$$K(\lambda_p) = \frac{E_v(\lambda_p - \text{measured})}{E_{e_o}(\lambda_p) \eta_v}$$

where  $K(\lambda_p)$  = photometer correlation factor at the peak wavelength for each interference filter.

$E_v(\lambda_p - \text{measured})$  = measured luminous incidence by the photometer in lumens / m<sup>2</sup>.

$E_{e_o}(\lambda_p) \eta_v$  = calculated photometric response of the NIST DRIP unit.

The values of  $K(\lambda_p)$  vs  $\lambda_p$  shall be plotted graphically and the correlation value for 655 nanometers ( $K_{655}$ ) shall be determined.

4.5.4.3 Operation of photometer. The photometer shall be adjusted to measure on axis light output as luminous intensity in candelas. The correct value for luminous intensity shall be calculated by using the following equation:

$$I_v = \frac{1}{K_{655}} * \text{Photometer reading}$$

where  $I_v$  = corrected value of photometer output in candelas.

$K_{655}$  = photometer correlation factor at 655 nanometers.

4.5.5 Luminous intensity off-axis (see figure 5). The display shall be rotated relative to the photometer detector head or the position and angle of the detector head can be varied provided that the distance from the display digit remains constant. The character "8" shall be illuminated on 4N51, 4N52, and 4N54. The character "+1" shall be illuminated on 4N53. Measurement of luminous intensity ( $I_{v\theta}$ ) at the specified angle  $\theta$  from the normal axis shall be made from four directions X', X", Y', and Y" as shown on figure 5.

4.5.6 Dimming range. Dimming range capability shall be determined by first measuring the on-axis luminous intensity of the display under test while the display is being driven at the standard dc drive conditions. The display shall then be dimmed by the appropriate pulse width modulation (see 4.5.6.1), and the luminous intensity of the display shall again be measured. The dimming range shall be determined by the ratio of on-axis luminous intensity at normal drive conditions to the on-axis luminous intensity at pulse width modulated drive conditions.

4.5.6.1 Pulse width modulation procedure. Display dimming shall be accomplished by pulse width modulation using the waveform shown on figure 6. The display under test is blanked when the pulse modulated voltage  $V_{PWM}$  is less than 0.8 V and is turned on when the pulse modulated voltage is greater than 3.5 V. Dimming circuitry for displays covered by this specification shall be as indicated on figure 7. Duty factor period time shall be equal to 10 milliseconds and the display 'on time' shall be adjusted to achieve the dimming range specified in 4.5.6. The displayed character shall be legible in a dark environment over the dimming range specified in 4.5.6.

4.5.7 Display color, dominant wavelength.

4.5.7.1 Apparatus. A spectroradiometer, designed to measure the spectral distribution of light sources, shall be used to measure the spectral distribution of the display under test. The spectroradiometer shall have a spectral bandwidth of 5 nanometers or less, a sensitivity of  $2.4 \times 10^{-9}$  watts/steradian per nanometer at 655 nanometers and a flat relative response within  $\pm 5$  percent from 550 to 730 nanometers.

4.5.7.2 Calibration. Calibration of the spectroradiometer shall be accomplished by using a light source of known spectral output and dividing the reading of the spectroradiometer at each wavelength by the output of the light source at that wave-length. By generating a table of weighting factors at each wavelength of the spectroradiometer, a uniform reading at all wavelengths for a light source of uniform output may be obtained by multiplying the reading of the spectroradiometer at each wavelength by the appropriate weighting factor.

4.5.7.3 Procedure. The LED display to be measured shall be mounted perpendicular to the entrance aperture of the spectroradiometer at a distance such that the flux emitted by all of the light emitting diodes is detected. The display shall be spectrally scanned between the wavelengths of 550 to 730 nanometers and the resulting spectrum normalized to 1.00 at the peak wavelength. The 1931 CIE X, Y color coordinates may be derived by first integrating the normalized LED display spectrum to obtain the two tristimulus values X, Y and then calculating the 1931 chromaticity coordinates as follows:

$$X = \int_{550}^{740} f(\lambda) \bar{x}_{\lambda} d_{\lambda}$$

$$Y = \int_{550}^{740} f(\lambda) \bar{y}_{\lambda} d_{\lambda}$$

where  $\bar{x}_{\lambda}$  and  $\bar{y}_{\lambda}$  are the 1931 CIE color matching functions and  $f_{\lambda}$  is the normalized radiated spectrum.

The integration shall be performed at a maximum of 5 nanometer intervals to determine color coordinates. The 1,931 chromaticity coordinates for light emitting diodes may be calculated directly from the values of X and Y as determined above, using the following relationships:

$$X = \frac{X}{X+Y} ; Y = \frac{Y}{X+Y}$$

4.5.7.4 Derivation of dominant wavelength. The dominant wavelength may be derived within an accuracy of  $\pm 1/2$  nanometer by plotting the X, Y chromaticity coordinates on the 1931 CIE Chromaticity Diagram and by drawing a line from the CIE Illuminant C point (6,500°K color temperature point) through the X, Y color point and intersecting the perimeter of the chromaticity diagram. The point where the line intersects the perimeter is the dominant wavelength.

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TABLE I. Group A inspection.

Inspection	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 1/</u>						
Logic supply current	3005	$V_{CC} = 5.5 \text{ V dc}$ ; (numeral 5 and decimal point lighted)	$I_{CC1}$		160	mA dc
Blanking input current "0" logic level <u>2/</u>		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{BL} = 0.8 \text{ V dc}$	$I_{BL1}$		20	$\mu\text{A dc}$
Blanking input current "1" logic level <u>2/</u>		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{BH} = 4.5 \text{ V dc}$	$I_{BH1}$		0.7	mA dc
Logic current "0" state	3009	$V_{CC} = 5.5 \text{ V dc}$ ; $V_{IL} = 0.4 \text{ V dc}$	$I_{IL1}$		-1.5	mA dc
Logic current "1" state	3010	$V_{CC} = 5.5 \text{ V dc}$ ; $V_{IH} = 2.4 \text{ V dc}$	$I_{IH1}$		50	$\mu\text{A dc}$
Enable current "0" state		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{EL} = 0.4 \text{ V dc}$	$I_{EL1}$		-1.5	mA dc
Enable current "1" state		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{EH} = 2.4 \text{ V dc}$	$I_{EH1}$		55	$\mu\text{A dc}$
<u>Subgroup 2 1/</u>						
		$T_A = 100^\circ\text{C}$				
Logic supply current	3005	$V_{CC} = 5.5 \text{ V dc}$ ; (numeral 5 and decimal point lighted)	$I_{CC2}$		150	mA dc
Blanking input current "0" logic level <u>2/</u>		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{BL} = 0.8 \text{ V dc}$	$I_{BL2}$		50	$\mu\text{A dc}$
Blanking input current "1" logic level <u>2/</u>		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{BH} = 4.5 \text{ V dc}$	$I_{BH2}$		0.6	mA dc
Logic current "0" state	3009	$V_{CC} = 5.5 \text{ V dc}$ ; $V_{IL} = 0.4 \text{ V dc}$	$I_{IL2}$		-1.4	mA dc
Logic current "1" state	3010	$V_{CC} = 5.5 \text{ V dc}$ ; $V_{IH} = 2.4 \text{ V dc}$	$I_{IH2}$		100	$\mu\text{A dc}$
Enable current "0" state		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{EL} = 0.4 \text{ V dc}$	$I_{EL2}$		-1.4	mA dc
Enable current "1" state		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{EH} = 2.4 \text{ V dc}$	$I_{EH2}$		130	$\mu\text{A dc}$
<u>Subgroup 3 1/</u>						
		$T_A = -55^\circ\text{C}$				
Logic supply current <u>2/</u>	3005	$V_{CC} = 5.5 \text{ V dc}$ ; (numeral 5 and decimal point lighted)	$I_{CC3}$		170	mA dc
Blanking input current "0" logic level <u>2/</u>		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{BL} = 0.8 \text{ V dc}$	$I_{BL3}$		20	$\mu\text{A dc}$
Blanking input current "1" logic level <u>2/</u>		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{BH} = 4.5 \text{ V dc}$	$I_{BH3}$		1.0	mA dc
Logic current "0" state	3009	$V_{CC} = 5.5 \text{ V dc}$ ; $V_{IL} = 0.4 \text{ V dc}$	$I_{IL3}$		-1.6	mA dc
Logic current "1" state	3010	$V_{CC} = 5.5 \text{ V dc}$ ; $V_{IH} = 2.4 \text{ V dc}$	$I_{IH3}$		20	$\mu\text{A dc}$
Enable current "0" state		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{EL} = 0.4 \text{ V dc}$	$I_{EL3}$		-1.6	mA dc
Enable current "1" state		$V_{CC} = 5.5 \text{ V dc}$ ; $V_{EH} = 2.4 \text{ V dc}$	$I_{EH3}$		20	$\mu\text{A dc}$
<u>Subgroups 4, 5, and 6</u>						
Not applicable						

See footnotes on next page.

TABLE I. Group A inspection - Continued.

Inspection	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 7</u> Luminous intensity for LED average <u>3/</u>  Functional test in accordance with truth table of figure 2  <u>Subgroup 8</u> External visual	2009	$V_{CC} = 5.0 \text{ V dc}$ 4N51, 4N52 and 4N54, $I_F = 6.0 \text{ mA dc}$ (4N53)  Logic low level = 0.8 V dc(4N51, 4N52 and 4N54) Logic high level = 2.0 V dc (4N51, 4N52 and 4N54), $I_F = 6.0 \text{ mA dc}$ (4N53)	$I_v$	44	820	$\mu\text{cd}$

1/ Does not apply to 4N53.

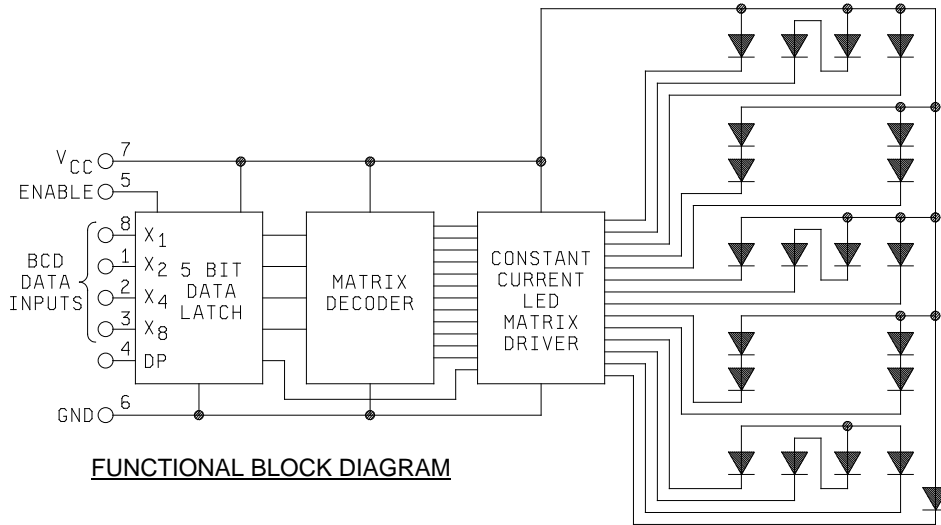
2/ Applies to 4N54 only.

3/ The following characters shall be displayed for the luminous intensity test:

4N51, 4N52 and 4N54 - - character "8".

4N53- - - - - character "+1" and decimal point.

4N51



TERMINAL CONNECTIONS

Pin	4N51
1	Input 2
2	Input 4
3	Input 8
4	Decimal point
5	Latch enable
6	Ground
7	V <sub>CC</sub>
8	Input 1

TRUTH TABLE				
BCD DATA				4N51
X8	X4	X2	X1	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	A
H	L	H	H	Blank
H	H	L	L	Blank
H	H	L	H	
H	H	H	L	Blank
H	H	H	H	Blank
Decimal point				On V <sub>DP</sub> - L
Decimal point				Off DP - H
Enable				Load data V <sub>E</sub> - L
Enable				Latch data V <sub>E</sub> - H

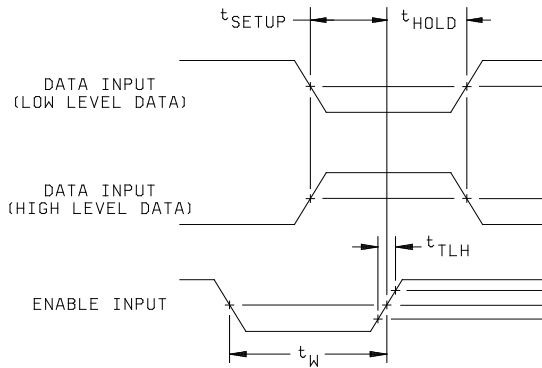
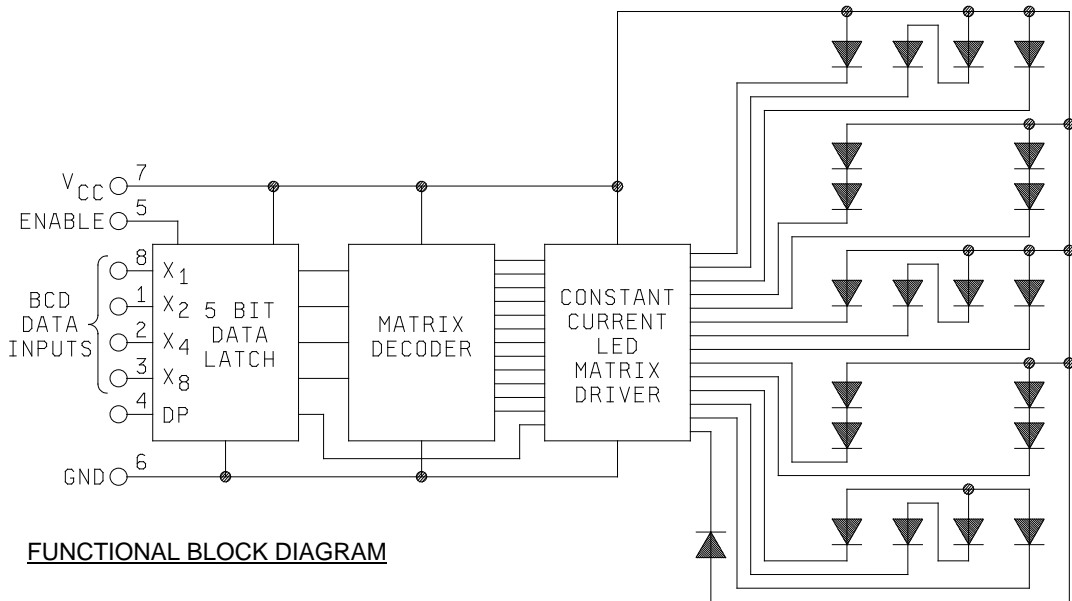


FIGURE 2. Functional block diagrams, terminal connections, timing diagrams, and truth tables.

4N52

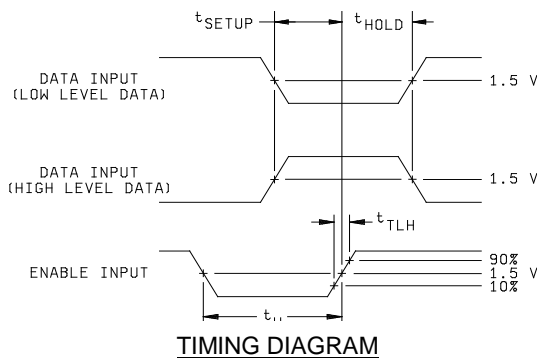


**FUNCTIONAL BLOCK DIAGRAM**

**TERMINAL CONNECTIONS**

Pin	4N52
1	Input 2
2	Input 4
3	Input 8
4	Decimal point
5	Latch enable
6	Ground
7	V <sub>CC</sub>
8	Input 1

BCD DATA				4N52
X8	X4	X2	X1	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	Blank
H	L	H	H	Blank
H	H	L	L	Blank
H	H	L	H	Blank
H	H	H	L	Blank
H	H	H	H	Blank
Decimal point				Display on V <sub>DP</sub> - L
Decimal point				Display off V <sub>DP</sub> - H
Enable				Load data V <sub>E</sub> - L
Enable				Latch data V <sub>E</sub> - H

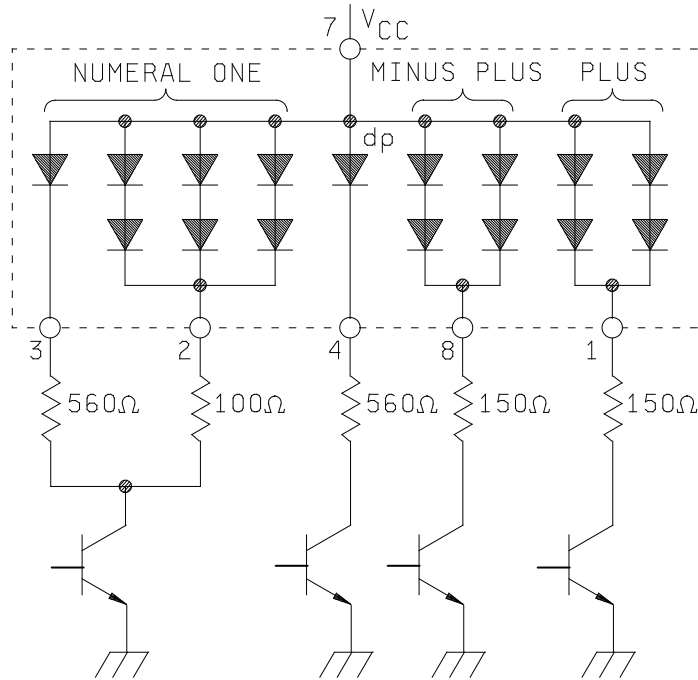


**TIMING DIAGRAM**

FIGURE 2. Functional block diagrams, terminal connections, timing diagrams, and truth tables - Continued.



4N53



TYPICAL DRIVE CIRCUIT;  $V_{CC}=5.0$  VOLTS

TRUTH TABLE

TERMINAL CONNECTIONS

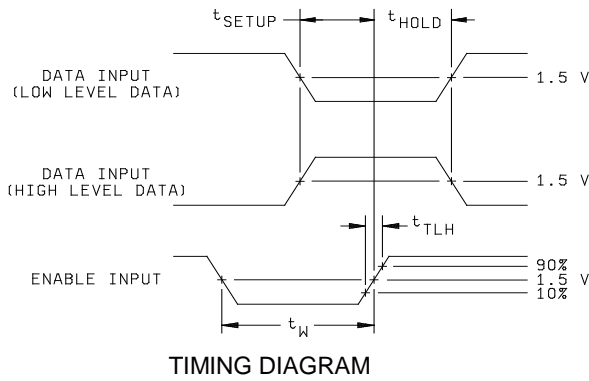
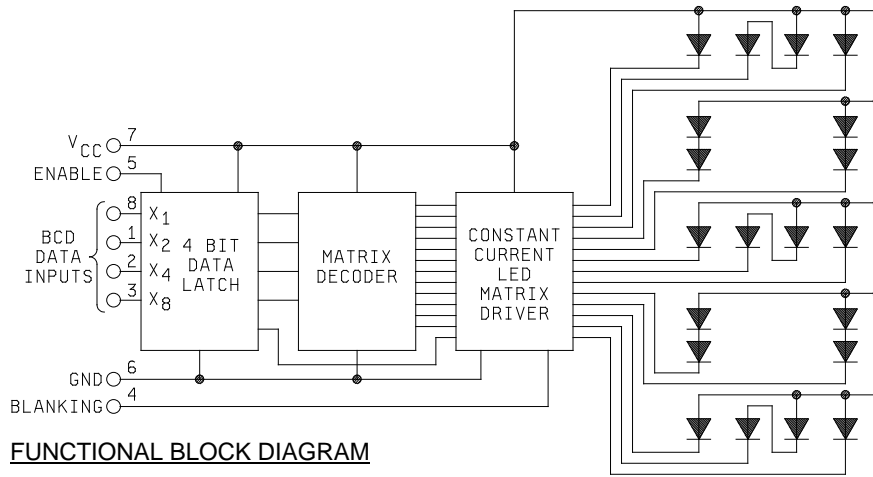
Pin	4N53
1	Plus
2	Numeral one
3	Numeral one
4	Decimal point
5	Open
6	Open
7	Vcc
8	Minus/plus

CHARACTER	PIN			
	1	2, 3	4	8
+	H	X	X	H
-	L	X	X	H
1	X	H	X	X
Decimal point	X	X	H	X
Blank	L	L	L	L

NOTES: L = LED driver transistor – OFF  
 H = LED driver transistor – ON  
 X = On or off

FIGURE 2. Functional block diagrams, terminal connections, timing diagrams, and truth tables - Continued.

MIL-PRF-19500/708A  
4N54



Pin	4N54
	Input 2
2	Input 4
3	Input 8
4	Blanking control
5	Latch enable
6	Ground
7	V <sub>CC</sub>
8	Input 1

TERMINAL CONNECTIONS

NOTE L = logic low  
H = logic high

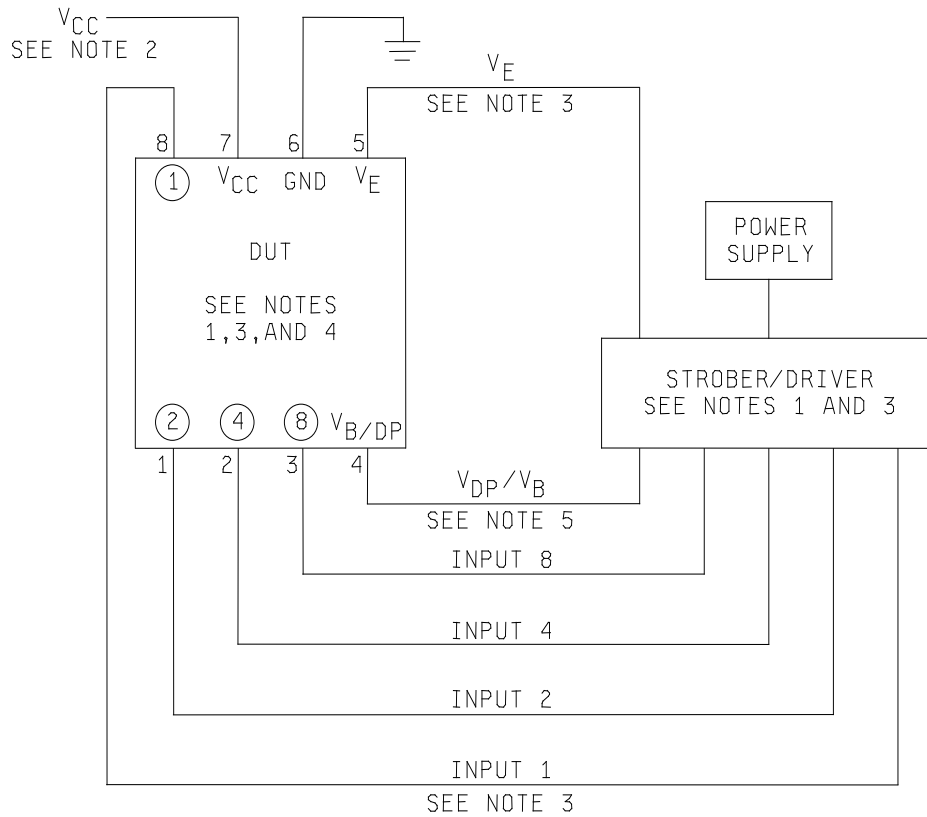
1/ The blanking input controls the LED display drivers, but does not have an effect on the display memory.

2/ With the enable high, changes in BCD inputs have no effect upon display memory or display character.

TRUTH TABLE				
BCD Data				4N54
X8	X4	X2	X1	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	A
H	L	H	H	B
H	H	L	L	C
H	H	L	H	D
H	H	H	L	E
H	H	H	H	F
Blanking 1/				Display on V <sub>B</sub> - L
				Display off V <sub>B</sub> - H
Enable 2/				Load data V <sub>E</sub> - L
				Latch data V <sub>E</sub> - H

FIGURE 2. Functional block diagrams, terminal connections, timing diagrams, and truth tables - Continued.

**4N51, 4N52 and 4N54**

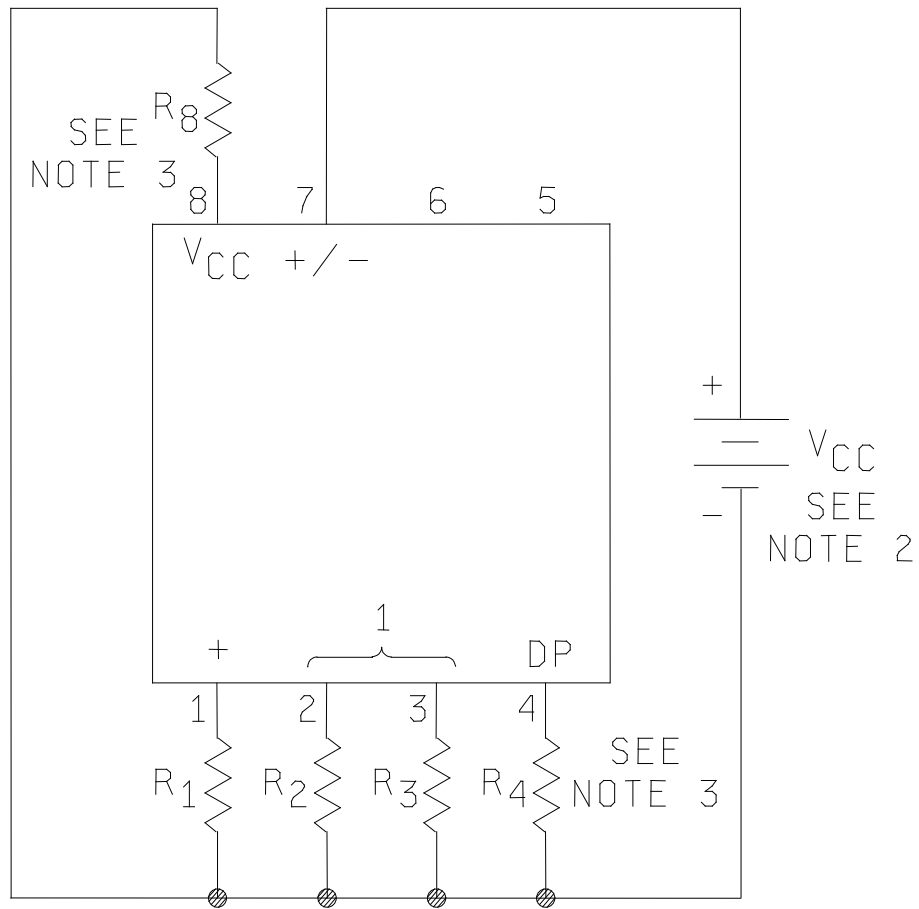


**NOTES:**

1. Strober/driver cycles the device under test through logic states at 1 character/second rate.
2.  $V_{CC} = 5.0 \text{ V}$ .
3. Logic and enable input allowed voltage levels:  $V_{IH} = 2.4 \text{ V dc to } V_{CC}$ ;  $V_{IL} = 0 \text{ V dc to } 4 \text{ V}$ .
4.  $T_A = 100^\circ\text{C}$ .
5.  $V_{DP}$  for 4N51 and 4N52;  $V_B$  for 4N54.

FIGURE 3. Burn-in circuits, 4N51, 4N52, and 4N54.

## 4N53



## NOTES:

1. The 8 mA average/LED; nominal current values are: Pin 1 and pin 8 = 16 mA, pin 2 = 24 mA, pin 3 and pin 4 = 8 mA.
2.  $V_{CC} = 5\text{ V}$ .
3. Current limiting resistors; 2 percent 1/4 W:  $R_1 = R_8 = 24\Omega$ ,  $R_2 = 15\Omega$ ,  $R_3 = R_4 = 91\Omega$ .
4.  $T_A = 100^\circ\text{C}$ .

FIGURE 3. Burn-in circuits, 4N53 - Continued.

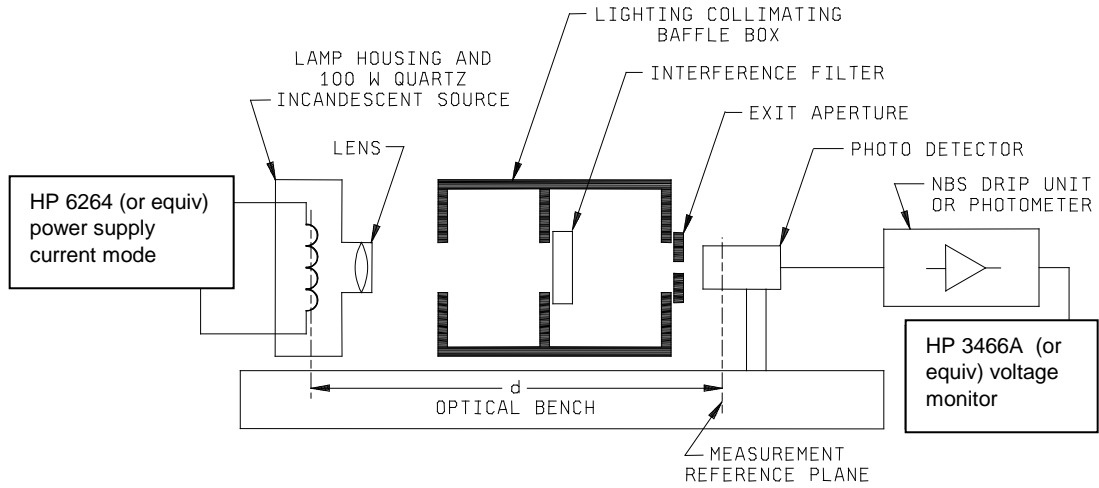


FIGURE 4. Photometer calibration block diagram.

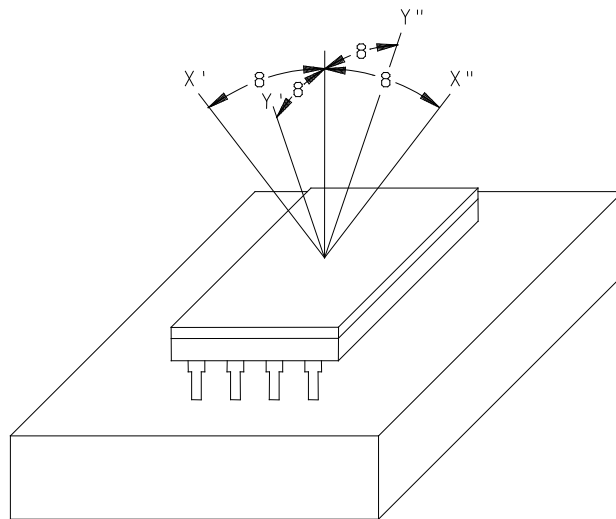


FIGURE 5. Off-axis luminous intensity.

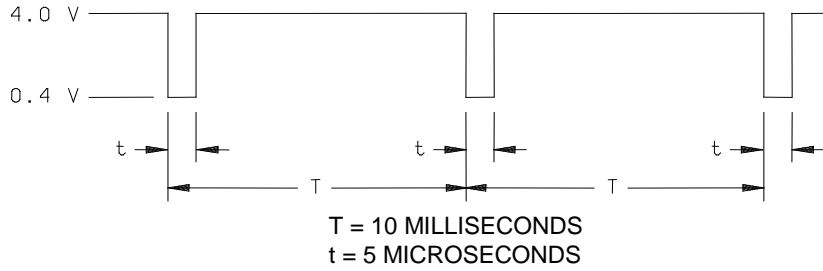


FIGURE 6. Pulse width modulation waveform.

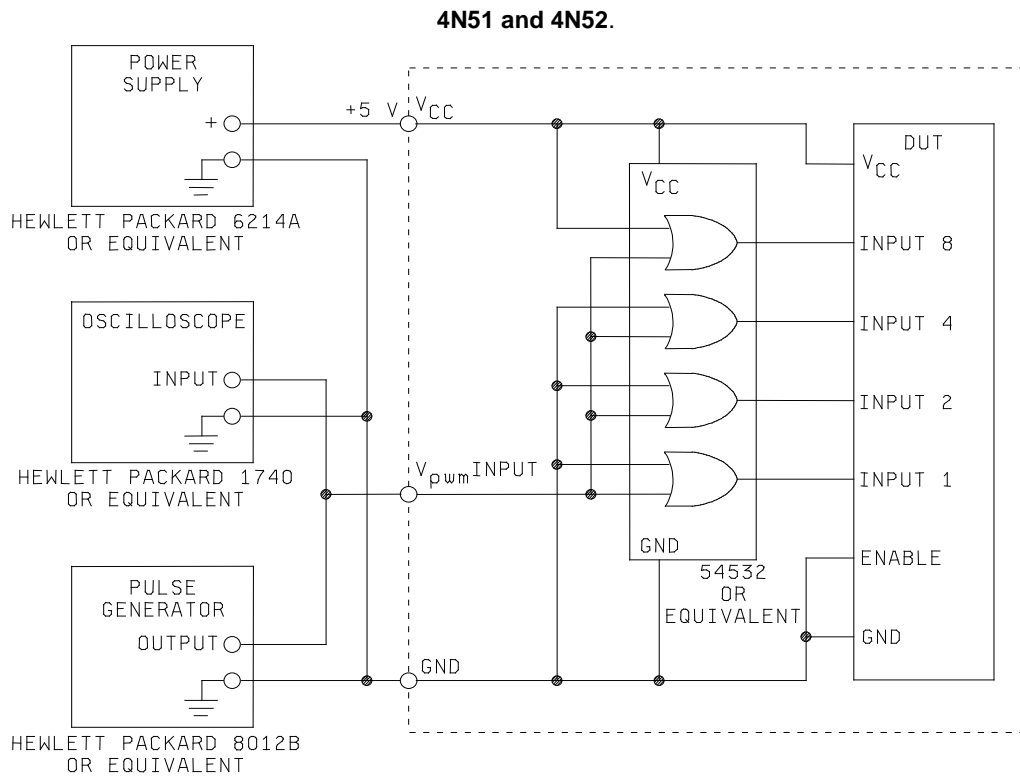


FIGURE 7. Dimming circuit, 4N51 and 4N52.

4N53

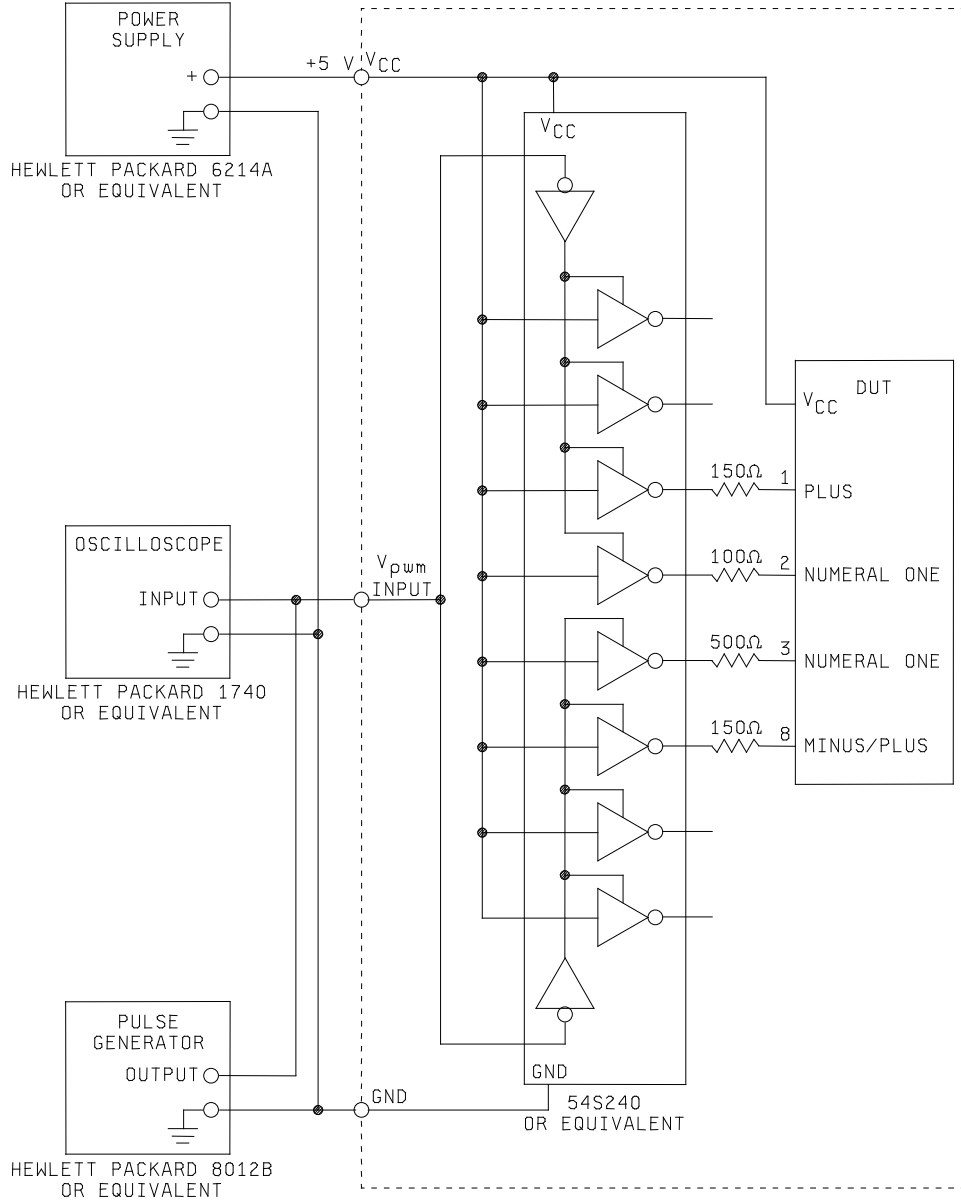


FIGURE 7. Dimming circuit, 4N53 - Continued.

4N54

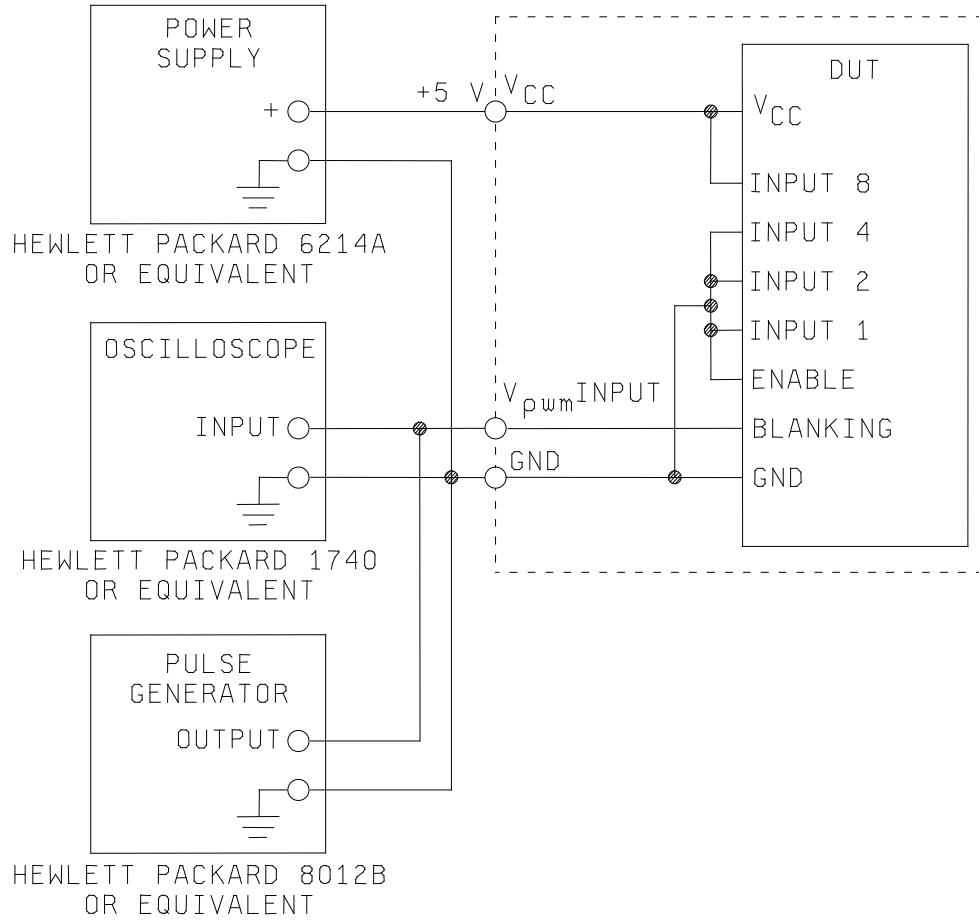


FIGURE 7. Dimming circuit, 4N54 - Continued.



## 5. PACKAGING

\* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

\* (This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

\* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

\* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.5).
- d. Product assurance level and type designator.

\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.daps.dla.mil>.

6.4 **Substitutability.** Displays covered by this specification are substitutable and directly interchangeable for the following device types:

Device type	PREVIOUS M87157 TYPE DESIGNATION	Device type	PREVIOUS M87157 TYPE DESIGNATION
JAN4N51CX	M87157/00101BCX	JANTX4N51CX	M87157/00101ACX
JAN4N52CX	M87157/00102BCX	JANTX4N52CX	M87157/00102ACX
JAN4N53CX	M87157/00103BCX	JANTX4N53CX	M87157/00103ACX
JAN4N54CX	M87157/00104BCX	JANTX4N54DX	M87157/00104ACX
JAN4N51DX	M87157/00101BDX	JANTX4N51DX	M87157/00101ADX
JAN4N52DX	M87157/00102BDX	JANTX4N52DX	M87157/00102ADX
JAN4N53DX	M87157/00103BDX	JANTX4N53DX	M87157/00103ADX
JAN4N54DX	M87157/00104BDX	JANTX4N54DX	M87157/00104ADX
JAN4N51EX	M87157/00101BEX	JANTX4N51EX	M87157/00101AEX
JAN4N52EX	M87157/00102BEX	JANTX4N52EX	M87157/00102AEX
JAN4N53EX	M87157/00103BEX	JANTX4N53EX	M87157/00103AEX
JAN4N54EX	M87157/00104BEX	JANTX4N54EX	M87157/00104AFX
JAN4N51FX	M87157/00101BFX	JANTX4N51FX	M87157/00101AFX
JAN4N52FX	M87157/00102BFX	JANTX4N52FX	M87157/00102AFX
JAN4N53FX	M87157/00103BFX	JANTX4N53FX	M87157/00103AFX
JAN4N54FX	M87157/00104BFX	JANTX4N54FX	M87157/00104AFX
JAN4N51GX	M87157/00101BGX	JANTX4N51GX	M87157/00101AGX
JAN4N52GX	M87157/00102BGX	JANTX4N52GX	M87157/00102AGX
JAN4N53GX	M87157/00103BGX	JANTX4N53GX	M87157/00103AGX
JAN4N54GX	M87157/00104BGX	JANTX4N54GX	M87157/00104AGX
JAN4N51HX	M87157/00101BHX	JANTX4N51HX	M87157/00101AHX
JAN4N52HX	M87157/00102BHX	JANTX4N52HX	M87157/00102AHX
JAN4N53HX	M87157/00103BHX	JANTX4N53HX	M87157/00103AHX
JAN4N54HX	M87157/00104BHX	JANTX4N54HX	M87157/00104AHX
JAN4N51IX	M87157/00101BIX	JANTX4N51IX	M87157/00101AIX
JAN4N52IX	M87157/00102BIX	JANTX4N52IX	M87157/00102AIX
JAN4N53IX	M87157/00103BIX	JANTX4N53IX	M87157/00103AIX
JAN4N54IX	M87157/00104BIX	JANTX4N54IX	M87157/00104AIX
JAN4N51JX	M87157/00101BJX	JANTX4N51JX	M87157/00101AIX
JAN4N52JX	M87157/00102BJX	JANTX4N52JX	M87157/00102AJX
JAN4N53JX	M87157/00103BJX	JANTX4N53JX	M87157/00103AJX
JAN4N54JX	M87157/00104BJX	JANTX4N54JX	M87157/00104AJX
JAN4N51KX	M87157/00101BKX	JANTX4N51KX	M87157/00101AJX
JAN4N52KX	M87157/00102BKX	JANTX4N52KX	M87157/00102AKX
JAN4N53KX	M87157/00103BKX	JANTX4N53KX	M87157/00103AKX
JAN4N54KX	M87157/00104BKX	JANTX4N54KX	M87157/00104AKX
JAN4N51XX	M87157/00101BXX	JANTX4N51XX	M87157/00101AXX
JAN4N52XX	M87157/00102BXX	JANTX4N52XX	M87157/00102AXX
JAN4N53XX	M87157/00103BXX	JANTX4N53XX	M87157/00103AXX
JAN4N54XX	M87157/00104BXX	JANTX4N54XX	M87157/00104AXX

\* 6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodian:  
Army - CR  
Air Force - 85  
DLA - CC

Preparing activity:  
DLA - CC  
  
Project (5980-2009-001)

\* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.daps.dla.mil/> .