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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS INTEGRATED CIRCUIT

μPD6464A,6465

ON-SCREEN CHARACTER DISPLAY CMOS LSI FOR 12-LINE, 24-COLUMN DECK-TYPE VCR

The μPD6464A,6465 are CMOS LSIs for on-screen character display that control various display systems (such as tape counters) including the program screens of deck-type VCRs and LD players. These LSIs are used in combination with a microcomputer.

It can display characters each consisting of 12 (horizontal) by 18 (vertical) dots. Some chinese characters and some pictograms can also be displayed by combining two or more characters.

The μPD6464A,6465 include a power-ON clear function and a video RAM batch clear command that mitigate the workload of the host microcomputer. It also has a synchronization separator and a ×4 multiplier on chip, eliminating the need of connecting an external separator IC and a crystal resonator, which reduces the mounting area and the total cost.

FEATURES

- Video signal input/output : Composite video signal
- Number of display characters : 12 lines, 24 columns (288 characters)
- Number of character types : 128 (μPD6464A)/256 (μPD6465) (ROM). Variable by mask code option.
- Character size : 1 dot/1 line. 2 lines (field) can be displayed in line units.
- Character color : White (single color)
- Background : No background, black framing, black-on-white, and black filling
- Dot matrix : 12 (horizontal) × 18 (vertical) dots without gap between adjacent characters
- Blinking : Blinking can be turned ON/OFF in character units. Blinking ratio is 1:1. Blinking frequency is selectable from about 0.5 Hz, 1 Hz, and 2 Hz in screen units.
- Character signal output: : Can support VCRs with S pins if external mixer is connected because character signal and blanking signal output pins are provided.
- Video RAM data clear : Video RAM data are cleared by video RAM clear command and power-ON clear function.
- Supported video signal method : NTSC/PAL/PAL-M/SECAM/PAL-N (μPD6464A only)
- Internal circuit : Synchronization separation circuit for composite synchronizing signal and ×4 multiplier
- Interface with microcomputer : Serial input type of 8-bit variable word length
- Supply voltage : +5 V, single power supply

ORDERING INFORMATION

Part Number	Package
μPD6464ACS-×××	24-pin plastic shrink DIP (300 mil)
μPD6465CS-×××	24-pin plastic shrink DIP (300 mil)
μPD6464AGT-×××	24-pin plastic SOP (375 mil)
μPD6465GT-×××	24-pin plastic SOP (375 mil)

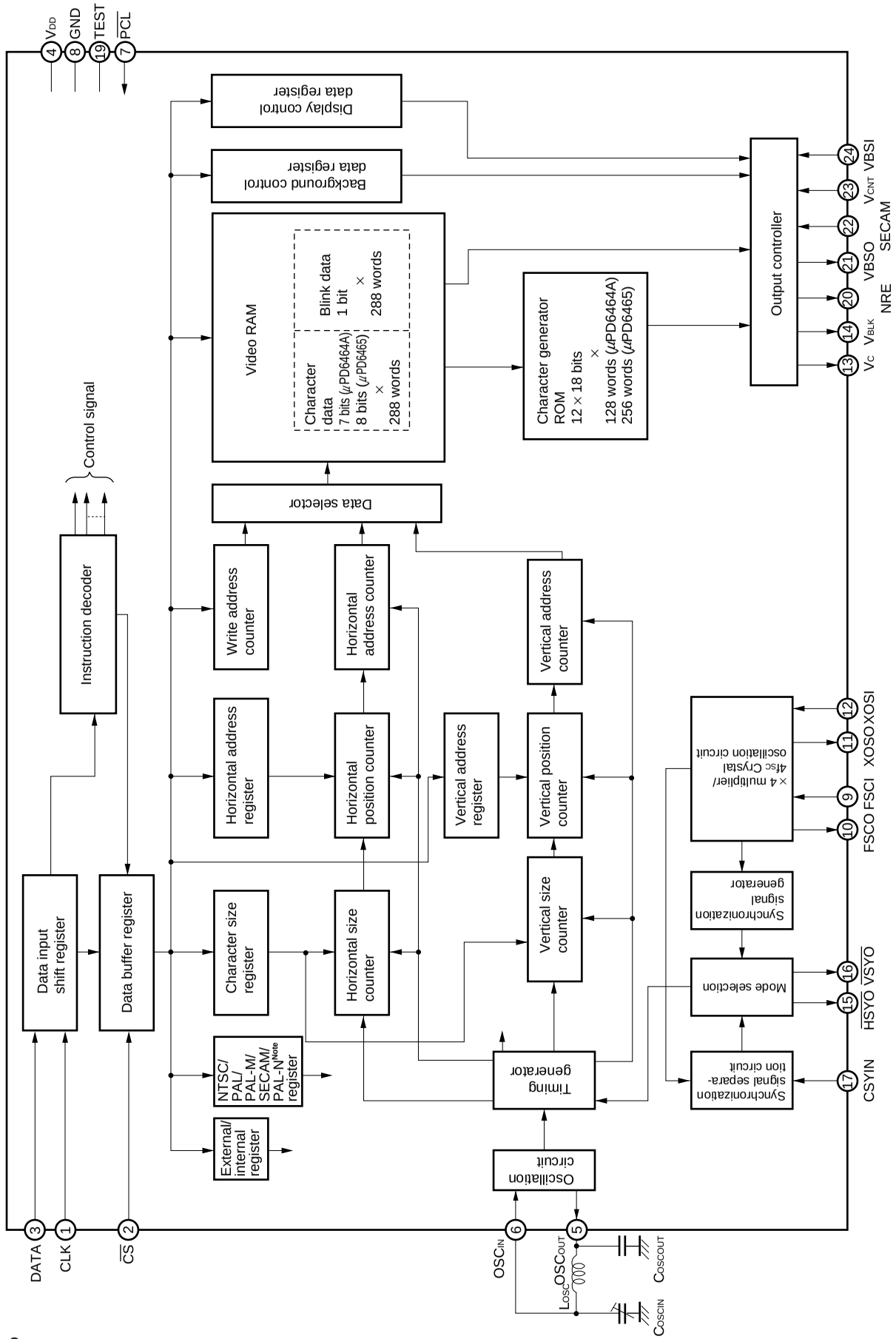
Remark ××× : ROM code suffix (CS-001, GT-101 : NEC standard device)

The information in this document is subject to change without notice.

Document No. S11043EJ4V0DS00 (4th edition)
Date Published May 1998 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ BLOCK DIAGRAM



Note μPD6464A only

PIN CONFIGURATION (Top View)

24-pin plastic shrink DIP (300 mil)

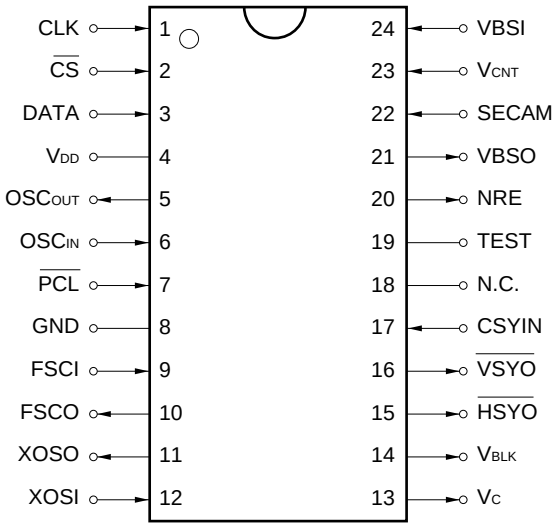
μPD6464ACS-×××

μPD6465CS-×××

24-pin plastic SOP (375 mil)

μPD6464AGT-×××

μPD6465GT-×××



Remark ×××: ROM code suffix (CS-001, GT-101: NEC standard device)

CLK	:	Clock Input	$\overline{PCL}$	:	Power-on Clear
$\overline{CS}$	:	Chip Select Input	SECAM	:	SECAM subcarrier Input
CSYIN	:	Composite Synchronization Signal Input	TEST	:	Test Pin
DATA	:	Serial Data Input	V_{BLK}	:	Blanking Signal Output
FSCI	:	f_{SC} Signal Input	VBSI	:	Composite Video Signal Input
FSCO	:	Frequency Error Output	VBSO	:	Composite Video Signal Output
GND	:	Ground	V_C	:	Character Signal Output
$\overline{HSYO}$	:	Horizontal Synchronization Signal Output	V_{CNT}	:	Video Signal Output Level Adjustment
N.C.	:	No Connection	V_{DD}	:	Power Supply
NRE	:	Noise Reduction Constant Append	$\overline{VSYO}$	:	Vertical Synchronization Signal Output
OSC_{IN}	:	LC Oscillation Input	XOSO	:	Quadruple Oscillation Output
OSC_{OUT}	:	LC Oscillation Output	XOSI	:	Quadruple Oscillation Input

PIN FUNCTIONS

No.	Symbol	Pin Name	Function
1	CLK	Clock input	Inputs clock for data read. Data input to the DATA pin is read at the rising edge of the clock input to this pin.
2	$\overline{CS}$	Chip select input	Serial transfer can be acknowledged by making this $\overline{CS}$ pin low.
3	DATA	Serial data input	Inputs control data. Data is read in synchronization with the clock input to the CLK pin.
4	V_{DD}	Power supply	Supplies power to the IC.
5	OSC_{OUT}	LC oscillation output	These are input and output pins of an oscillator that generates dot clocks. Connect a coil and a capacitor to these pins for oscillation.
6	OSC_{IN}	LC oscillation input	
7	$\overline{PCL}$	Power-ON clear	Power-ON clear pin. Make this pin high on power application. It initializes the internal circuitry of the IC.
8	GND	Ground	Ground pin of the IC.
★ 9	FSCI	f_{SC} signal input	In case of the ×4 multiplier, the color sub-carrier (f_{SC}) is input to this pin. In case of the $4f_{SC}$ Crystal oscillation, connect this pin to GND or V_{DD}.
★ 10	FSCO	Frequency error output	The frequency error signal of the ×4 multiplier is output to this pin. In case of the $4f_{SC}$ Crystal oscillation, this pin should be open.
11	XOSO	Quadruple oscillation output	A quadruple oscillation LC for internal video signal generation is connected to these pins. A crystal oscillator can also be connected.
12	XOSI	Quadruple oscillation input	
13	V_C	Character signal output	Character signal output pin. Positive signal output.
14	V_{BLK}	Blanking signal output	This pin outputs a blanking signal that cuts the video signal. It corresponds to the output of V_C. Positive signal output.
15	$\overline{HSYO}$	Horizontal synchronization signal output	Outputs a horizontal synchronization signal separated from a composite synchronization signal.
16	$\overline{VSYO}$	Vertical synchronization signal output	Outputs a vertical synchronization signal separated from a composite synchronization signal.
★ 17	CSYIN	Composite synchronization signal input	A composite synchronization signal is input to this pin for synchronization signal separation. In case of the external signal mode, input the signal certainly. Input a positive synchronization signal.
18	N. C.	Non connection	Non connection. Leave this pin open.
19	TEST	Test pin	Test mode select pin. Connect this pin to GND.
20	NRE	Noise reduction constant append	Constant append pin for noise reduction.
21	VBSO	Composite video signal output	Outputs a composite video signal mixing a character signal.
★ 22	SECAM	SECAM subcarrier input	SECAM sub-carrier signal mixing pin. In cases of any system except for SECAM, this pin should be open.
23	V_{CNT}	Video signal output level adjustment	Adjusts the output level of the composite video signal and luminance signal.
24	VBSI	Composite video signal input	Inputs a composite video signal. Inputs a signal with the leading edge clamped, consisting of a negative synchronization signal and a positive video signal.

CONTENTS

1. COMMANDS

1.1 Command Format

Control commands are of variable length in 8-bit units and are input in serial.

Three types of commands are available: 1-byte commands consisting of 8 bits of instruction and data in combination, 2-byte commands of 16 bits of instruction and data in combination, and a 2-byte contiguous command that can be abbreviated for input.

Input command data from the MSB first.

1.2 Command List

1-byte commands

(MSB)

Function	D7	D6	D5	D4	D3	D2	D1	D0
Video RAM batch clear	0	0	0	0	0	0	0	0
Display control	0	0	0	1	D0	LC	BL1	BL0
Internal video signal color control	0	0	1	0	R	G	B	0
Background control	0	0	1	1	0	BS1	BS0	0
Internal/external mode control, crystal oscillation control	0	1	0	0	0	E/I	0	X_{OSC}
Video signal method control	0	1	0	0	1	N/P2	N/P1	N/P0
Oscillation method control	0	1	0	1	0	0	Xf_c	0

2-byte commands

(MSB)

Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display position control	1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0
Write address control	1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0
Output level control	1	0	0	1	0	0	0	VPD	0	0	0	0	0	1	VC1	VC0
Character size control	1	0	0	1	1	0	0	0	0	S0	0	0	AR3	AR2	AR1	AR0
Test mode [Note]	1	0	1	1	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

Note Must not be used.

2-byte contiguous command

(MSB)

Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display character control	1	1	0	0	0	0	BL	0	[Note] C7	C6	C5	C4	C3	C2	C1	C0

Note Fixed to "0" (μPD6464A)

1.3 Power-ON Clear Function

Because the internal status of the IC is unstable on power application, initialize the IC by making the $\overline{PCL}$ pin high and executing a clear operation. When the clear operation has been performed, the following setting is made:

- Test mode is cleared.
- All the character data of the video RAM (12 lines, 24 columns) are set to display OFF data (7E$_H$ (μPD6464A)/FE$_H$ (μPD6465)) and the blinking data are set to OFF.
- Video RAM write address (line 0, column 0) is set.
- Character size is set to ×1 (minimum) on all lines.
- Display is turned OFF and LC oscillation is turned ON.

The time required for the power-ON clear operation can be calculated by the following expression:

$t = t_{PCLL}$**Note** + {video RAM clear time}
$= 10\ (\mu s) + \{10\ (\mu s) + 12/f_{OSC}\ (MHz) \times 288\ [\mu s]\}$

Note Refer to **7. ELECTRICAL SPECIFICATIONS Power-ON Clear Specification**.

Remark f_{OSC}: LC oscillation frequency (dot clock frequency)

2. COMMAND DETAILS

2.1 Video RAM Batch Clear Command

This command can clear the video RAM with a single command.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

The video RAM batch clear command performs the following setting:

- Sets all the character data of the video RAM (12 lines, 24 columns) to display OFF data (7E$_H$ (μPD6464A)/FE$_H$ (μPD6465)) and blinking data to OFF.
- Sets a video RAM write address (line 0, column 0).
- Sets the character size to ×1 (minimum) on all lines.
- Turns display OFF and LC oscillation ON.

The time required for clearing the video RAM can be calculated by the following expression:

t = video RAM clear time
$= 10\ (\mu s) + 12/f_{OSC}\ (MHz) \times 288\ [\mu s]$

Remark f_{OSC}: LC oscillation frequency (dot clock frequency)

2.2 Display Control Command

This command turns ON/OFF the display and controls LC oscillation and blinking of characters.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	D0	LC	BL1	BL0

Blinking control bits		
BL1	BL0	Function
0	0	Blinking OFF
0	1	Blinking frequency: about 2 Hz
1	0	Blinking frequency: about 1 Hz
1	1	Blinking frequency: about 0.5 Hz

LC oscillation control bit	
LC	Function
0	LC oscillation OFF
1	LC oscillation ON

Display ON/OFF control bit	
D0	Function
0	Display OFF
1	Display ON

- Blinking control bits

  These bits blink the character that is specified by the display character control command.
  The blinking ratio is 1:1, and three blinking frequencies can be selected.
  Blinking in character units can be specified by the display character control command.

- LC oscillation control bit

  This bit controls LC oscillation and can turn ON/OFF the oscillation circuit. While no character is displayed, oscillation can be stopped to reduce the power dissipation.
  Data cannot be written to the video RAM with oscillation stopped. To write data to the video RAM, be sure to turn ON oscillation.

  Remark Oscillation is synchronized with $\overline{\text{Hsync}}$ when display is ON and LC oscillation is ON, and oscillation is stopped while $\overline{\text{Hsync}}$ is low. When display is OFF and LC oscillation is ON, oscillation is performed, regardless of the level of $\overline{\text{Hsync}}$.

- Display ON/OFF control bit

  This bit turns ON/OFF the display output. The display is turned ON/OFF in synchronization with the fall of $\overline{\text{Hsync}}$.

2.3 Internal Video Signal Color Control Command

This command sets the color of an internal video signal. The internal video signal is a video signal (e.g., blue back) internally generated by the μPD6464A, 6465. While no external video signal is input to the μPD6464A, 6465 and therefore no character can be displayed, if the internal video signal is selected, characters can be displayed.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	R	G	B	0

Internal video signal color control bits			
R	G	B	Function
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Setting prohibited
1	0	0	Setting prohibited
1	0	1	Setting prohibited
1	1	0	Setting prohibited
1	1	1	White

- Internal video signal color control bits

  These bits can select four colors as the color of the internal video signal.

2.4 Background Control Command

This command selects the background of the displayed character.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	BS1	BS0	0

Background control bits		
BS1	BS0	Function
0	0	No background
0	1	Black framing
1	0	Black-on-white
1	1	Black filling

- Background control bits
  These bits select the type of background in screen units from none, black-framed, black-on-white, or black-filled background.

  No background : Only character data are output.

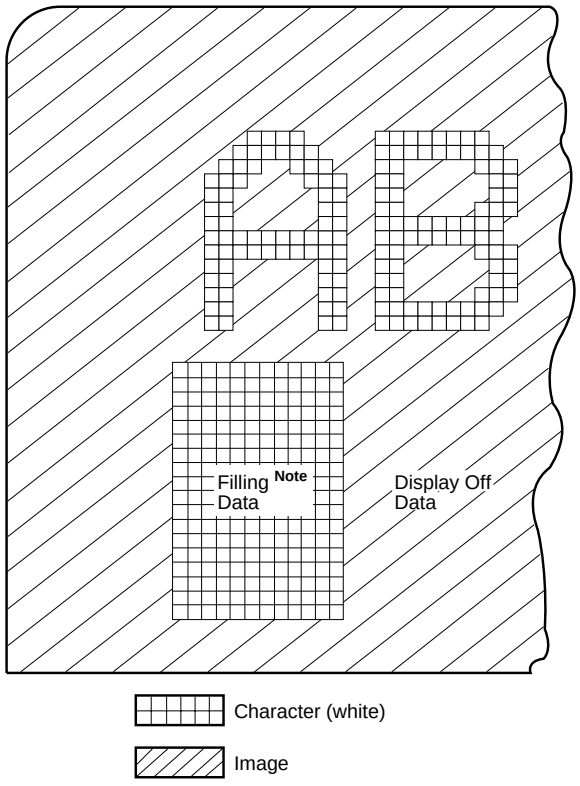
  Black framing : If the left- and rightmost columns or the top and bottom lines of a dot matrix are not used, the displayed character can be framed horizontally, vertically, or diagonally. When the dots on the rightmost or leftmost column of the dot matrix are used, a frame is displayed in the adjacent character display areas. Even when the dots on the top and bottom lines of the dot matrix are used, the lines above and below the dot matrix are not framed. Even if the character size is changed, the size of black framing is fixed to 1 dot, which is the minimum size.

  Black-on-white : A black background is displayed on the rightmost and leftmost positions of the display area of the character written to the video RAM with 1 extra dot, which is the minimum size, at both positions.

  Black filling : A black background is displayed outside the character display area, in addition to the black-on-white background.,

Display format in each background mode

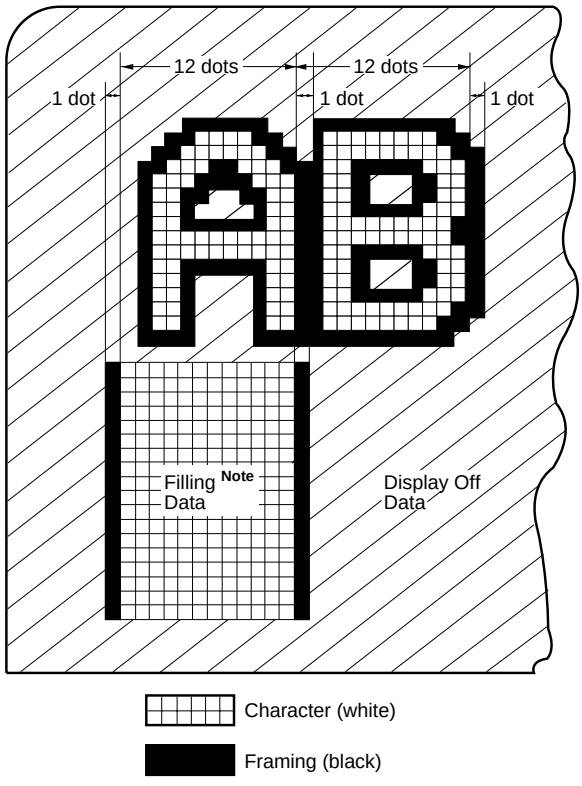
No backgraund



Character (white)

Image

Black framing

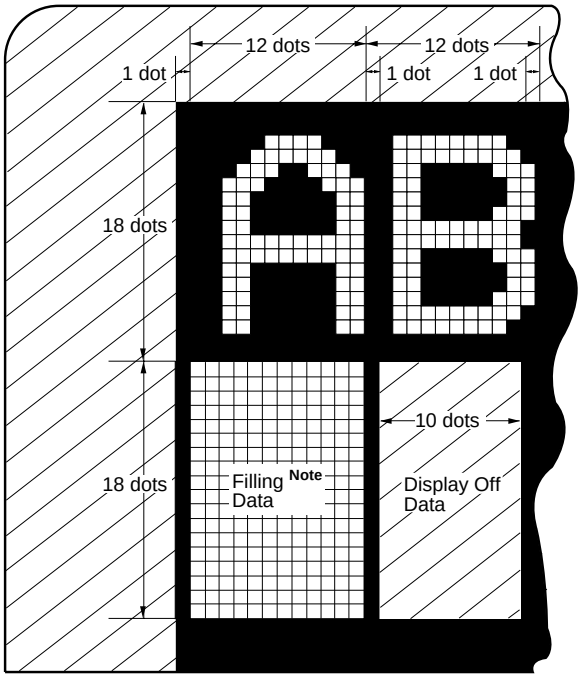


Character (white)

Framing (black)

Image

Black-on-white

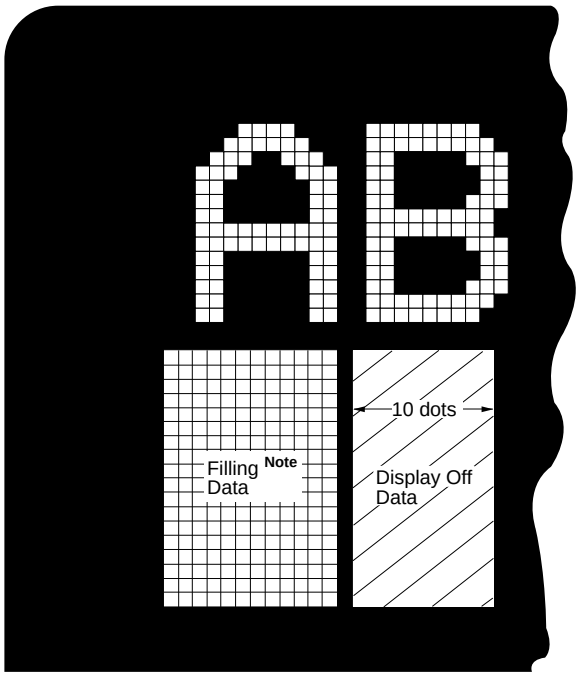


Character (white)

Background (black)

Image

Black filling



Character (white)

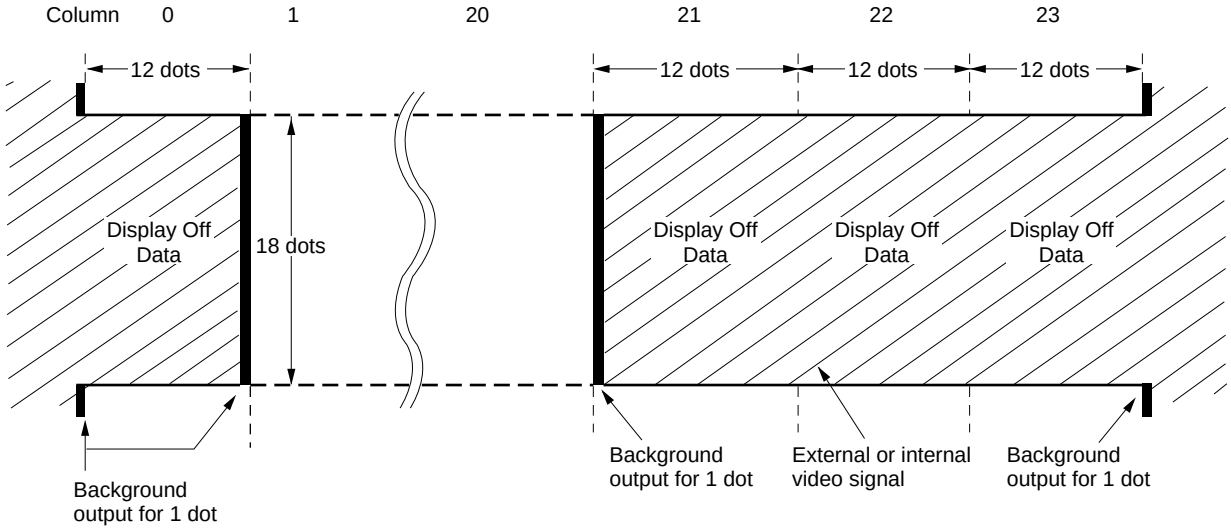
Background (black)

Image

Note Filling data means 1F$_H$ (μPD6464A), 6E$_H$ (μPD6465) with the NEC's standard character.

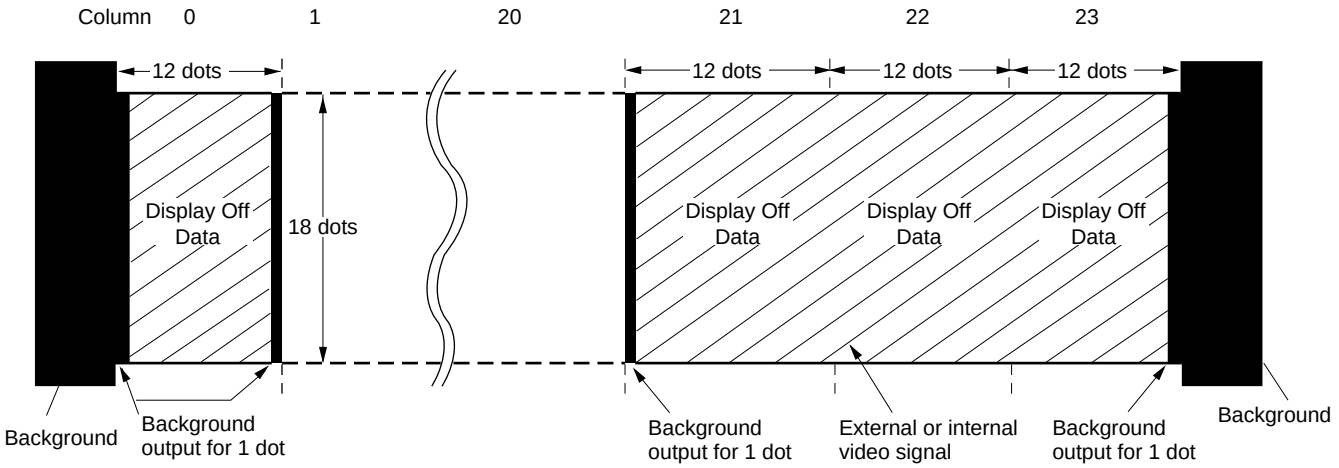
Example of display when Display Off Data is used

- Black-on-white background



The background color is output on 1 dot on both the edges of Display Off Data when the Display Off Data is used.

- Black-filled background



The background color is output on 1 dot on both the edges of Display Off Data when the Display Off Data is used.

Remark The “Background output for 1 dot” does not change by 1 dot, which is the minimum size, even when the character size is changed.

2.5 Internal/external Mode Control, Crystal Oscillation Control Command

This command selects the video signal with which a character signal overlaps (internal mode/external mode) and controls ON/OFF of crystal oscillation.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	E/I	0	Xosc

Crystal oscillation control bit	
Xosc	Function
0	Oscillation OFF
1	Oscillation ON

Internal/external mode control bit	
E/I	Function
0	External video signal mode
1	Internal video signal mode

- Crystal oscillation control bit

  This bit controls oscillation of the crystal for internal video signal generation. When crystal oscillation is turned ON and the mode is changed from the external video signal mode to the internal video signal mode, the internal video signal is selected without the screen disturbed.

  When crystal oscillation is turned OFF, the synchronization separation circuit does not operate. Be sure to turn ON crystal oscillation.

★ • Internal/external mode control bit

External video signal mode : In this mode, character signals are output to the μPD6464A and 6465, overlapping the external video signal that is input from external. The overlapped signal is output to the VBSO pin. If character signals should not be overlapped, set the display ON/OFF control bit to 0 (Display OFF) with the display control command. Moreover, a composite synchronization signal (Csync), which synchronizes with the video signal input from external, is required to be input from the CSYIN pin. If no Csync exists, input the composite synchronization signal generated from the input video signal via the composite sync signal separation circuit (refer to **5. COMPOSITE SYNC. SIGNAL SEPARATION CIRCUIT**).

In the timing generator block built in the μPD6464A and 6465, a horizontal synchronization signal and a vertical synchronization signal are generated by separating from a composite synchronization signal synchronously. A reference signal is generated from these synchronous signals. The reference signal is used to reset and count the horizontal control block, vertical control block, and output control block. If Csync is not input, characters may not be displayed because the reference signal is not generated in the timing generator block.

Internal video signal mode : In this mode, characters are output overlapping the video signal that is created in the μPD6464A and 6465 (e.g., blue back signal) to the VBSO pin. In the internal video signal mode, characters can be displayed on the screen because horizontal and vertical synchronization signals are generated in a device, even if no composite synchronization signal is input.

2.6 Video Signal Method Control Command

The μPD6464A, 6465 can select the NTSC, PAL, and PAL-M methods for the internal video signal.
The μPD6464A can also select the PAL-N method.
When the SECAM method is selected, the internal video signal is output by the PAL method.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	N/P2[Note]	N/P1	N/P0

Video signal method control bits			
N/P2	N/P1	N/P0	Function
0	0	0	NTSC
0	0	1	PAL
0	1	0	PAL-M
0	1	1	SECAM
1	0	0	PAL-N
Setting prohibited			

Note Fixed to "0" (μPD6465).

- Video signal method control bits
  These bits can generate internal NTSC, PAL, PAL-M and PAL-N (μPD6464A only) video signals.
  With the SECAM method, however, a color subcarrier from the SECAM color subcarrier input pin (pin 22) is fixed in the external mode. In the internal mode, an internal PAL video signal is generated.
  The internal video signal is generated by using a ×4 multiplier or an external crystal. Use a crystal with a frequency of 4 f_{SC} for each video signal.

2.7 Oscillation Method Control Command

The μPD6464A, 6465 can select a crystal for internal video signal generation or a ×4 multiplier.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	Xf_c	0

Oscillation method control bit	
Xf_c	Function
0	Quadruple oscillation
1	$4f_{SC}$ crystal oscillation

★ • Oscillation method control bit

In the μPD6464A and 6465, the oscillation method can be selected from ×4 multiplication oscillation and $4f_{SC}$ crystal oscillation with the oscillation method control command.

When ×4 multiplication oscillation is selected, the f_{SC} signal must be input from the FSCI pin. The $4f_{SC}$ signal is generated from an external LC resonator and an internal circuit of the μPD6464A and 6465. The phase of four-divided $4f_{SC}$ signal generated via LC oscillation is compared with that of the f_{SC} signal that is input to the FSCI pin. The obtained phase error is converted to a voltage value, and then output from the FSCO pin. In the circuit shown in **8. APPLICATION CIRCUIT DIAGRAM (1) In ×4 multiplication oscillation**, the $4f_{SC}$ signal synchronizing with the external f_{SC} signal is generated by changing the capacitance of varactor diodes with this voltage that is based on a phase error.

When $4f_{SC}$ crystal oscillation is selected, the FSCI and FSCO pins are not used. These pins should be connected as follows.

FSCI pin (pin 9) : Connect to GND or V_{DD}.
FSCO pin (pin 10) : Leave open.

Remark The scanning method in the internal video signal mode is non-interlacing. With the NTSC and PAL-M methods, the number of scanning lines is 263. With the PAL and PAL-N method, it is 312.

2.8 Display Position Control Command

This command can set the display start position in 12-dot units and 32 steps in the horizontal direction, and in 9-line units and 32 steps in the vertical direction.

Because this command is a 2-byte command, it must be input in 16-bit units even when the command is successively input.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0

Horizontal display start position control bit					
H4	H3	H2	H1	H0	Function
0	0	0	0	0	From rising of $\overline{\text{Hsync}}$ $(12 \times 1)/f_{osc}+4/f_{osc}$ (μs)
0	0	0	0	1	From rising of $\overline{\text{Hsync}}$ $(12 \times 2)/f_{osc}+4/f_{osc}$ (μs)
≈	≈	≈	≈	≈	≈
1	1	1	1	1	From rising of $\overline{\text{Hsync}}$ $(12 \times 32)/f_{osc}+4/f_{osc}$ (μs)

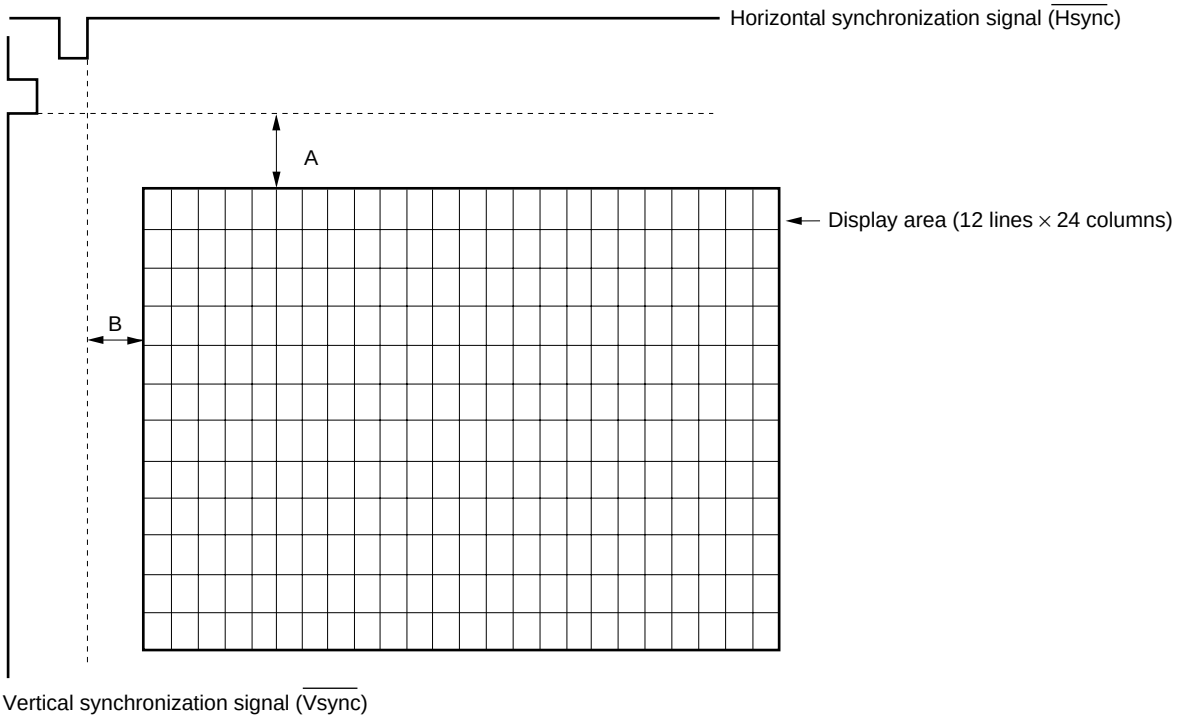
Remark f_{osc}: LC oscillation frequency (Dot Clock frequency)

Vertical display start position control bit					
V4	V3	V2	V1	V0	Function
0	0	0	0	0	From rising of $\overline{\text{Vsync}}$ 9H × 0
0	0	0	0	1	From rising of $\overline{\text{Vsync}}$ 9H × 1
≈	≈	≈	≈	≈	≈
1	1	1	1	1	From rising of $\overline{\text{Vsync}}$ 9H × 31

Remark H: Line

- Horizontal display start position control bits
  The horizontal display start position can be set in 12-dot units and 32 steps, 16 clocks after the rising of the horizontal synchronization signal ($\overline{\text{Hsync}}$) (16/fosc (MHz)).

- Vertical display start position control bits
  The vertical display start position can be set in 9-line units and 32 steps, from the rising of the vertical synchronization signal ($\overline{\text{Vsync}}$).



A: $9H\ (\text{line}) \times (2^4V_4 + 2^3V_3 + 2^2V_2 + 2^1V_1 + 2^0V_0)$

B: $\dfrac{12}{f_{OSC}\ (\text{MHz})} \times (2^4H_4 + 2^3H_3 + 2^2H_2 + 2^1H_1 + 2^0H_0) + \dfrac{16}{f_{OSC}\ (\text{MHz})}$

Remark fosc: LC oscillation frequency (Dot Clock frequency)

$\overline{\text{Hsync}}$ and $\overline{\text{Vsync}}$, which serve as references, are as follows:
Internal video signal mode : $\overline{\text{Hsync}}$ and $\overline{\text{Vsync}}$ are generated by internal circuit.
External video signal mode : $\overline{\text{Hsync}}$ and $\overline{\text{Vsync}}$ are generated from composite synchronization signal, input to CSYN pin (pin 17), by sync. signal separation circuit.

2.9 Write Address Control Command

This command specifies a write address when a character is written to the display area (video RAM) of 12 lines by 24 columns. Because this command is a 2-byte command, it must be input in 16-bit units even when input successively.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0

Write column address control bits					
AC4	AC3	AC2	AC1	AC0	Function
0	0	0	0	0	Sets column 0
0	0	0	0	1	Sets column 1
≈	≈	≈	≈	≈	≈
1	0	1	1	1	Sets column 23
Setting prohibited					

Write line address control bits				
AR3	AR2	AR1	AR0	Function
0	0	0	0	Sets line 0
0	0	0	1	Sets line 1
≈	≈	≈	≈	≈
1	0	1	1	Sets line 11
Setting prohibited				

- Write column address control bits
  One line consists of 24 columns in the horizontal direction. These bits specify the column to be written.

- Write line address control bits
  One column consists of 12 lines in the vertical direction. These bits specify the line to be written.

Video RAM configuration

The video RAM consists of 12 lines by 24 columns as shown below.

The number of display characters therefore is 12 lines by 24 columns (when all the lines are set to the minimum size).

AC4, AC3, AC2, AC1, AC0		00000	00001	00010	≈	10110	10111
AR3, AR2, AR1, AR0	0000				≈		
	0001				≈		
	0010				≈		
	0011				≈		
	0100				≈		
	0101				≈		
	0110				≈		
	0111				≈		
	1000				≈		
	1001				≈		
	1010				≈		
	1011				≈		

2.10 Output Level Control Command

The μPD6464A, 6465 can set the luminance level of the character and background (including the frame) by using a command.

This command is a 2-byte command, and must be input in 16-bit units even when successively input.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	VPD	0	0	0	0	0	1	VC1	VC0

Character level control bits		
VC1	VC0	Function
0	0	Setting Prohibited
0	1	75 I.R.E.
1	0	Setting Prohibited
1	1	90 I.R.E.

Internal video signal amplitude control bit	
VPD	Function
0	1 V_{p-p} amplitude
1	2 V_{p-p} amplitude

- Character level control bits

  These bits can select two character luminance levels: 75 or 90 I.R.E.

  If these bits are not set, the character level is set to 75 I.R.E.

  Remark The background (frame) level is fixed to 0 I.R.E.

- Internal video signal amplitude control bit

  This bit sets the amplitude of the internal video signal to 1 or 2 V_{p-p} (this amplitude must match the amplitude of the signal input in the external video signal mode). When the amplitude is set to 1 V_{p-p}, the voltage applied to the V_{CNT} pin must be 2.5 V.

  When the amplitude is set to 2 V_{p-p}, apply 5 V to the V_{CNT} pin.

2.11 Character Size Control Command

This command can set the character size in line units (in both the horizontal and vertical directions). Because this is a 2-byte command, it must be input in 16-bit units even when successively input.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0	0	S0	0	0	AR3	AR2	AR1	AR0

Line specification control bits				
AR3	AR2	AR1	AR0	Function
0	0	0	0	Sets line 0
0	0	0	1	Sets line 1
≈	≈	≈	≈	≈
1	0	1	1	Sets line 11
Setting Prohibited				

Character size control bit	
S0	Function
0	Vertical 1 dot: 1H, horizontal 1 dot: 1t dot (minimum size)
1	Vertical 1 dot: 2H, horizontal 1 dot: 2t dots

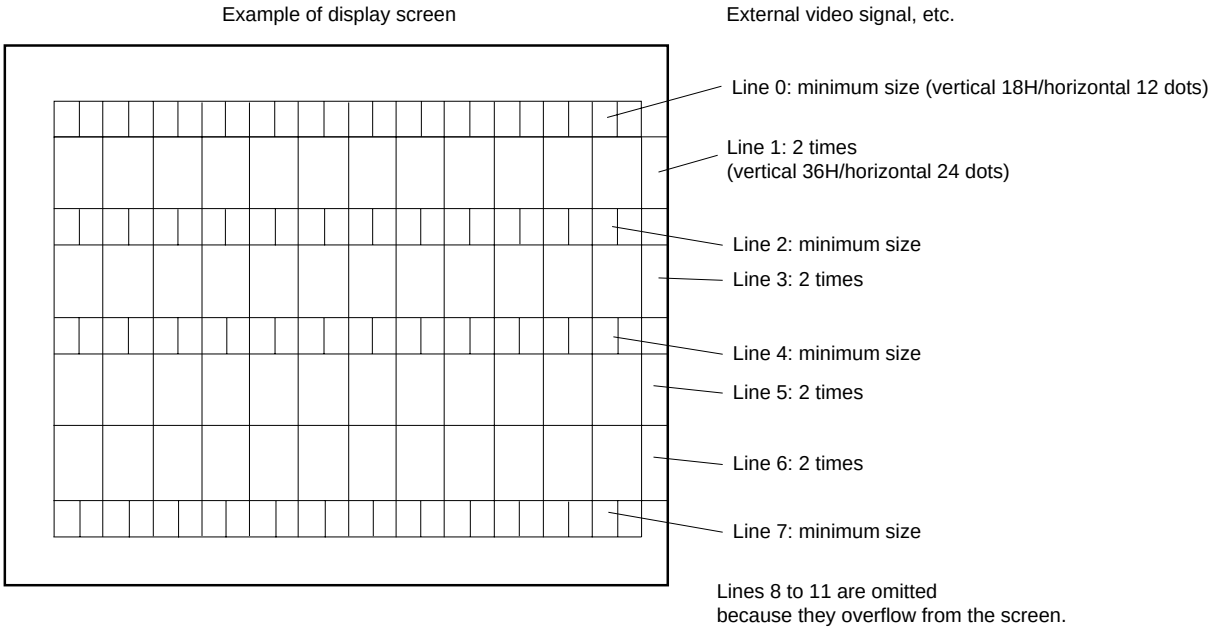
$$1t\ dot = \frac{1}{f_{OSC}\ (MHz)}\ \mu s$$

f_{OSC}: LC oscillation frequency

- Line specification control bits
  These bits specify the character size in line units, and control which line is to be specified.

- Character size control bit
  This bit selects the character size in two steps.

Display with two character size specified



The size in the vertical direction (the number of horizontal scanning lines) is the size in field units.

2.12 Test Mode Command

This command is for testing the IC. Do not set this command.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

[Reference] Test mode clear command

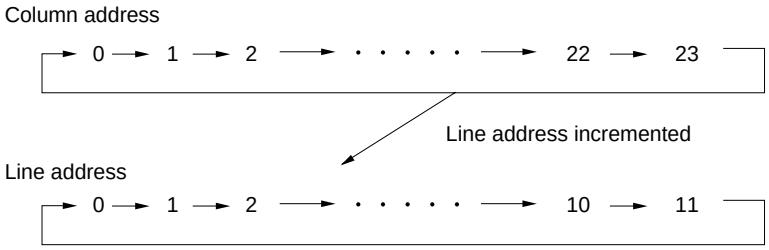
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

2.13 Display Character Control Command (2-byte contiguous command)

This command specifies the character data and blinking data to be written to the video RAM.

When inputting this command, turn ON LC oscillation (if LC oscillation is turned OFF, no character can be written to the video RAM).

Because this command is a 2-byte contiguous command, if character data are successively written without the blinking data changed, the second character and those that follow can be abbreviated to the lower 8 bits (D7 to D0). In this case, the write column address is automatically incremented (if a character is written to column 23 at the rightmost position, the next write address is automatically incremented to column 0 of the next line (leftmost position)).



D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	0	BL	0	C7	C6	C5	C4	C3	C2	C1	C0

Character specification bits								
C7 Note 1	C6	C5	C4	C3	C2	C1	C0	Function
0	0	0	0	0	0	0	0	Outputs data of 00_H
0	0	0	0	0	0	0	1	Outputs data of 01_H
≈	≈	≈	≈	≈	≈	≈	≈	≈
1	1	1	1	1	1	1	0	Outputs data DISPLAY OFF Note 2
1	1	1	1	1	1	1	1	End code of 2-byte contiguous command Note 3

Blink control bit	
BL	Function
0	Does not blink character
1	Blinks character

Notes 1. Fixed to "0" (μPD6464A).

2. $7E_H$ (μPD6464A), FE_H (μPD6465).

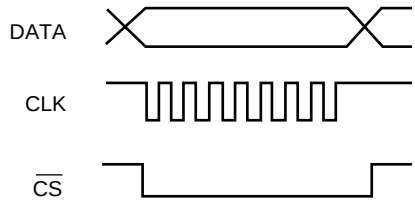
3. $7F_H$ (μPD6464A), FF_H (μPD6465).

- Character specification bits
  These bits specify the address of a character. There are 128 types of characters available (μPD6465: 256 types). Addresses 7EH (μPD6464A), FEH (μPD6465), 7FH (μPD6464A) and FFH (μPD6465), however, are fixed to the display OFF data and 2-byte contiguous command end code, respectively (no character can be set to these addresses even when the character is changed by mask code option because these addresses are fixed nevertheless). The character designs can be changed by mask code option.

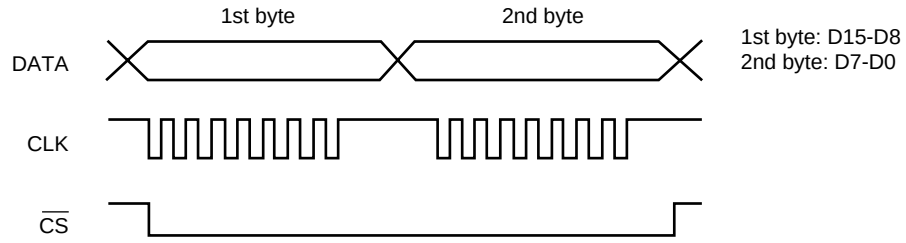
- Blink control bit
  This bit specifies whether the character written to the video RAM blinks, in character units. For the details of turning ON/OFF blinking in screen units, refer to **2.2 Display Control Command**.

3. TRANSFERRING COMMANDS

3.1 1-Byte Command

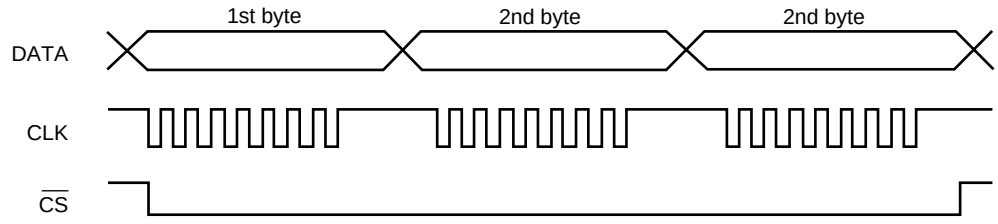


3.2 2-Byte Command



When transferring a 2-byte command, keep $\overline{CS}$ low between the first byte and second byte.

3.3 2-Byte Contiguous Command



The 2-byte contiguous command writes a character to the video RAM. To write characters in succession without changing the blink data, first transfer the first byte and then transfer the second bytes (character addresses) in succession.

3.4 Successive Command Input

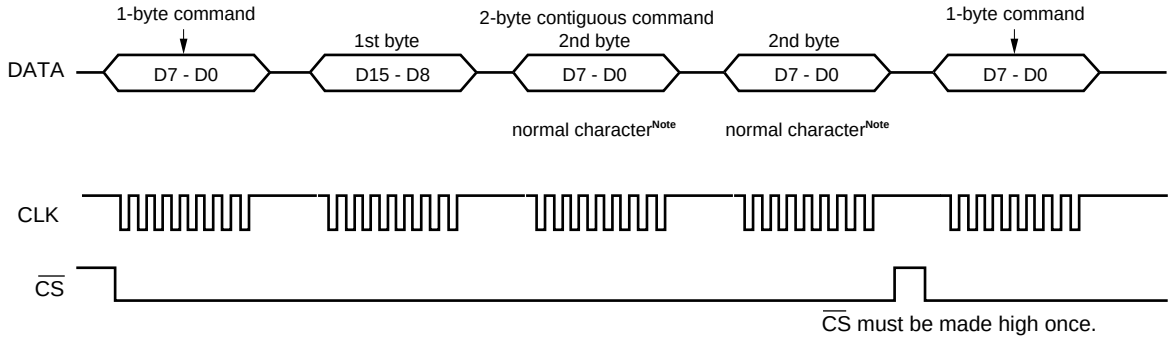
Transfer each of the 1-byte, 2-byte, and 2-byte contiguous commands from a microcomputer to the μPD6464A, 6465 as described below.

When transferring a 1-byte command, 2-byte command, or a 2-byte contiguous command with the blink data changed after a 2-byte contiguous command has been transferred, either make $\overline{CS}$ high once, or transfer end code of the 2-byte contiguous command[Note] at the end of the 2-byte contiguous command. In the latter case, $\overline{CS}$ needs not to be made high.

Note 7FH (μPD6464A), FFH (μPD6465)

3.4.1 When 2-byte contiguous command end code is not used

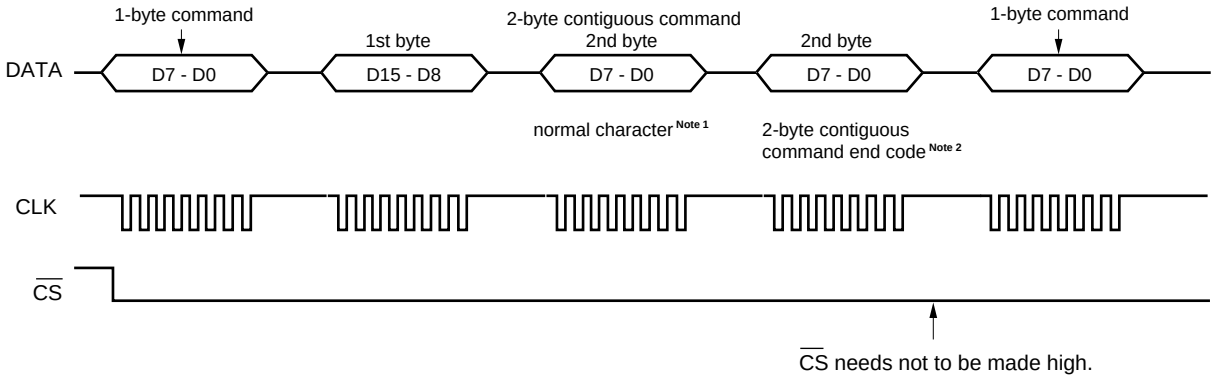
Example 1-byte command → 2-byte contiguous command → 1-byte command



Note 00H-7EH (μPD6464A), 00H-FEH (μPD6465)

3.4.2 When 2-byte contiguous command end code is used

Example 1-byte command → 2-byte contiguous command → 1-byte command



Notes 1. 00H-7EH (μPD6464A), 00H-FEH (μPD6465)

2. 7FH (μPD6464A), FFH (μPD6465)

Remark Although the $\overline{CS}$ pin can remain low when the end code of the 2-byte contiguous command is used, making this pin high is recommended as a countermeasures against noise.

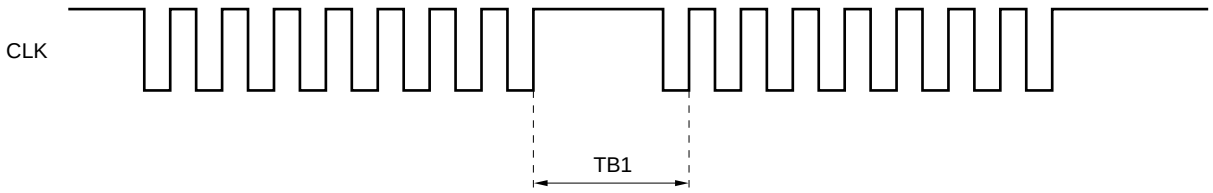
3.5 BUSY Period for Command Input

The BUSY period for command input is distinguished depending on whether a 1-byte, 2-byte, or 2-byte contiguous command is used.

When inputting 2-byte contiguous command, there are two timings as shown below, (1) Not transferring 2-byte contiguous command in $\overline{\text{Vsync}}$ period with detecting $\overline{\text{Vsync}}$ and (2) Transferring 2-byte contiguous command in $\overline{\text{Vsync}}$ period without detecting $\overline{\text{Vsync}}$.

When inputting commands in succession, observe the following timing:

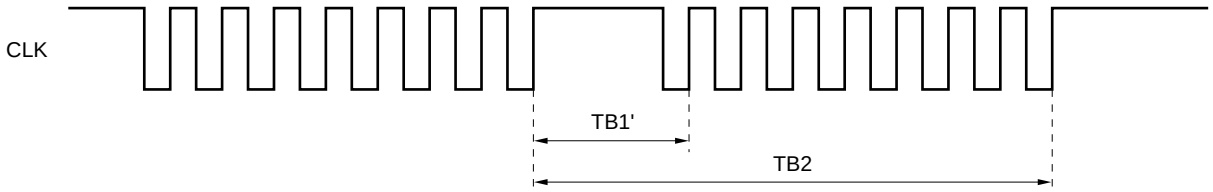
3.5.1 When inputting 1-byte or 2-byte command



Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Command continuous input enable time 1	TB1	1-byte or 2-byte command	2.0			μs

3.5.2 When inputting 2-byte contiguous command

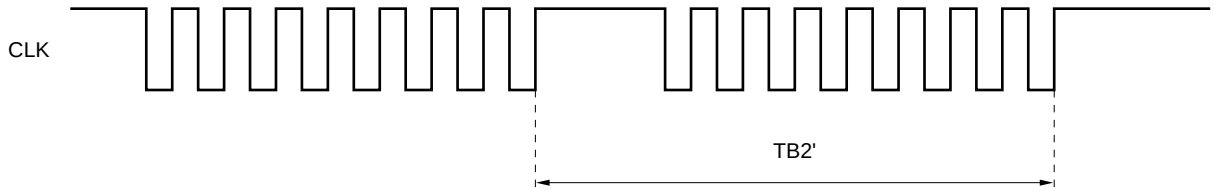
(1) Not transferring 2-byte contiguous command in $\overline{\text{Vsync}}$ period with detecting $\overline{\text{Vsync}}$ (command continuous input enable time 2 = TB2)



Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Command continuous input enable time 2	TB2	2-byte contiguous command (= video RAM write command)	Display ON	TB1' + (21/f_{OSC}) × S_1 + T_{HWL1}			μs
			Display OFF	TB1' + (21/f_{OSC}) × S_1			

Remark f_{OSC} : clock frequency of LC oscillation
S_1 : character size
T_{HWL1} : $\overline{\text{Hsync}}$ width
TB1' ≥ 2.0 μs

(2) Transferring 2-byte contiguous command in $\overline{\text{Vsync}}$ period without detecting $\overline{\text{Vsync}}$ (command continuous input enable time 2' = TB2')



Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Command continuous input enable time 2'	TB2'	2-byte contiguous command (= video RAM write command), Display ON	$(21/f_{OSC}) \times S_2 + T_{HWL2}$			μs

Remark f_{OSC} : clock frequency of LC oscillation
S_2 : character size of the first line
T_{HWL2} : $\overline{\text{Hsync}}$ period

4. ADJUSTING

This section describes how to adjust each circuit of the μPD6464A, 6465. When performing adjustment, the TEST pin (pin 19) must be connected to V_{CC}.

4.1 Adjusting Oscillation Frequency

4.1.1 Adjusting ×4 multiplier and crystal oscillation frequency

The μPD6464A, 6465 generate the internal video signal by means of quadruple oscillation of $4f_{SC}$ or crystal oscillation.

The oscillation frequency of $4f_{SC}$ can be output from the $\overline{VSYO}$ pin (pin 16) by using the test mode command.

Adjustment

- Connect the TEST pin (pin 19) to V_{CC} (normally, connect this pin to GND).
- Input the following command. The quadrupled or crystal oscillation frequency will be output from the $\overline{VSYO}$ pin (pin 16). To clear the test mode, either transfer the test mode clear command, or connect the TEST pin to GND.
- In this case, the $\overline{VSYO}$ pin does not function as a vertical synchronization signal output pin.
- Adjust the frequency with a capacitor (or coil), connected to XOSI pin (pin 12), shown in **8. APPLICATION CIRCUIT DIAGRAM** using a frequency counter.

Crystal oscillation frequency output command (2-byte command)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1

4.1.2 Adjusting LC oscillation frequency (dot clock)

The μPD6464A, 6465 create the dot clock of characters by means of LC oscillation.

The LC oscillation frequency can be output from the $\overline{HSYO}$ pin by using the test mode command, in the same manner as when adjusting the crystal oscillation frequency described in 4.1.1.

Adjustment

- Connect the TEST pin (pin 19) to V_{CC} (normally, connect this pin to GND).
- Input the following command. The LC oscillation frequency will be output from $\overline{HSYO}$ pin (pin 15). To adjust the LC oscillation frequency, turn OFF display. When display is ON and while $\overline{Hsync}$ is low, oscillation is stopped and the accurate oscillation frequency cannot be obtained (when using a frequency counter).
  To clear the test mode, either transfer the test mode clear command, or connect the TEST pin to GND.
- In this case, the $\overline{HSYO}$ pin does not function as a horizontal synchronization signal output pin.
- Adjust the frequency with a trimmer capacitor (or coil), connected to OSC_{IN} pin (pin 6) shown in **8. APPLICATION CIRCUIT DIAGRAM** using a frequency counter.

LC oscillation frequency output command (2-byte command)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1

4.2 Test Mode Clear Command

The command that clears the test mode is as follows:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Caution Be sure to connect the TEST pin to V_{CC} when performing the above adjustment. Be sure to connect the TEST pin to GND after adjustment.

★ 4.3 Clamp Level of Video Signal

Match the clamp level of the composite video signal input to the μPD6464A, 6465 with the internal video signal level of the μPD6464A, 6465. Otherwise, the character level in the external video signal mode will differ from that in the internal video signal mode.

Adjustment

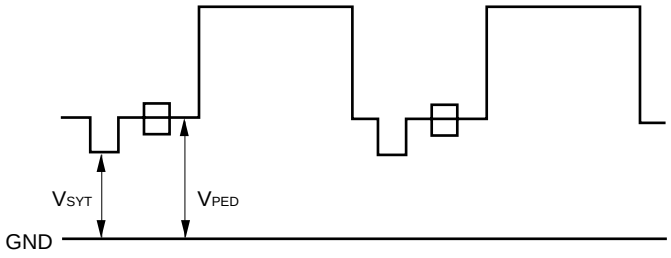
The internal video signal level of the μPD6464A, 6465 is set by the voltage applied to the V_{CNT} pin and an "output level control command".

The amplitude level of the internal video signal, sync-chip level, and pedestal level can be set in the following combination:

V_{CNT} Pin Voltage	Specified by Output Level Control Command	Internal Video Signal Amplitude Level (V_{DD} = 5.0 typ.)	Sync-Chip Level (V_{DD} = 5.0 typ.) (V_{SYT})	Pedestal Level (V_{DD} = 5.0 typ.) (V_{PED})
2.5 V	Selects 1 V_{p-p}	1 V_{p-p}	1 V	1.29 V
5.0 V	Selects 2 V_{p-p}	2 V_{p-p}	1 V	1.58 V

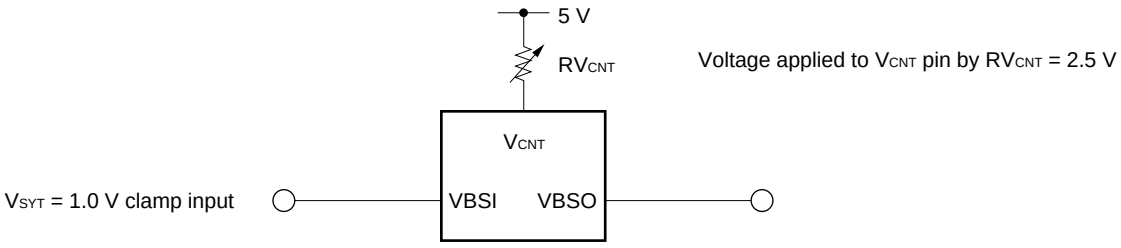
Adjust the sync-chip and pedestal levels of the external video signal to the same level of the internal video signal by using a variable resistor (pin 23) shown in **8. APPLICATION CIRCUIT DIAGRAM**. When setting the video amplitude level to 1 V_{p-p}, connecting a variable resistor to the V_{CNT} pin is recommended to adjust the internal video signal level (when setting the video signal to 2 V_{p-p}, connect the V_{CNT} pin to the power supply (5 V)).

★ **V_{SYT} and V_{PED} levels of composite video signal**



Match the level output from the VBSI pin in the external video signal mode with the level output from the same pin in the internal video signal mode.

Input level in external video signal mode (when video signal of 1 V_{p-p} is input)



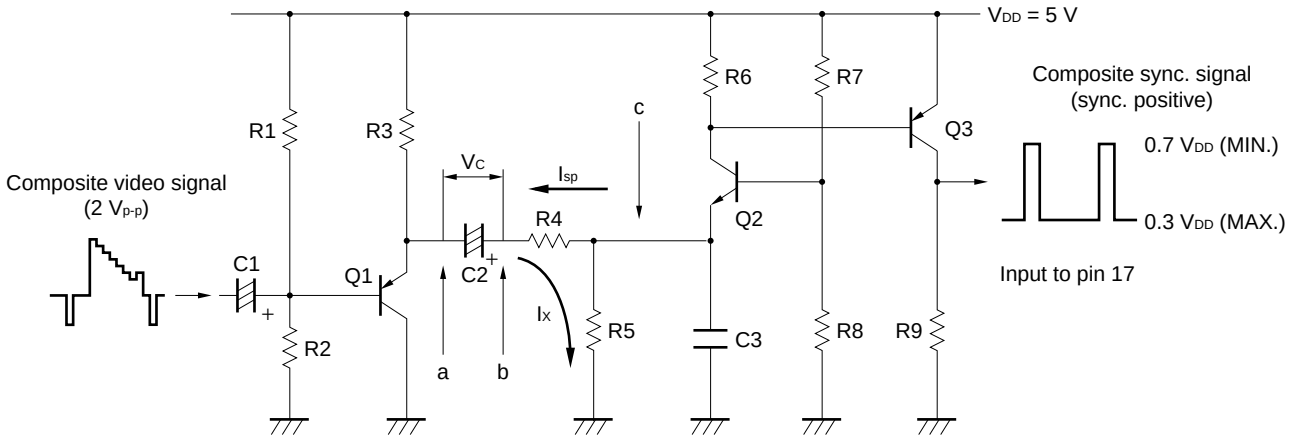
To input an external video signal with an amplitude of 2 V_{p-p}, input a 1.0-V clamp signal to V_{SYT}, apply 5.0 V to the V_{CNT} pin, and set the amplitude of 2 V_{p-p} by using the “output level control command”.

★ 5. COMPOSITE SYNC. SIGNAL SEPARATION CIRCUIT

An example of composite sync. signal separation circuit is shown in Figure 5-1.

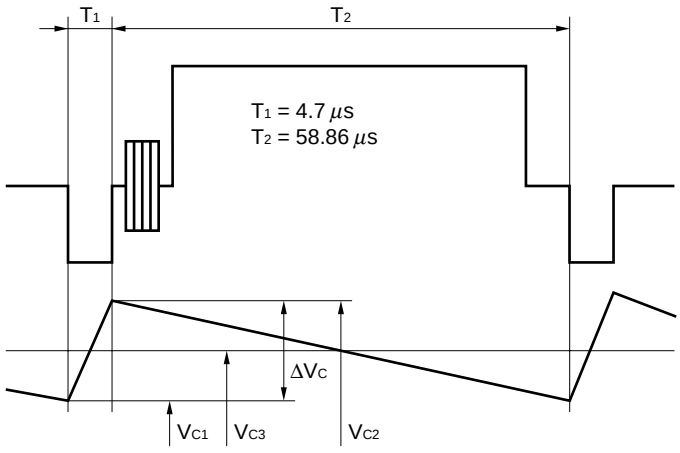
Figure 5-1. Composite Sync. Signal Separation Circuit

(a) Example of Composite Sync. Signal Separation Circuit



R1 = 5.1 kΩ, R2 = 1.2 kΩ, R3 = 1 kΩ, R4 = 220 Ω, R5 = 100 kΩ, R6 = 10 kΩ, R7 = 1 kΩ, R8 = 2.2 kΩ, R9 = 10 kΩ, C1 = 10 μF, C2 = 1 μF, C3 = 1000 pF

(b) Image of sync. signal separation waveform



The slice level (V_S) of Figure 5-1 (a) is defined as follows.

$$V_S = 2.7 \times \frac{R5}{R4} \times \frac{T_2}{T_1} \fallingdotseq 74 \text{ mV}$$

When V_S is small, it is suited for horizontal sync. separation, but is against to vertical sync. separation. And when V_S is large, edge noise of horizontal sync. separation causes a synchronization error (jitter). Therefore, the constant of each element in the circuit should be optimized according to input signal's characteristics.

The C2 capacitance should be specified as a sufficient larger value compared to charge/discharge current. If the value overly exceeds the suitable value, however, excessive response characteristics will be inferior, falling to trace rapid average-picture-level (APL) fluctuation of input signal. In the circuit shown in Figure 5-1 (a), a capacitor is connected to the composite video signal input portion for measurement. However, this makes it hard to trace APL fluctuation. Therefore, in designing an actual circuit, insert a sync-chip clamp in front of Q1 in Figure 5-1 (a). to stabilizes the potential of a synchronization signal, for tracing APL fluctuation.

Caution In the circuit of Figure 5-1 (a), the width of the $\overline{\text{Hsync}}$ synchronization signal that is included in the composite synchronization signal after separation may be wider than that of the $\overline{\text{Hsync}}$ synchronization signal that is included in the input video signal, because of its circuit configuration. Therefore, the width of the $\overline{\text{Hsync}}$ synchronization signal during a command continuous input enable time (refer to 3.5 BUSY Period for Command Input) should be the same as that of the $\overline{\text{Hsync}}$ synchronization signal included in Csync after separation in the circuit of Figure 5-1 (a).

6. CHARACTER PATTERN DATA

The only difference between the μPD6464ACS-001 and μPD6464AGT-101 is the package. The character patterns in the character ROMs of both the models are the same. The same applies to the μPD6465CS-001 and the μPD6465GT-101. Both the μPD6464ACS-001 and μPD6464AGT-101 can display 128 types of alphanumeric characters and character patterns such as Kanji, Hiragana, and Katakana. The μPD6465CS-001 and μPD6465GT-101 can display 256 types of them.

The contents of the character ROM (character design) can be changed by mask code option. However, the characters at addresses 7EH and 7FH (μPD6464A)/FEH and FFH (μPD6465) are fixed to [Display Off Data] and [2-byte contiguous command end code], respectively, and no character patterns can be set to these addresses.

Although 10H (μPD6464A)/6FH (μPD6465) (Blank Data) and 7EH (μPD6464A)/FEH (μPD6465) (Display Off Data) of the NEC's standard model are represented in the same manner in the page showing the character patterns (i.e., these are shown as characters without dots), they have the following differences:

Video Signal Mode	Character Code[Note]	Display of Part to Which Character Is Written in Each Mode		
		Background		
		No background	Black-on-white	Black filling
External video signal mode	Blank Data	Displays external video signal	Displays background	Displays background
	Display Off Data		Displays external video signal (without background)	Displays external video signal (without background)
Internal video signal mode	Blank Data	Displays internal video signal color	Displays background	Displays background
	Display Off Data		Displays internal video signal color	Displays internal video signal color

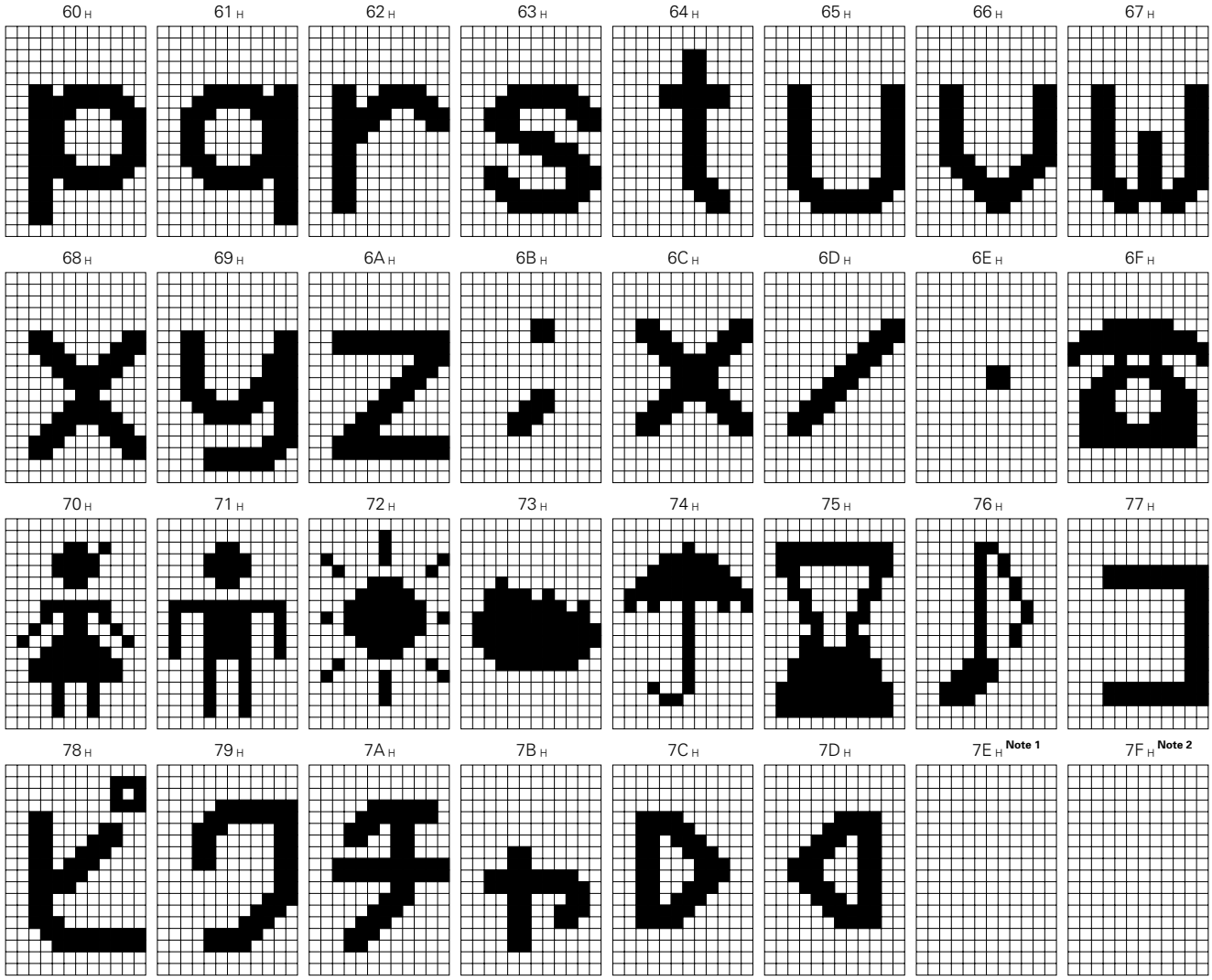
You cannot specify Display Off Data for addresses other than 7EH (μPD6464A)/FEH (μPD6465) when using a mask option. Blank Data, however, can be specified at any address from 00H to 7DH (μPD6464A)/FDH (μPD6465) (address 7FH (μPD6464A)/FFH (μPD6465) cannot be used because it contains the end code for second-byte continuous input).

The character patterns of the μPD6464ACS-001 and GT-101/μPD6465CS-001 and GT-101 (NEC's standard models) are shown on the following pages.

6.1 Standard Character Patterns of the μPD6464A

Note Blank Data

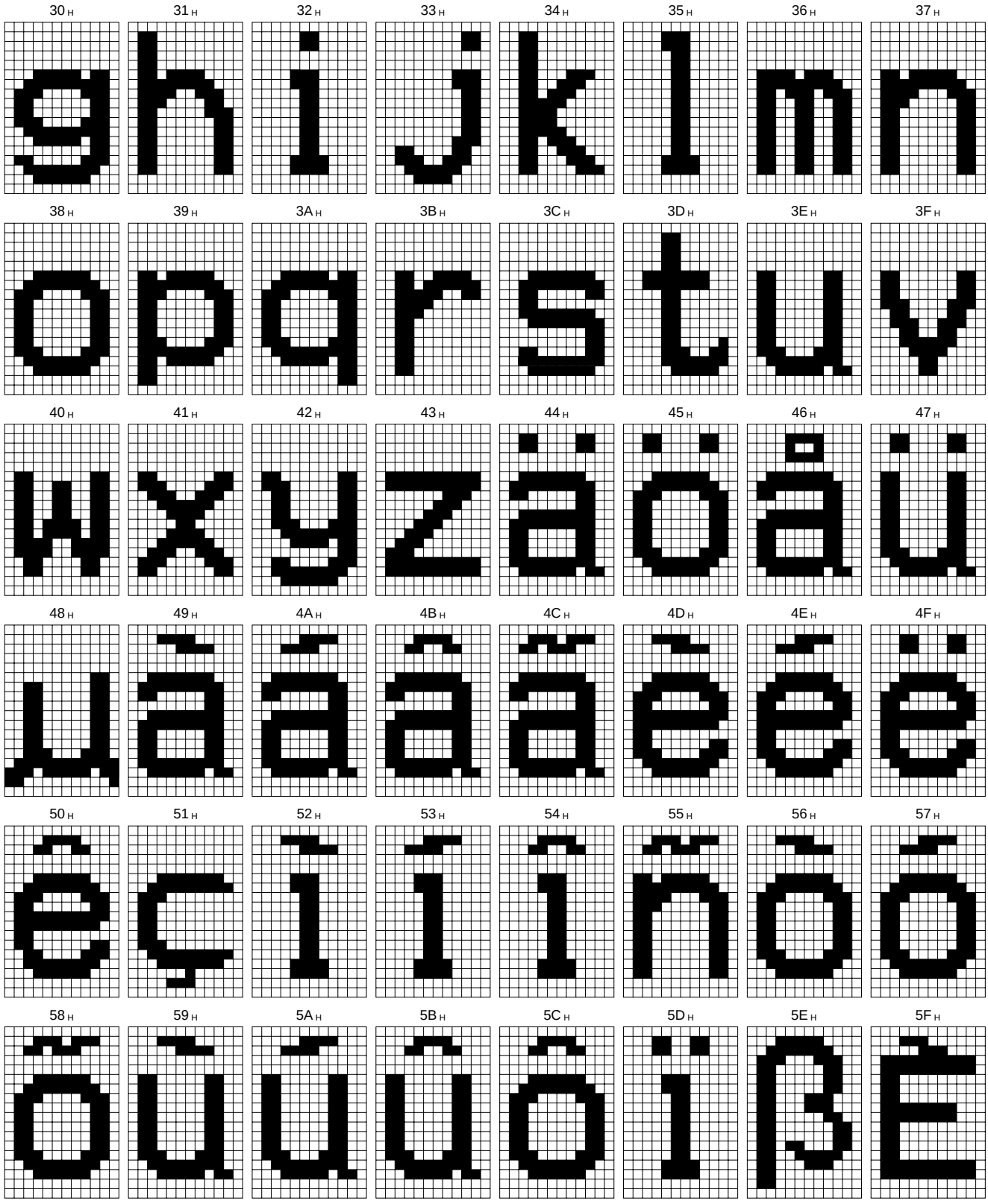

30H 31H 32H 33H 34H 35H 36H 37H
38H 39H 3AH 3BH 3CH 3DH 3EH 3FH
40H 41H 42H 43H 44H 45H 46H 47H
48H 49H 4AH 4BH 4CH 4DH 4EH 4FH
50H 51H 52H 53H 54H 55H 56H 57H
58H 59H 5AH 5BH 5CH 5DH 5EH 5FH



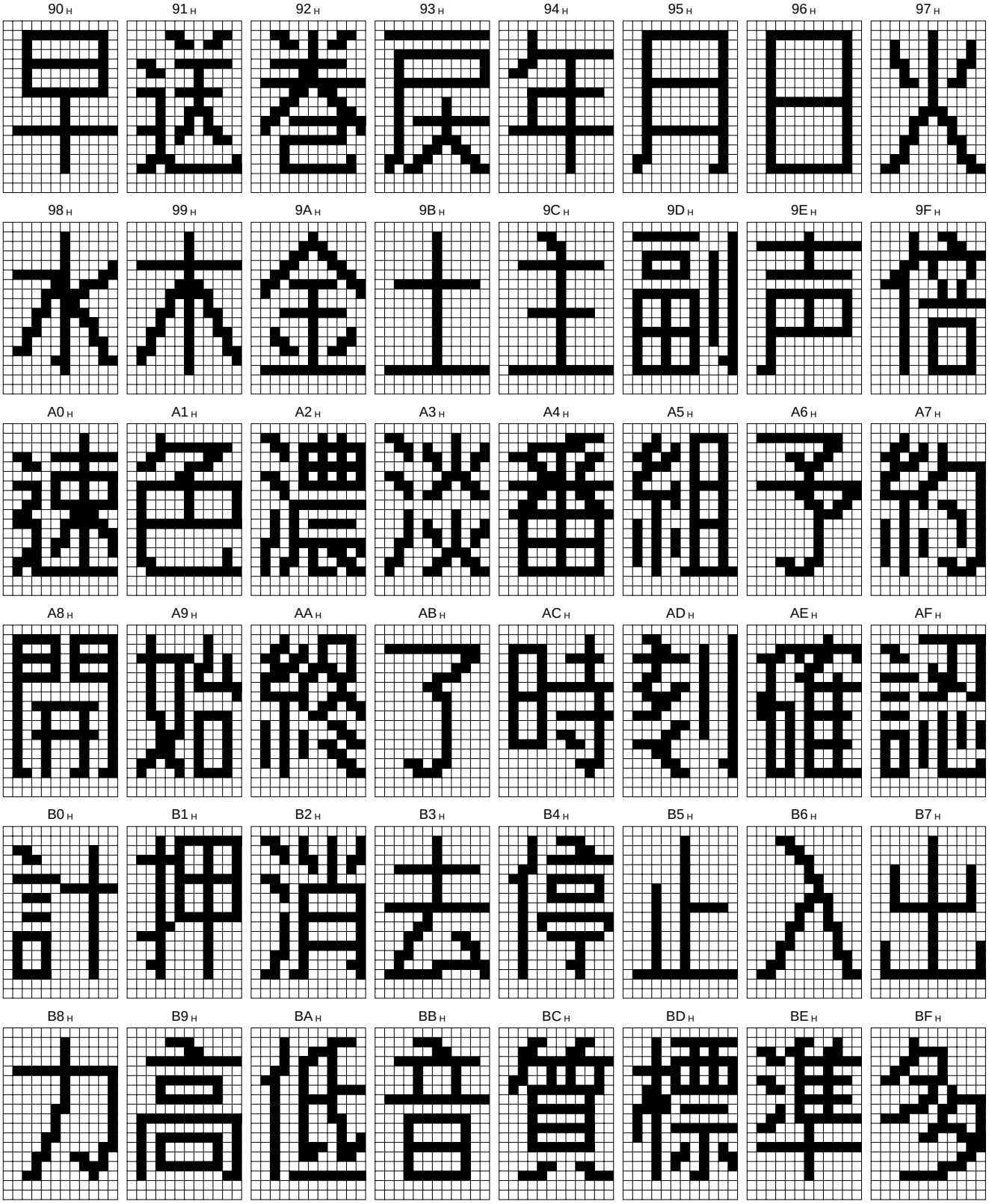
Notes 1. Display Off Data (character address fixed)

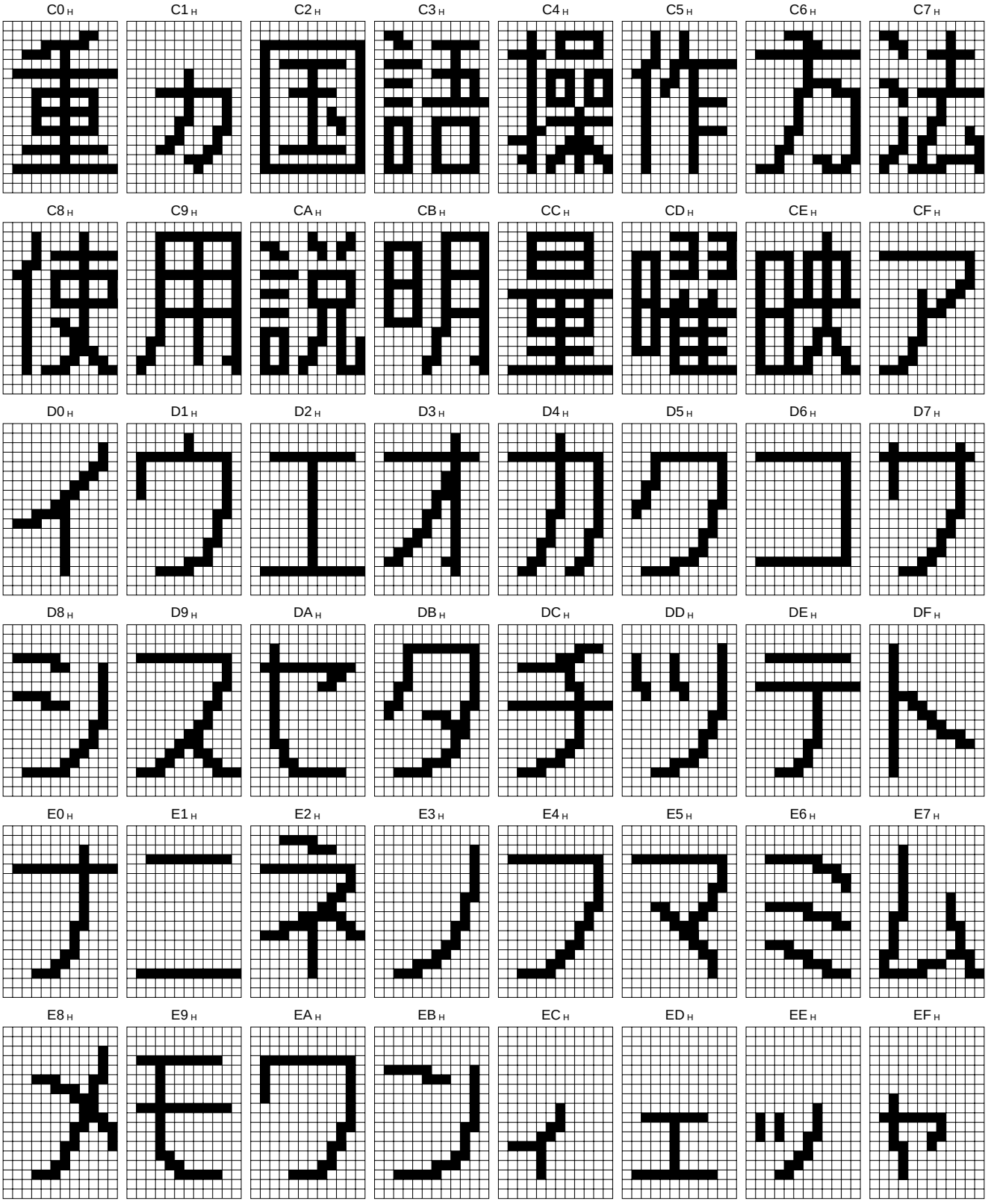
2. End code of 2-byte contiguous command (character address fixed)

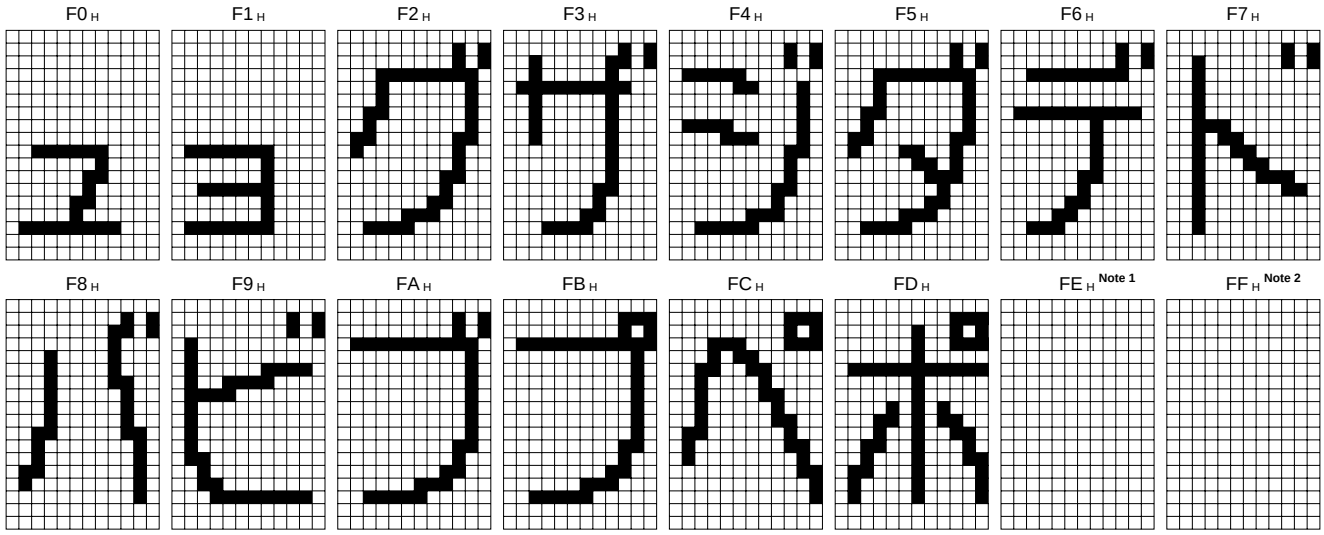
6.2 Standard Character Patterns of the μPD6465


30 H
31 H
32 H
33 H
34 H
35 H
36 H
37 H
38 H
39 H
3A H
3B H
3C H
3D H
3E H
3F H
40 H
41 H
42 H
43 H
44 H
45 H
46 H
47 H
48 H
49 H
4A H
4B H
4C H
4D H
4E H
4F H
50 H
51 H
52 H
53 H
54 H
55 H
56 H
57 H
58 H
59 H
5A H
5B H
5C H
5D H
5E H
5F H

Note Blank Data


90H
91H
92H
93H
94H
95H
96H
97H
98H
99H
9AH
9BH
9CH
9DH
9EH
9FH
A0H
A1H
A2H
A3H
A4H
A5H
A6H
A7H
A8H
A9H
AAH
ABH
ACH
ADH
AEH
AFH
B0H
B1H
B2H
B3H
B4H
B5H
B6H
B7H
B8H
B9H
BAH
BBH
BCH
BDH
BEH
BFH


C0 H
C1 H
C2 H
C3 H
C4 H
C5 H
C6 H
C7 H
C8 H
C9 H
CA H
CB H
CC H
CD H
CE H
CF H
D0 H
D1 H
D2 H
D3 H
D4 H
D5 H
D6 H
D7 H
D8 H
D9 H
DA H
DB H
DC H
DD H
DE H
DF H
E0 H
E1 H
E2 H
E3 H
E4 H
E5 H
E6 H
E7 H
E8 H
E9 H
EA H
EB H
EC H
ED H
EE H
EF H



Notes 1. Display Off Data (character address fixed)

2. End code of 2-byte contiguous command (character address fixed)

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	μPD6464ACS, 6465CS	μPD6464AGT, 6465GT	Unit
Supply voltage	V_{DD}	7		V
Input pin voltage	V_{IN}	–0.3 to V_{DD} +0.3		V
Output pin voltage	V_{OUT}	–0.3 to V_{DD} +0.3		V
★ Permissible package power dissipation (T_A = 75 °C)	P_D	470	320	mW
Operating ambient temperature	T_A	–20 to +75		°C
Storage temperature	T_{stg}	–40 to +125		°C
Output current	I_O	±5		mA

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

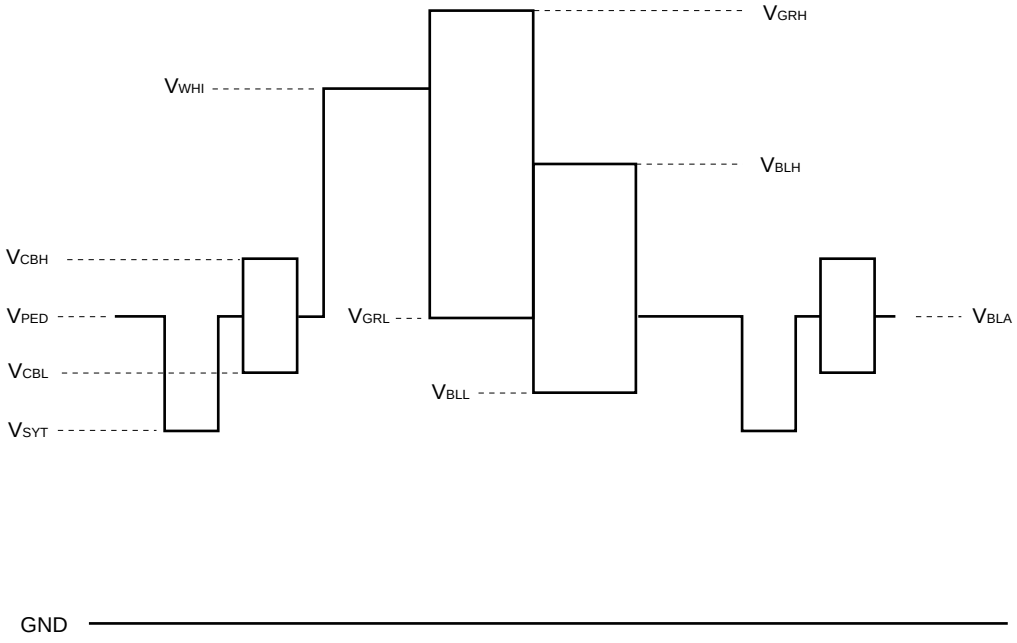
Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Operating ambient temperature	T_A		–20		+75	°C
LC oscillation frequency	f_{OSC}		4	7	8	MHz
Control input high level voltage	V_{CIH}	DATA, CLK, $\overline{CS}$, $\overline{PCL}$	3.5			V
Control input low level voltage	V_{CIL}	DATA, CLK, $\overline{CS}$, $\overline{PCL}$			1.5	V
Signal output high level voltage	V_{SOH}	I_{SOH}=–1mA, V_{DD}=5.0 V	4.5			V
Signal output low level voltage	V_{SOL}	I_{SOL}=1mA, V_{DD}=5.0 V			0.5	V
Internal signal level setting voltage	V_{VL}	V_{CNT}	2.5		V_{DD}	V
External video signal input voltage	V_i	VBSI	0		V_{DD}	V
Current consumption	I_{DD}	f_{OSC}=8MHz			20	mA

AC Characteristics (Unless otherwise specified, V_{DD} = 5 V, T_A = +25 ˚C)

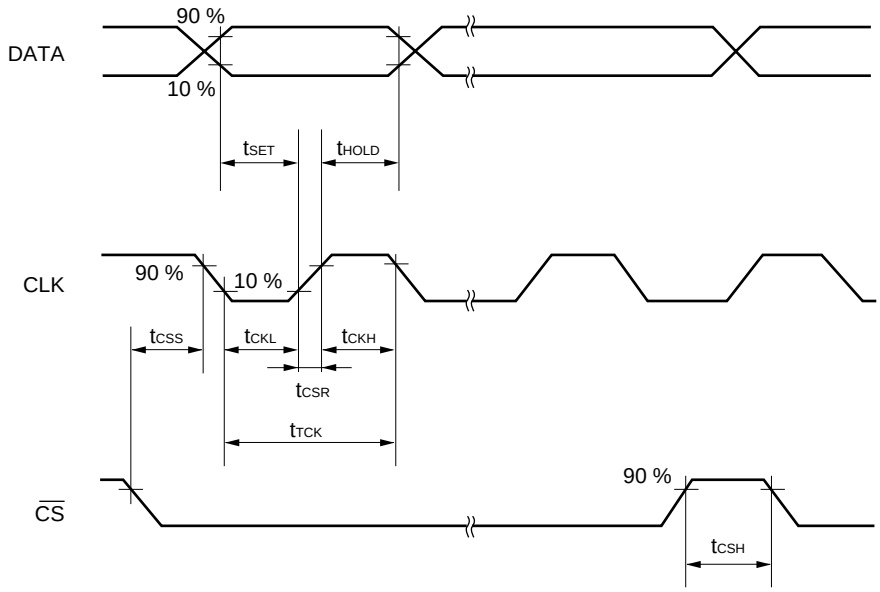
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Synchronization signal input pulse width	t_{HST}		4.0		9.0	μs
Pedestal level voltage	V_{PED}	VBSO, internal mode, V_{CNT} = 2.5 V, V_{SYT} = 1.0 V	1.03	1.29	1.55	V
Sync-chip level voltage	V_{SYT}		0.8	1.0	1.20	V
Color burst high level voltage 1	V_{CBH1}		1.15	1.44	1.73	V
Color burst low level voltage 1	V_{CBL1}		0.91	1.14	1.37	V
Color burst high level voltage 2	V_{CBH2}		1.20	1.50	1.80	V
Color burst low level voltage 2	V_{CBL2}		0.85	1.07	1.28	V
Black level voltage	V_{BLA}		1.03	1.29	1.55	V
Blue VBS high level voltage	V_{BLH}		1.26	1.58	1.90	V
Blue VBS low level voltage	V_{BLL}		0.88	1.11	1.34	V
Green VBS high level voltage	V_{GRH}		1.53	1.92	2.31	V
Green VBS low level voltage	V_{GRL}		1.03	1.29	1.55	V
White level voltage	V_{WHI}		1.45	1.82	2.19	V
Burst phase angle	ϕ_{BSC}	NTSC, internal mode	170	180	190	deg
Green phase angle	ϕ_G		215	225	235	deg
Blue phase angle	ϕ_B		350	0	10	deg
Burst phase angle	ϕ_{BSC1}	PAL1, internal mode	125	135	145	deg
Green phase angle	ϕ_{G1}		215	225	235	deg
Blue phase angle	ϕ_{B1}		350	0	10	deg
Burst phase angle	ϕ_{BSC2}	PAL2, internal mode	215	225	235	deg
Green phase angle	ϕ_{G2}		125	135	145	deg
Blue phase angle	ϕ_{B2}		350	0	10	deg
Crystal oscillation frequency 1	f_{XON1}	In NTSC mode		14.31818		MHz
Crystal oscillation frequency 2	f_{XON2}	In PAL, SECAM mode		17.734475		MHz
Crystal oscillation frequency 3	f_{XON3}	In PAL-M mode		14.302446		MHz
Crystal oscillation frequency 4	f_{XON4}	In PAL-N mode		14.328225		MHz
Character 90% level voltage	V90	V_{CNT} = 2.5 V, V_{SYT} = 1.0 V	1.53	1.92	2.31	V
Character 75% level voltage	V75		1.45	1.82	2.19	V
Background 0% level voltage	V0	V_{CNT} = 2.5 V, V_{SYT} = 1.0 V	1.03	1.29	1.55	V
f_{SC} input amplitude	f_{in}		300			mV_{p-p}

Concept of μPD6464A, 6465 internal video signal level



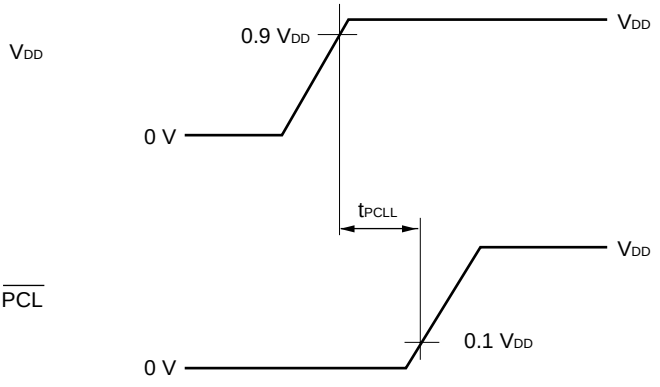
Recommended Operation Timing (T_A = –20 to +75 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Setup time	t_{SET}		200			ns
Hold time	t_{HOLD}		200			ns
Minimum clock low-level width	t_{CKL}		400			ns
Minimum clock high-level width	t_{CKH}		400			ns
Clock cycle	t_{TCK}		1.0			μs
$\overline{CS}$ setup time	t_{CSS}		400			ns
$\overline{CS}$ hold time	t_{CSH}		400			ns
CLK slew rate	t_{CSR}				100	ns



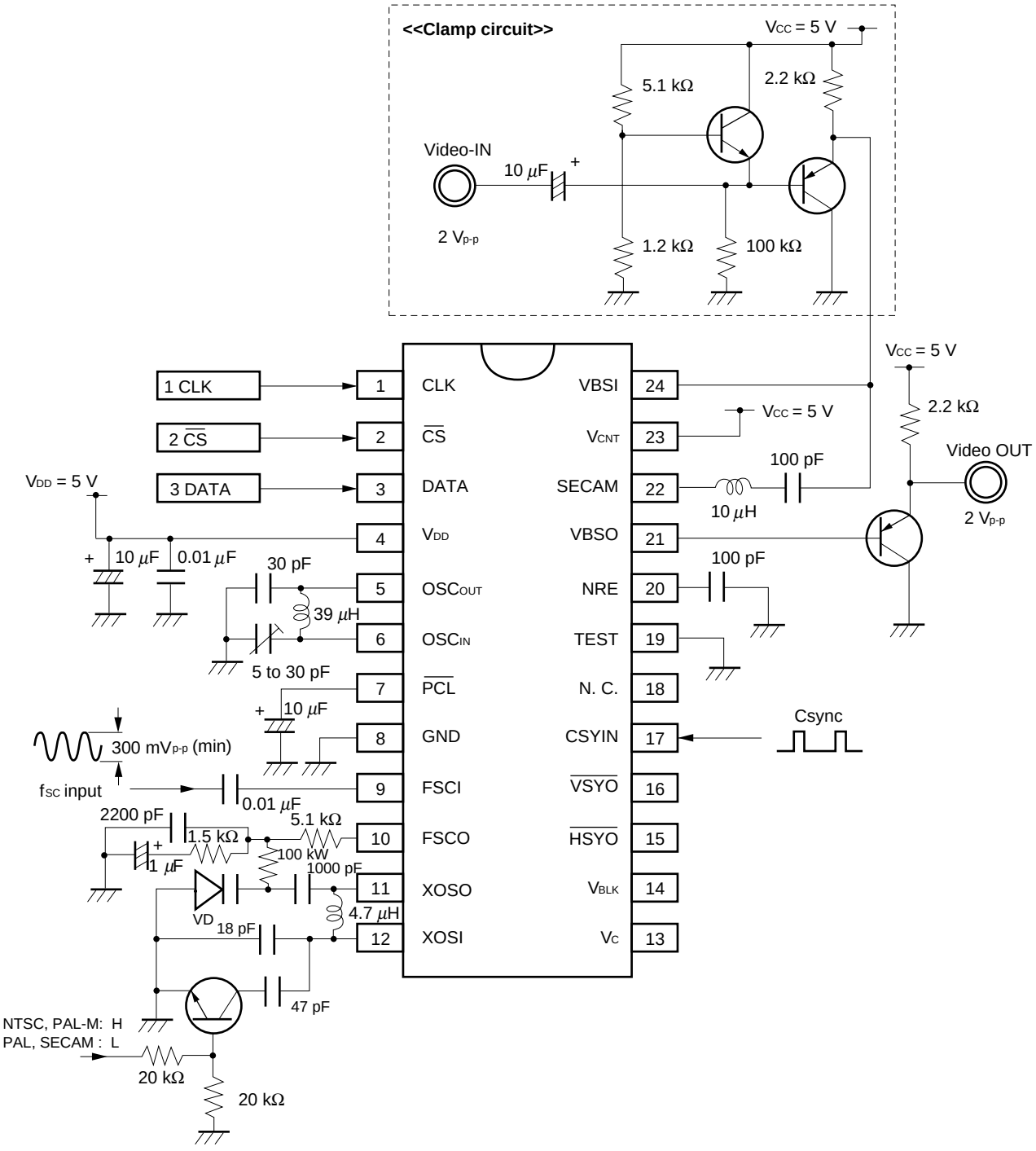
Power-ON Clear Specification

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{PCL}$ pin low-level hold period	t_{PCLL}		10			μs



8. APPLICATION CIRCUIT DIAGRAM

(1) ×4 multiplier oscillation



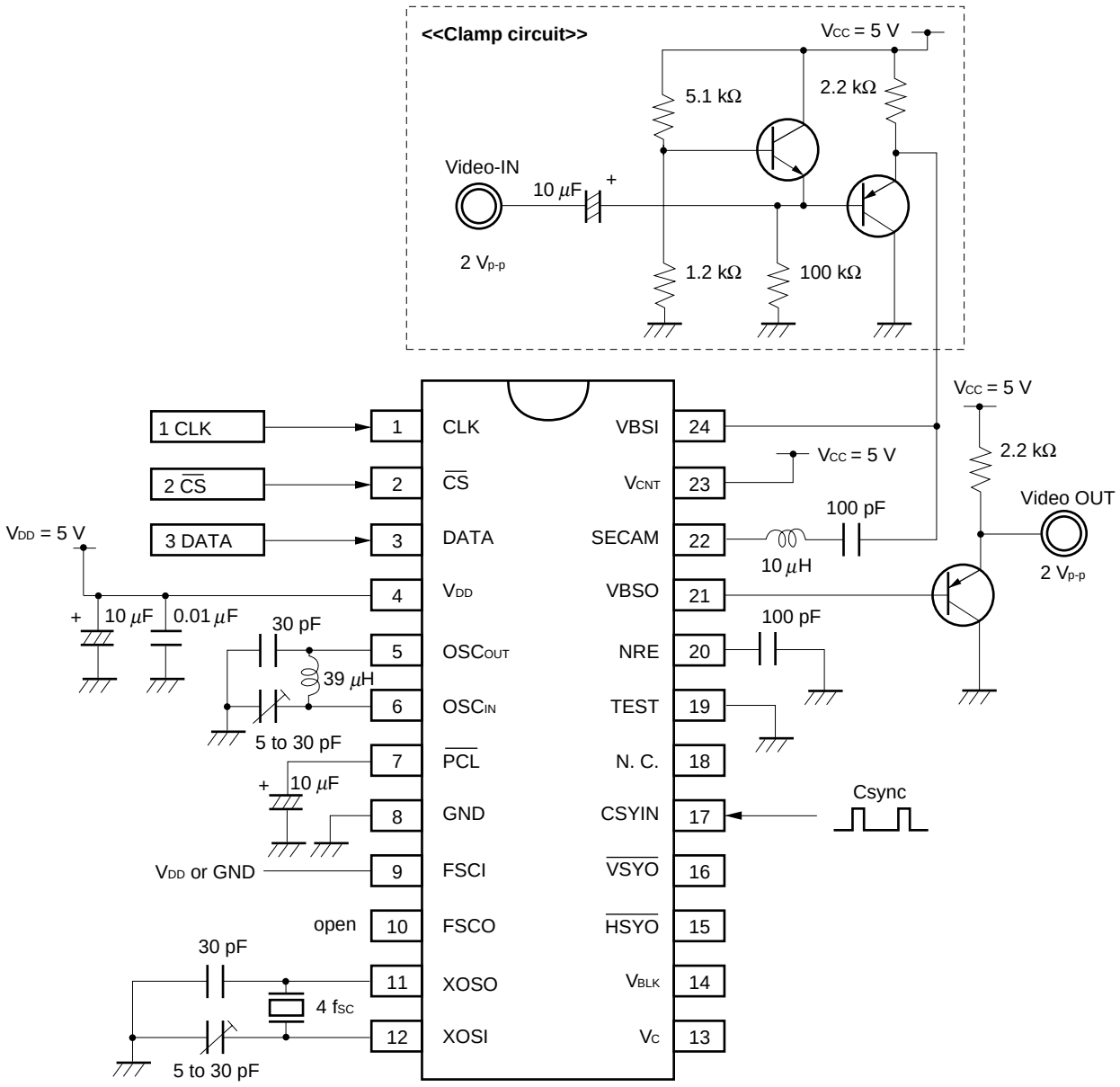
Cautions 1. The clamp circuit is not necessary when the sync-chip level (1 V DC) can be directly input to pin 24.

2. Pin 20 is connected so as to reject unwanted radiation.

3. This application circuit is assumed to input $2V_{p\text{-}p}$ video signals.

4. Product equivalent to 1SV163 can be used as a VD (Varactor diode).

★ **(2) 4fSC Crystal oscillation**



Cautions 1. The clamp circuit is not necessary when the sync-chip level (1 V DC) can be directly input to pin 24.

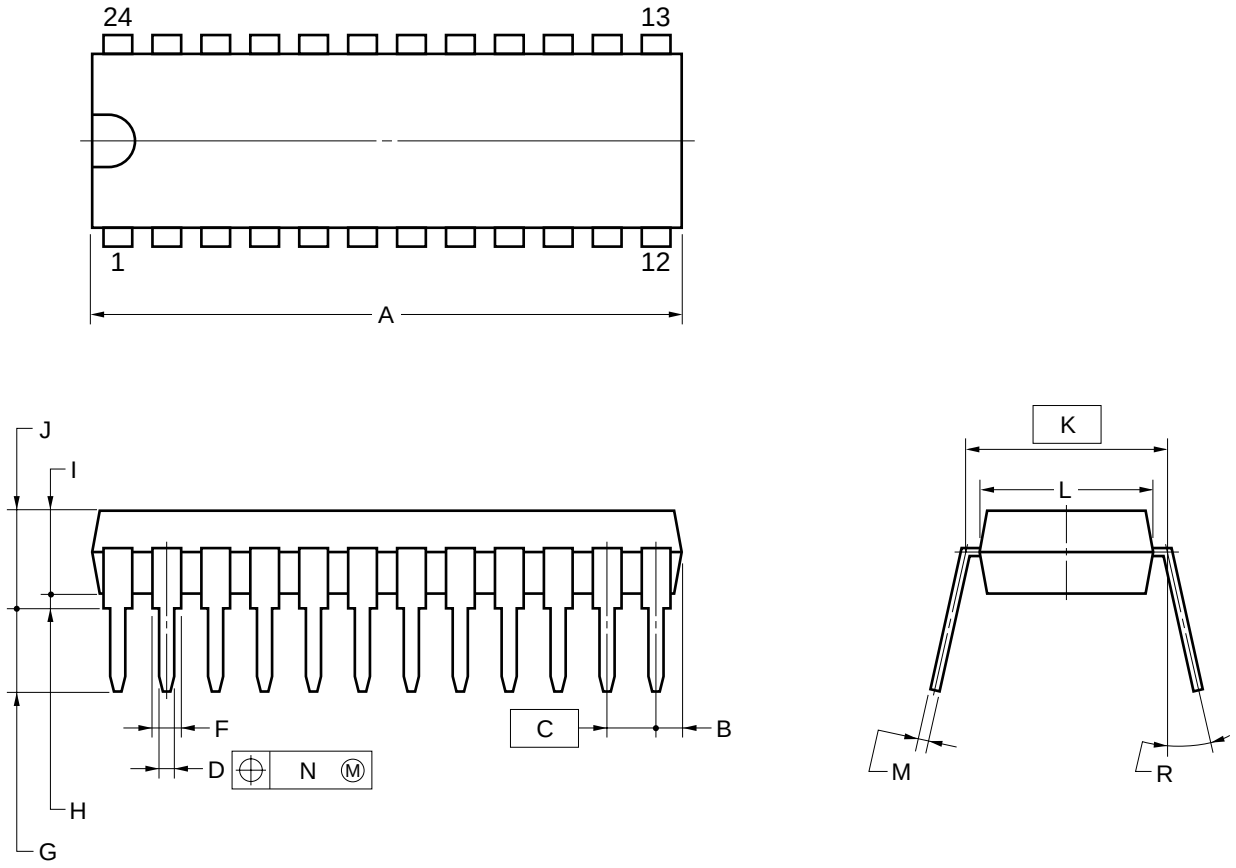
2. Pin 20 is connected so as to reject unwanted radiation.

3. This application circuit is assumed to input $2V_{p\text{-}p}$ video signals.

4. Connect pin 9 to GND or V_{DD} (do not open). Pin 10 should be open.

9. PACKAGE DRAWINGS

24 PIN PLASTIC SHRINK DIP (300 mil)



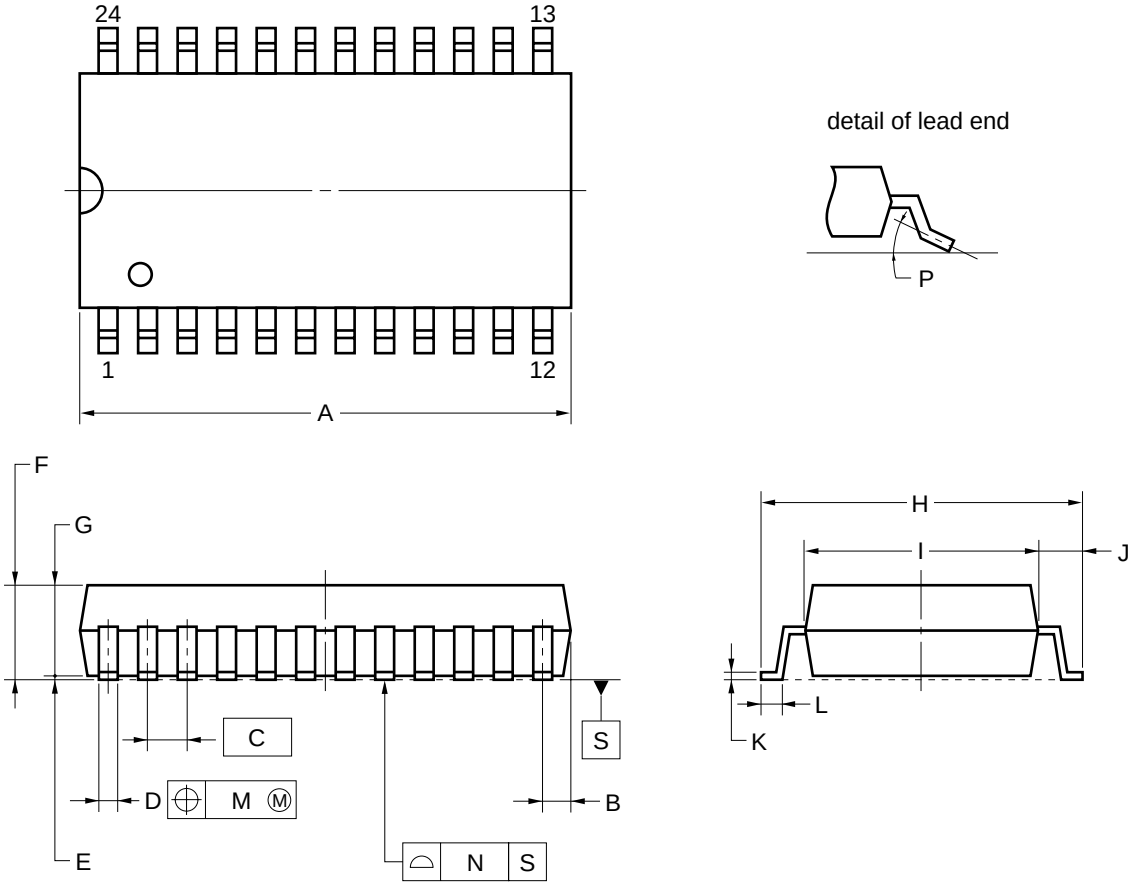
NOTES

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
3. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	21.95±0.2	$0.864^{+0.009}_{-0.008}$
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	3.45±0.2	$0.136^{+0.008}_{-0.009}$
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4±0.2	0.252±0.008
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

S24C-70-300B-2

24 PIN PLASTIC SOP (375 mil)



NOTE

1. Controlling dimention — millimeter.

2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$15.3^{+0.41}_{-0.2}$	$0.602^{+0.017}_{-0.008}$
B	0.87 MAX.	0.035 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	$0.017^{+0.003}_{-0.004}$
E	0.125±0.075	0.005±0.003
F	2.9 MAX.	0.115 MAX.
G	2.50±0.2	$0.098^{+0.009}_{-0.008}$
H	10.3±0.2	$0.406^{+0.008}_{-0.009}$
I	7.2±0.2	$0.283^{+0.009}_{-0.008}$
J	1.6±0.2	0.063±0.008
K	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P24GT-50-375B-2

10. RECOMMENDED SOLDERING CONDITIONS

Solder the μPD6464A, 6465 under the conditions shown below.

For the details of the recommended soldering conditions, refer to **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For other soldering methods and conditions, consult NEC.

Surface mount devices

μPD6464AGT-×××: 24-pin plastic SOP (375 mil)
μPD6465GT-×××: 24-pin plastic SOP (375 mil)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 235 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 2 times,	IR35-00-2
Vapor Phase Soldering	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 2 times,	VP15-00-2
★ Wave Soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature),	WS60-00-1
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Through-hole devices

μPD6464ACS-×××: 24-pin plastic shrink DIP (300 mil)
μPD6465CS-×××: 24-pin plastic shrink DIP (300 mil)

Process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each lead).

Caution For through-hole devices, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

M4 96.5