Chapter 3

TSP50C0x/1x Electrical Specifications

This chapter contains electrical and timing information for the TSP50C0x/1x family devices, organized according to device category.

Topic **Page**

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range†

Supply voltage range, V_{DD} (see Note 1) ..... –0.3 V to 8 V
Input voltage range, V_I (see Note 1) ..... –0.3 V to V_{DD} + 0.3 V
Output voltage range, V_O (see Note 1) ..... –0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range (TSP50C04/06/10/11/12/13/14) ..... –30°C to 125°C
Storage temperature range (TSP50C19 only) ..... 0°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to ground.

3.2 Recommended Operating Conditions

The following table contains recommended operating characteristics for the TSP50C0x/1x family.

Table 3–1. Recommended Operating Conditions

			Min	Nom	Max	Unit
V_{DD}	Supply voltage†		4		6.5	V
V_{IH}	High-level input voltage	V_{DD} = 4 V	3		4	V
		V_{DD} = 5 V	3.8		5	
		V_{DD} = 6 V	4.5		6	
V_{IL}	Low-level input voltage	V_{DD} = 4 V	0		0.8	V
		V_{DD} = 5 V	0		1	
		V_{DD} = 6 V	0		1.3	
T_A	Operating free-air temperature	Device functionality	0		70	°C
		LCD reference spec (TSP50C12 only)	10		40	
f_{osc}	Clock frequency	10-kHz speech sample rate‡		9.6		MHz
		8-kHz speech sample rate‡		7.68		
f_{clock}	ROM clock frequency	External ROM mode interface to TSP60C18 speech ROMs		$f_{osc}/4$		MHz

† Unless otherwise noted, all voltages are with respect to V_{SS}.
‡ Speech sample rate = $f_{osc}/960$.

3.3 Timing Requirements

The following tables give timing requirements and the following figures give timing waveforms for the TSP50C0x/1x family.

Table 3–2. D/A Options Timing Requirements

			Min	Nom	Max	Unit
t_r	Rise time, PAx, PBx, D/A options 1, 2	V_{DD} = 4 V, C_L = 100 pF		22		ns
t_f	Fall time, PAx, PBx, D/A options 1, 2			10		ns

Table 3–3. Initialization Timing Requirements

		Min	Max	Unit
t_{INIT}	$\overline{INIT}$ pulsed low while the TSP50C0x/1x has power applied	1		µs

Figure 3–1. Initialization Timing Diagram

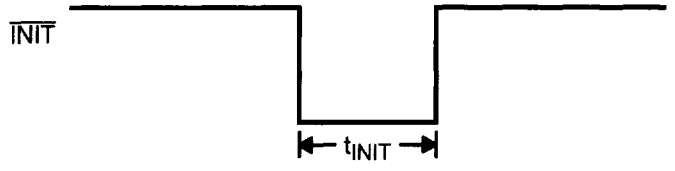


Table 3–4. Write Timing Requirements (Slave Mode)

		Min	Max	Unit
$t_{su(PB1)}$	Setup time, PB1 low before PB0 goes low	20		ns
$t_{su(d)}$	Setup time, data valid before PB0 goes high	100		ns
$t_{h(PB1)}$	Hold time, PB1 low after PB0 goes high	20		ns
$t_{h(d)}$	Hold time, data valid after PB0 goes high	30		ns
t_w	Pulse duration, PB0 low	100		ns
t_r	Rise time, PB0		50	ns
t_f	Fall time, PB0		50	ns

Figure 3–2. Write Timing Diagram (Slave Mode)

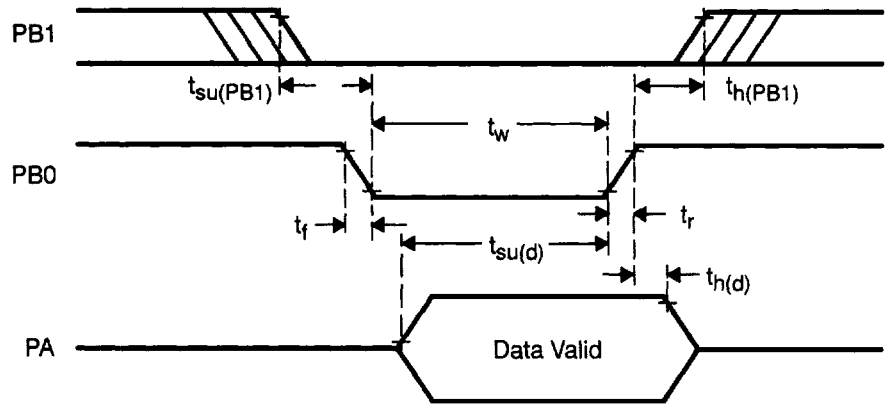


Table 3–5. Read Timing Requirements (Slave Mode)

		Min	Max	Unit
$t_{su(PB1)}$	Setup time, PB1 before PB0 goes low	20		ns
$t_{h(PB1)}$	Hold time, PB1 after PB0 goes high	20		ns
t_{dis}	Output disable time, data valid after PB0 goes high	0	30	ns
t_w	Pulse duration, PB0 low	100		ns
t_r	Rise time, PB0		50	ns
t_f	Fall time, PB0		50	ns
t_d	Delay time for PB0 low to data valid		50	ns

Figure 3–3. Read Timing Diagram (Slave Mode)

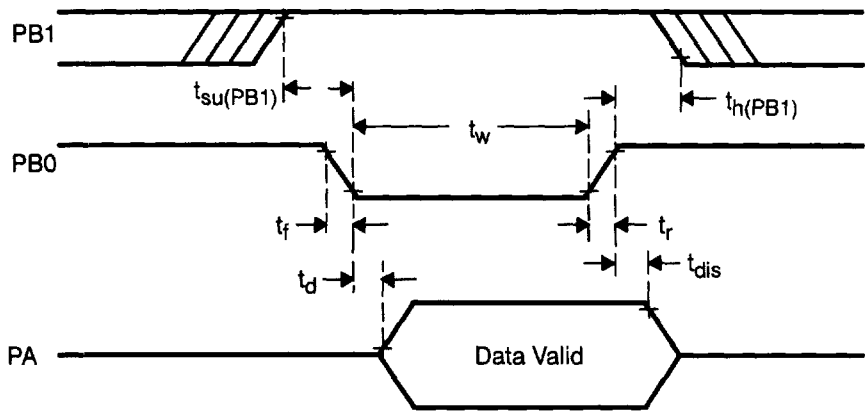
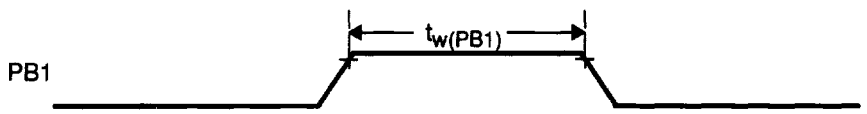


Table 3–6. External Interrupt Timing Requirements

		Min	Max	Unit
$t_{w(PB1)}$ Pulse duration, before PB1 goes low	f_{clock} = 7.6 MHz	2		µs
	f_{clock} = 9.6 MHz	2.5		µs

Figure 3–4. External Interrupt Timing Diagram



3.4 TSP50C10/11 Electrical Characteristics

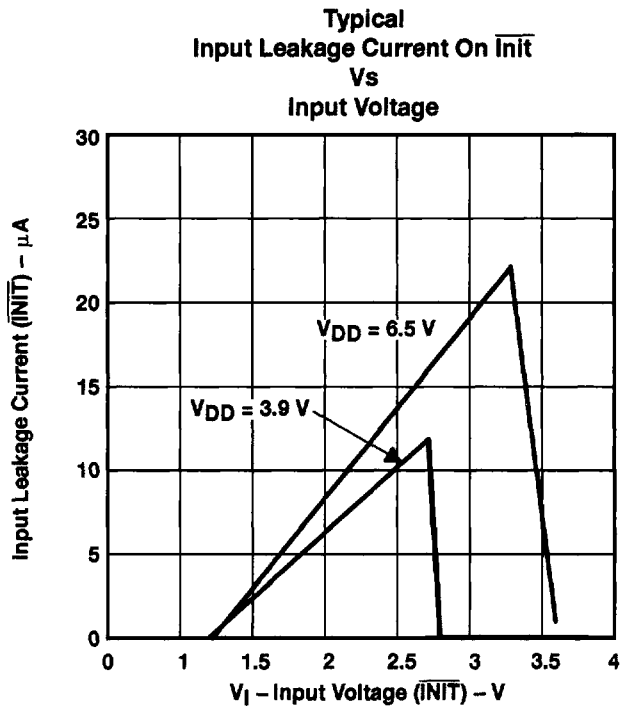
Table 3–7 gives specifications and the Figure 3–5 gives the input leakage current that applies to the TSP50C10 and TSP50C11.

Table 3–7. TSP50C10/11 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (unless otherwise noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
V_{T+}	Positive-going threshold voltage ($\overline{INIT}$)	V_{DD} = 4.5 V			2.7		V
		V_{DD} = 6 V			3.65		
V_{T-}	Negative-going threshold voltage ($\overline{INIT}$)	V_{DD} = 4.5 V			2.3		V
		V_{DD} = 6 V			3.15		
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) (INIT)	V_{DD} = 4.5 V			0.4		V
		V_{DD} = 6 V			0.5		
I_{lkg}	Input leakage current (except for OSC1, $\overline{INIT}$ see Figure 3–5)					1	µA
$I_{standby}$	Standby current ($\overline{INIT}$ low)					10	µA
I_{DD}†	Supply current	D/A option 1, 2, or 3			5		mA
I_{OH}	High-level output current (PAx, PBx, D/A options 1, 2)	V_{DD} = 4 V,	V_{OH} = 3.5 V	–4	–6		mA
		V_{DD} = 5 V,	V_{OH} = 4.5 V	–5	–7.5		
		V_{DD} = 6 V,	V_{OH} = 5.5 V	–6	–9.2		
		V_{DD} = 4 V,	V_{OH} = 2.67 V	–8	–13		mA
		V_{DD} = 5 V,	V_{OH} = 3.33 V	–14	–20		
		V_{DD} = 6 V,	V_{OH} = 4 V	–20	–29		
I_{OL}	Low-level output current (PAx, PBx, D/A options 1, 2)	V_{DD} = 4 V,	V_{OL} = 0.5 V	10	17		mA
		V_{DD} = 5 V,	V_{OL} = 0.5 V	13	20		
		V_{DD} = 6 V,	V_{OL} = 0.5 V	15	25		
		V_{DD} = 4 V,	V_{OL} = 1.33 V	20	32		mA
		V_{DD} = 5 V,	V_{OL} = 1.67 V	30	52		
		V_{DD} = 6 V,	V_{OL} = 2 V	41	71		
	Pullup resistance	Resistors selected with software and connected between pin and V_{DD}		15	30	60	kΩ

† Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

Figure 3–5. Typical Input Leakage Current on $\overline{INIT}$



3.5 TSP50C12 Electrical Characteristics

Table 3–8 gives specifications that apply to the TSP50C12.

Table 3–8. TSP50C12 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (unless otherwise noted)

Parameter			Test Conditions		Min	Typ	Max	Unit
V_{T+}	Positive-going threshold voltage ($\overline{INIT}$)		V_{DD} = 4.5 V			2.7		V
			V_{DD} = 6 V			3.65		
V_{T-}	Negative-going threshold voltage ($\overline{INIT}$)		V_{DD} = 4.5 V			2.3		V
			V_{DD} = 6 V			3.15		
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) (INIT)		V_{DD} = 4.5 V			0.4		V
			V_{DD} = 6 V			0.5		
	LCD reference voltages	V_r	DAC register = 1000, T_A = 25°C, See Figures 2–5 and 2–6		4.7	4.9	5.1	V
		$-V_r'$			3.717	3.875	4.033	
		V_c'			2.734	2.85	2.966	
		V_r'			1.751	1.825	1.899	
		$-V_r$			0.767	0.8	0.833	
V_r	LCD temperature coefficient†		T_A = 0°C to 40°C			–2.5		mV/°C
	DAC step		DAC step control of V_r with respect to $-V_r$, V_{DD} = 5 V, T_A = 25°C		74	100	124	mV
I_{lkg}	Input leakage current (except for OSC1, $\overline{INIT}$ see Figure 3–5)						1	µA
$I_{standby}$	Standby current ($\overline{INIT}$ low)						10	µA
I_{DD}‡	Supply current		D/A option 1 or 3			5		mA
I_{OH}	High-level output current (PAx, PBx, D/A options 1)		V_{DD} = 4 V,	V_{OH} = 3.5 V	–4	–6		mA
			V_{DD} = 5 V,	V_{OH} = 4.5 V	–5	–7.5		
			V_{DD} = 6 V,	V_{OH} = 5.5 V	–6	–9.2		
			V_{DD} = 4 V,	V_{OH} = 2.67 V	–8	–13		mA
			V_{DD} = 5 V,	V_{OH} = 3.33 V	–14	–20		
			V_{DD} = 6 V,	V_{OH} = 4 V	–20	–29		
I_{OL}	Low-level output current (PAx, PBx, D/A options 1)		V_{DD} = 4 V,	V_{OL} = 0.5 V	10	17		mA
			V_{DD} = 5 V,	V_{OL} = 0.5 V	13	20		
			V_{DD} = 6 V,	V_{OL} = 0.5 V	15	25		
			V_{DD} = 4 V,	V_{OL} = 1.33 V	20	32		mA
			V_{DD} = 5 V,	V_{OL} = 1.67 V	30	52		
			V_{DD} = 6 V,	V_{OL} = 2 V	41	71		

† This negative temperature coefficient is normally advantageous because it tracks the temperature variation of most LCD materials.

‡ Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

Table 3–8. TSP50C12 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature(unless otherwise noted) (Continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
Pull up resistance	Resistors selected with software and connected between pin and V_{DD}	15	30	60	kΩ
DAC buffer drive (D/A option 1)	32-Ω load connected across DA1 and DA2, VDD = 4.5 V		60		mA
LCD frame rate	f_{OSC} = 9.6 MHz		96		Hz

3.6 TSP50C04/06/13/14/19 Electrical Characteristics

Table 3–9 gives specifications that apply to the TSP50C04, TSP50C06, TSP50C13, TSP50C14, and the TSP50C19.

Table 3–9. TSP50C04/06/13/14/19 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (unless otherwise noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
V_{T+}	Positive-going threshold voltage ($\overline{INIT}$)	V_{DD} = 4.5 V			2.7		V
		V_{DD} = 6 V			3.65		
V_{T-}	Negative-going threshold voltage ($\overline{INIT}$)	V_{DD} = 4.5 V			2.3		V
		V_{DD} = 6 V			3.15		
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) (INIT)	V_{DD} = 4.5 V			0.4		V
		V_{DD} = 6 V			0.5		
I_{lkg}	Input leakage current (except for OSC1, $\overline{INIT}$ see Figure 3–5)					1	µA
$I_{standby}$	Standby current ($\overline{INIT}$ low)					10	µA
I_{DD}†	Supply current	DAC option 1 or 2			5		mA
I_{OH}	High-level output current (D/A options 1, 2)	V_{DD} = 4 V,	V_{OH} = 3.5 V	–27	–41		mA
		V_{DD} = 5 V,	V_{OH} = 4.5 V	–34	–51		
		V_{DD} = 6 V,	V_{OH} = 5.5 V	–41	–63		
		V_{DD} = 4 V,	V_{OH} = 2.67 V	–54	–88		mA
		V_{DD} = 5 V,	V_{OH} = 3.33 V	–95	–136		
		V_{DD} = 6 V,	V_{OH} = 4 V	–136	–197		
	High-level output current (PAx, PBx)	V_{DD} = 4 V,	V_{OH} = 3.5 V	–4	–6		mA
		V_{DD} = 5 V,	V_{OH} = 4.5 V	–5	–7.5		
		V_{DD} = 6 V,	V_{OH} = 5.5 V	–6	–9.2		
		V_{DD} = 4 V,	V_{OH} = 2.67 V	–8	–13		mA
		V_{DD} = 5 V,	V_{OH} = 3.33 V	–14	–20		
		V_{DD} = 6 V,	V_{OH} = 4 V	–20	–29		

† Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

Table 3–9 TSP50C04/06/13/14/19 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (unless otherwise noted) (Continued)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{OL}	Low-level output current (D/A options 1, 2)	V_{DD} = 4 V,	V_{OL} = 0.5 V	27	41		mA
		V_{DD} = 5 V,	V_{OL} = 0.5 V	34	51		
		V_{DD} = 6 V,	V_{OL} = 0.5 V	41	63		
		V_{DD} = 4 V,	V_{OL} = 1.33 V	54	88		mA
		V_{DD} = 5 V,	V_{OL} = 1.67 V	95	136		
		V_{DD} = 6 V,	V_{OL} = 2 V	136	197		
	Low-level output current (PAx, PBx)	V_{DD} = 4 V,	V_{OL} = 0.5 V	10	17		mA
		V_{DD} = 5 V,	V_{OL} = 0.5 V	13	20		
		V_{DD} = 6 V,	V_{OL} = 0.5 V	15	25		
		V_{DD} = 4 V,	V_{OL} = 1.33 V	20	32		mA
		V_{DD} = 5 V,	V_{OL} = 1.67 V	30	52		
		V_{DD} = 6 V,	V_{OL} = 2 V	41	71		
	Pullup resistance	Resistors selected with software and connected between pin and V_{DD}		15	30	60	kΩ
f_{osc}	Oscillator frequency‡	7.68-MHz target frequency, V_{DD} = 5 V, T_A = 25°C		7.21	7.68	8.15	MHz
		9.6-MHz target frequency, V_{DD} = 5 V, T_A = 25°C		9.02	9.6	10.2	

‡ The frequency of the internal clock has a temperature coefficient of approximately −0.2 %/°C and a V_{DD} coefficient typical = 3%/V and a maximum =5.4%/V.