DESCRIPTION

The HYM536410A is a 4M x 36-bit Fast page mode CMOS DRAM module consisting of eight HY5117400A in 24/26 pin SOJ or TSOPII and four HY514100A in 20/26 pin SOJ or TSOPII on a 72 pin glass-epoxy printed circuit board. 0.22μF decoupling are mounted for each DRAM. The HYM536410AM / ASLM / ATM / ASLTM are Tin-Lead plated and HYM536410AMG / ASLMG / ATMG / ASLTMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- Low power dissipation
  Max. battery back-up 30.8mW (L-part)
  Max. CMOS standby 22.0mW (L-part)
  66.0mW
  Max. TTL standby 132.0mW
  Max. operating

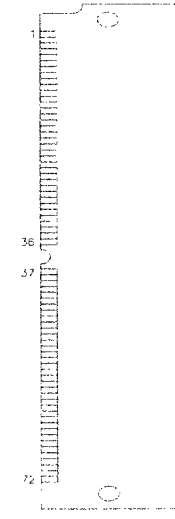
Speed	Power
50	9.13W
60	7.70W
70	6.49W

- Single power supply of 5V ± 10%
- TTL compatible inputs and outputs
- Fast access time

Speed	tRAC	tCAC	tPC
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- Fast Page Mode Operation
- /CAS-before-/RAS, /RAS-only, Hidden refresh, Self-refresh
- 2048 refresh cycles / 256ms (L-part)
  2048 refresh cycles / 32ms

PIN CONNECTION



PIN CONNECTION

/RAS0, /RAS2	Row Address Strobe
/CAS0-/CAS3	Column Address Strobe
/WE	Write Enable
A0-A10	Address Input
DQ0-DQ35	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

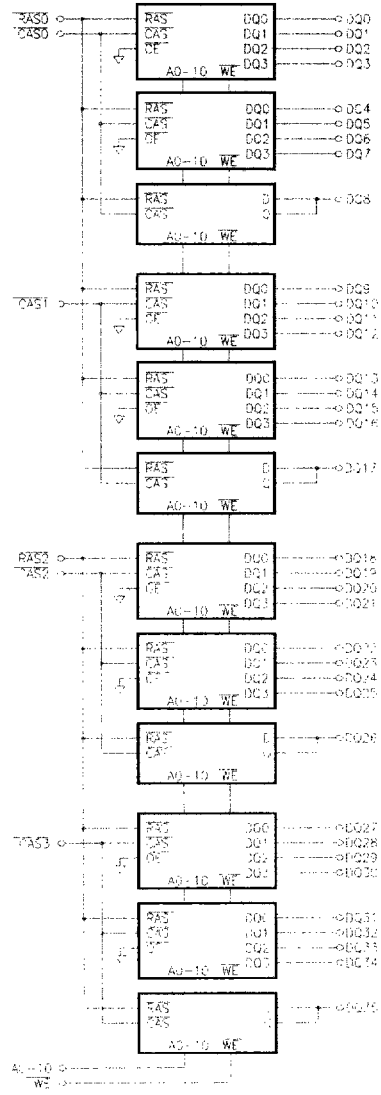
PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	/CAS0
5	DQ19	41	/CAS2
6	DQ2	42	/CAS3
7	DQ20	43	/CAS1
8	DQ3	44	/RAS0
9	DQ21	45	NC
10	Vcc	46	NC
11	PD5	47	/WE
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	Vcc	66	PD EDO
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	/RAS2	70	PD4
35	DQ26	71	PD REF.
36	DQ8	72	Vss

PRESENCE DETECT PINS

PIN	-50	-60	-70
PD1	Vss	Vss	Vss
PD2	NC	NC	NC
PD3	Vss	NC	Vss
PD4	Vss	NC	NC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	-1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	12.76	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(TA=0°C to 70°C, V_{CC}= 5V ± 10%, Vss=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	Vss ≤ V_{IN} ≤ V_{CC}+1.0, All other her pins not under test=Vss		-120	120	μA	
I_{LO}	Output Leakage Current (High impedance State)	Vss ≤ V_{OUT} ≤ V_{CC} /RAS & /CAS at V_{IH}		-10	10	μA	
I_{CC1}	Vcc Supply Current Operating	t_{RC}=t_{RC} (min.)	50	-	1660	mA	1,2,3
			60	-	1400		
			70	-	1180		
I_{CC2}	Vcc Supply Current TTL Standby	/RAS & /CAS at V_{IH}, other inputs ≥ Vss		-	24	mA	
I_{CC3}	Vcc Supply Current /RAS-only refresh	t_{RC}=t_{RC}(min.)	50	-	1660	mA	1,3
			60	-	1400		
			70	-	1180		
I_{CC4}	Vcc Supply Current, EDO mode	t_{HPC}= t_{HPC} (min.)	50	-	1020	mA	1,2,3
			60	-	900		
			70	-	780		
I_{CC5}	Vcc Supply Current CMOS Standby	/RAS & /CAS ≥ V_{CC} – 0.2V		-	12	mA	
			L-part	-	4.0		5
I_{CC6}	Vcc Supply Current /CAS before /RAS refresh	t_{RC}=t_{RC}(min.)	50	-	1660	mA	1,3
			60	-	1400		
			70	-	1180		
I_{CC7}	Vcc Supply Current, Battery Back Up (L-part only)	t_{RC}= 125μs, /CAS = CBR cycling or 0.2V, /WE = V_{CC} – 0.2V A0 - A10 = V_{CC} – 0.2V or 0.2V DQ0-DQ31=V_{CC}-0.2V, 0.2V or open	t_{RAS} ≤ 300ns	-	3.6	mA	1,4,5
			t_{RAS} ≤ 1μs	-	5.6		
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= -5mA		2.4	-	V	

NOTE

1. I_{CC1}, I_{CC3}, I_{CC4},I_{CC6} and I_{CC7} depend on cycle rate.
2. output loading. Specified values are obtained with the ouptup open.
3. I_{CC} is specified as average current. For I_{CC1},I_{CC3} and I_{CC6} address can be changed maximum two times while /RAS=V_{IL}. For I_{CC4}, address can be changed maximum once while /CAS=V_{IH}.
4. Only t_{RAS}(max.)=1μs is applied to refresh of battery backup but t_{RAS}(max.)=10μs is applied to normal functional operation.
5. I_{CC5}(max.)=4.0mA and I_{CC7} are applied to L-part only (HYM536410ALM/ALTM/ALMG/ALTMG).

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc= 5V ± 10%, Vss= 0V, unless otherwise noted.) NOTE : 1,2,3

#	SYMBOL	PARAMTER	HYM536410A M-Series						UNIT	NOTE
			-50		-60		-90			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tRHCP	/RAS Hold Time from /CAS Precharge	30	-	35	-	40	-	ns	
5	tRAC	Access Time from /RAS	-	50	-	60	-	70	ns	5,10,11
6	tCAC	Access Time from /CAS	-	13	-	15	-	18	ns	5,10
7	tAA	Access Time from Coulmn Address	-	25	-	30	-	35	ns	5,10,11
8	tCPA	Access Time from /CAS Precharge	-	30	-	35	-	40	ns	5
9	tCLZ	/CAS to Output Low Impedance	0	-	0	-	0	-	ns	5
10	tOFF	Output Buffer Turn-off Delay	0	10	0	13	0	15	ns	6
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	4
12	tRP	/RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	/RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	/RAS Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	/RAS Hold Time	13	-	15	-	18	-	ns	
16	tCSH	/CAS Hold Time	50	-	60	-	70	-	ns	
17	tCAS	/RAS Pulse Width	13	10K	15	10K	18	10K	ns	
18	tRCD	/RAS to /CAS Delay	18	37	20	45	20	52	ns	10
19	tRAD	/RAS to Column Address Delay Time	15	30	15	35	15	40	ns	11
20	tCRP	/CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	/CAS Precharge Time	8	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	8	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	10	-	ns	
26	tAR	Column Address Hold Time from /RAS	50	-	50	-	55	-	ns	
27	tRAL	Column Address to /RAS Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	7
30	tRRH	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	7
31	tWCH	Write Command Hold Time	8	-	10	-	10	-	ns	
32	tWCR	Write Command Hold Time from /RAS	45	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	8	-	10	-	10	-	ns	
34	tRWL	Write Command to /RAS Lead Time	13	-	15	-	18	-	ns	
35	tCWL	Write Command to /CAS Lead Time	13	-	15	-	18	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	8
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	8
38	tDHR	Data-In Hold Time Referenced to /RAS	50	-	50	-	55	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		L-part	-	256	-	256	-	256	ms	12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	9

AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMTER	HYM536410A M-Series						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	t_{CSR}	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	t_{CHR}	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
43	t_{CPT}	/RAS Precharge Time (CBR Counter Test)	25	-	30	-	35	-	ns	
44	t_{WRP}	/WE to /RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	t_{WRH}	/WE to /RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS intilization cycles instead of 8 /RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If /RAS=V_{SS} during power-up, the HYM536410A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that /RAS and /CAS track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition time is measured beteen V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
4. Refer to the HY5117400A and HY514100A data sheet for detailed information.
5. Measured at with a load equivalent to 2 TTL loads and 100pF. (V_{OH}=2.4V, V_{OL}=0.4V)
6. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in late write or read-modify-write cycles.
9. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throught the entire cycle
10. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
11. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
12. t_{REF} (max.)= 256ms is applied to L-part only (HYM536410ALM/ALTM/ALMG/ALTMG).

CAPACITANCE

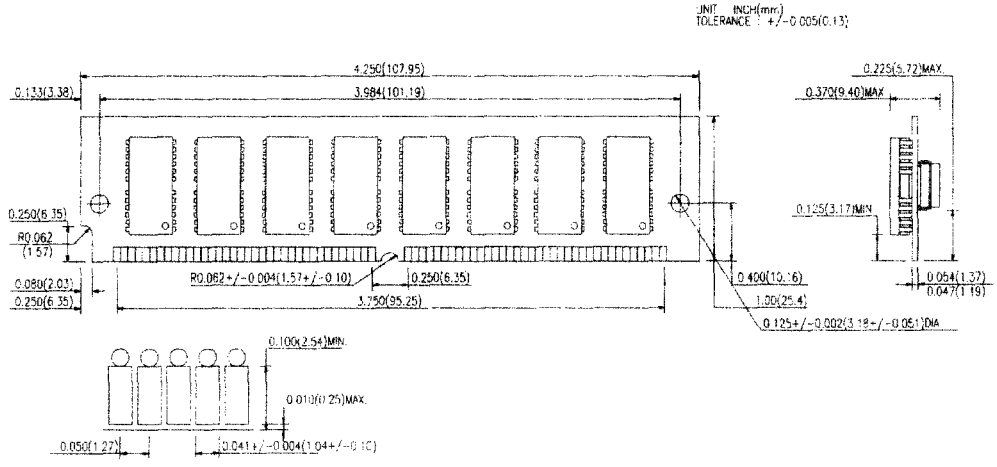
(TA=25°C, V_{CC}= 5V± 10%, Vss=0V, f=1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	88	pF
C_{IN2}	Input Capacitance (/WE)	-	94	pF
C_{IN3}	Input Capacitance (/RAS0)	-	94	pF
C_{IN4}	Input Capacitance (/CAS0, /CAS3)	-	36	pF
C_{DQ1}	Data Input/Output Capacitance (DQ0-7,9-16,18-25,27-34)	-	17	pF
C_{DQ2}	Data Input/output Capacitance (DQ8,17,26,35)	-	22	pF

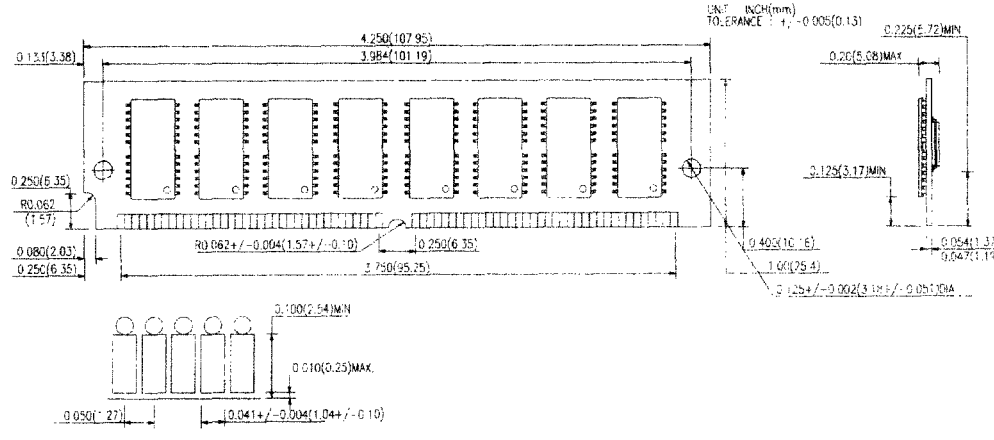
PACKAGE DIMENSION

72pin Single In-line Memory Module (M;Tin-Lead, MG;Gold plated)

HYM536410A/AL (SOJ Mounted)



HYM536410AT/ALT (TSOPII Mounted)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM536410AM	50/60/70		SIMM	Tin-Lead
HYM536410ALM	50/60/70	L-part	SIMM	Tin-Lead
HYM536410ATM	50/60/70		SIMM	Tin-Lead
HYM536410ALTM	50/60/70	L-part	SIMM	Tin-Lead
HYM536410AMG	50/60/70		SIMM	Gold
HYM536410ALMG	50/60/70	L-part	SIMM	Gold
HYM536410ATMG	50/60/70		SIMM	Gold
HYM536410ALTMG	50/60/70	L-part	SIMM	Gold