T-46-13-27

HYBRID

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128 k x 8 EEPROM

ME8128SC
Issue 1.3 : September 1988

Supersedes:-HMEE48128J

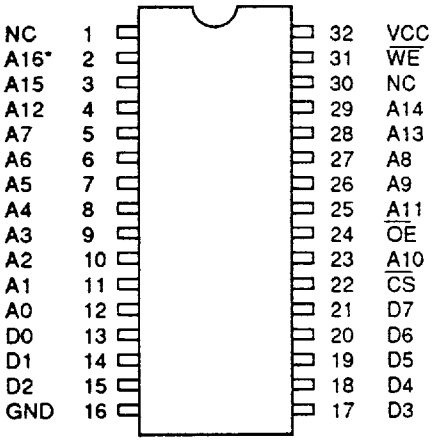
ADVANCED PRODUCT INFORMATION

131,072 x 8 CMOS High Speed EEPROM .

Features

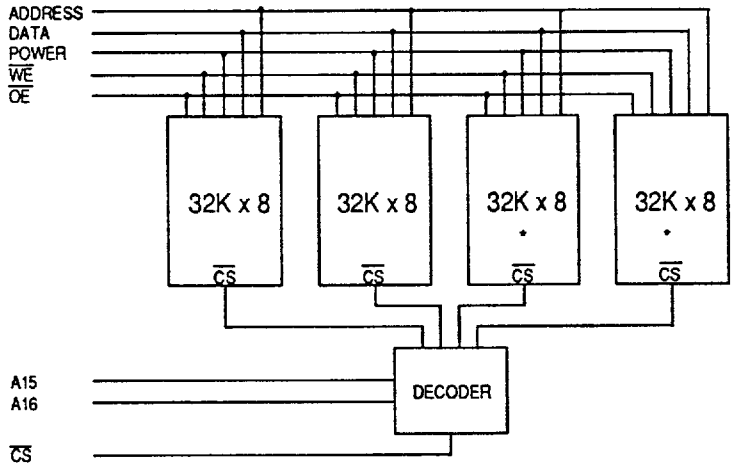
- Fast Access Times of 260/300/350 nS
- Half populated version ME864SC available
- Standard 32 pin DIL footprint
- JEDEC pin definition
- Directly TTL Compatable
- Low Power Consumption 310mW (typ. active)
- Completely Static Operation
- Data Protection on Power On/Power Off
- Common data inputs & outputs
- Byte and Page Write up to 64bytes in 12mS
- 10,000 Erase/Write cycles minimum
- 10 year data retention
- May be Screened in accordance with BS9400 and MIL-STD-883C (suffix HR)

Pin Definition



*Pin 2 should be connected to V_{cc} on ME864SC
Pins 1 & 30 are connected together internally

Block Diagram

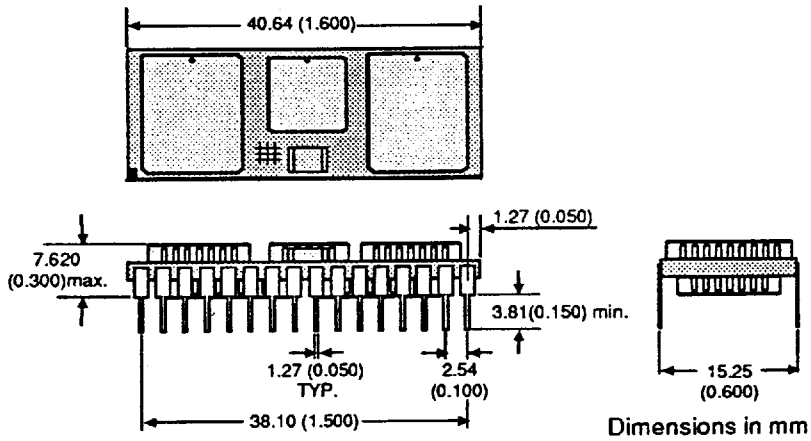


*Not fitted to ME864SC

Pin Functions

A0-A16	Address Inputs
D0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
NC	No Connect
VCC	Power (+5V)
GND	Ground

Package Details



Dimensions in mm (inches).
Tolerance on all dimensions +/-0.254(0.010).
No LCC's fitted to underside of ME864SC.

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Absolute Maximum Ratings

Supply Voltage*	V_{CC}	-0.3 to +6	V
Input Voltage*	V_{in}	-0.3 to +6	V
Operating Temperature	T_{opr}	-55 to +125	°C
Storage Temperature	T_{stg}	-65 to +150	°C

* With Respect to V_{ss}

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.1*	-	0.8	V
Operating Temperature	T_{opr}	0	-	70	°C
		-40	-	85	°C (8128SCI)
		-55	-	125	°C (8128SCM,MB)

*Pulse Width:50nS,DC:V_{IL}min=-0.3V

DC Electrical Characteristics(T_a=0 to +70°C,V_{CC}=5V±10%)

			8128SC		864SC		
Parameter	*Symbol*	*Test Condition*	*min*	*max*	*min*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{CC}= 5.5V & V_{in}=5.5V	-	40	-	20	µA
Output Leakage Current	I_{LO}	V_{CC}=5.5V & V_{out}=5.5/0.4V	-	40	-	20	µA
V_{CC} Current	I_{CC1}	$\overline{CE}$=V_{IH},$\overline{OE}$=V_{IL},I_{out}=0mA	-	12	-	6	mA
(Standby)	"	$\overline{CE}$>=V_{CC}-0.3	-	1.4	-	0.7	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IL},I_{out}=0mA,f=1MHz	-	105	-	62.5	mA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	-	0.45	-	0.225	V
Output High Voltage	V_{OH}	I_{OH}=- 400uA	2.4	-	1.2	-	V

Capacitance (T_a=25°C,f=1MHz)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance on any input	C_{in}	V_{in}=0V	18	26	pF
Output Capacitance:	C_{out}	V_{out}=0V	36	48	pF

AC Test Conditions(T_a=0 to +70°C,V_{CC}=5V±10%)

* Input pulse levels: 0.45V to 2.4V
* Input rise and fall times: ≤20ns
* Input timing reference level: 1V and 2V
* Output timing reference level: 0.8V and 2V
* Output load: 1 TTL gate + 100pF

Electrical Characteristics & Recommended AC Operating Conditions

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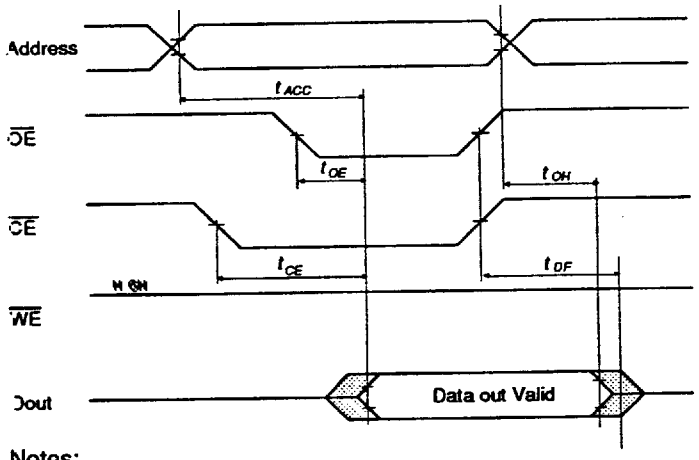
Read Cycle

Parameter	Symbol	-26 min	-26 max	-30 min	-30 max	-35 min	-35 max	Unit
Address to Output Delay	t_{ACC}	-	260	-	300	-	350	ns
$\overline{CE}$ to Output Delay	t_{CE}	-	260	-	300	-	350	ns
$\overline{OE}$ to Output Delay	t_{OE}	0	100	0	120	0	120	ns
Address to Output Hold	t_{OH}	0	-	0	-	0	-	ns
$\overline{OE}$ High to Output Float	t_{DF}	0	60	0	80	0	80	ns

Read Cycle Timing Waveform (1,2)

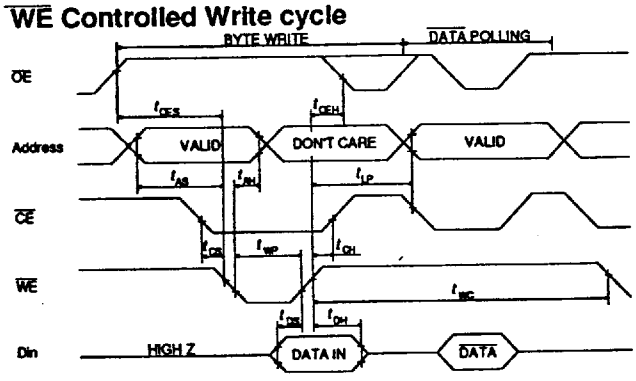


Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition Low.

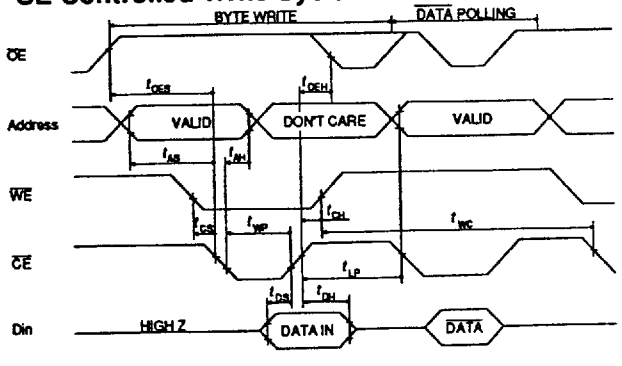
Byte Erase and Byte Write Operation

Parameter	Symbol	min	max	units	notes
Address Setup Time	t_{AS}	20	-	nS	5
$\overline{CE}$ to Write Setup Time	t_{CS}	0	-	nS	
Write Pulse Width	t_{WP}	150	-	nS	1, 4
Address Hold Time	t_{AH}	150	-	nS	5
Data Setup Time	t_{DS}	50	-	nS	
Data Hold Time	t_{DH}	20	-	nS	
$\overline{CE}$ Hold Time	t_{CH}	20	-	nS	
$\overline{OE}$ to Write Setup Time	t_{OES}	20	-	nS	
$\overline{OE}$ Hold Time	t_{OEH}	40	-	nS	
Last Byte Loaded to $\overline{Data}$ Polling	t_{LP}	650	-	uS	3
Write Cycle Time	t_{WC}	-	12	mS	
Byte Load Timer Cycle	t_{BLC}	0.2	100	uS	2

$\overline{WE}$ Controlled Write cycle



$\overline{CE}$ Controlled Write Cycle



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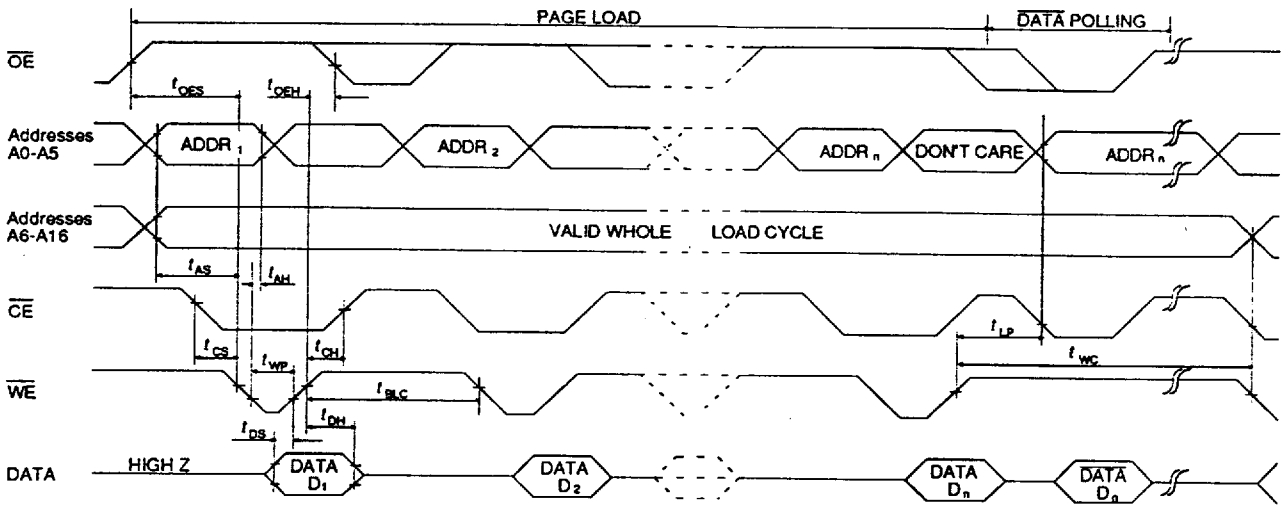
Notes:

1. A write occurs during the overlap (t_{wp}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{wc} (min) is the minimum time before the next byte can be loaded, t_{wc} (max) is the minimum time the internal byte load timer waits before initiating an internal write cycle.
3. $\overline{Data}$ polling allows comparison operation to determine the status of the EEPROM.During a write cycle,an attempted read of the last byte written in the EEPROM results in the complement data of that byte at bit D7. Data polling must not commence until t_{wc} (min) has elapsed.
4. There are four features that protect the data from an inadvertant write.
   i)Noise Protection : A write cycle will not be initiated with a $\overline{WE}$ pulse of less than 20ns.
   ii)Vcc Sense : When the Vcc is approximately 3.0V,Write and Erase functions are not initiated.
   iii)Write Inhibit : Holding $\overline{OE}$ low,$\overline{WE}$ high,or $\overline{CE}$ high,inhibits a write cycle during power-on and power-off.
   iv)Write Inhibit : Holding $\overline{OE}$ low,$\overline{WE}$ low and $\overline{CE}$ low,inhibits a write cycle during power-on and power-off.
5. During a write cycle,addresses are latched on the falling edge of $\overline{WE}$: data is latched on the rising edge of $\overline{WE}$.

Page Timing



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