Signetics

FAST 74F1764/1765, 74F1764-1/1765-1

1 Megabit DRAM Dual-Ported Controllers

Preliminary Specification

FAST Products

FEATURES

- Allows two microprocessors to access the same bank of dynamic RAM
- Performs arbitration, signal timing, address multiplexing, and refresh
- 10 address output pins allow direct control of up to 1Mbit dynamic RAMS
- External address multiplexing enables control of 4Mbit (or greater) dynamic RAMs
- Separate refresh clock allows adjustable refresh timing
- F1764/F1764-1 have on-chip 20-bit address input latch
- Allows control of dynamic RAMs with row access times down to 40ns
- F1764/1765 output drivers designed for incident wave switching
- F1764-1/1765-1 output drivers designed for first reflected wave switching

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1764/1765	150MHz	150mA
74F1764-1/1765-1	150MHz	125mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%, T_A = 0°C to +70°C
Plastic DIP	74F1764N, 74F1765N, 74F1764-1N, 74F1765-1N
PLCC-44	74F1764A, 74F1765A, 74F1764-1A, 74F1765-1A

DESCRIPTION

The 74F1764/1765 DRAM Dual-ported Controller is a high-speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F1764 vs 74F1765

The F1764 though functionally and pin to pin compatible with the F1765 differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

74F1764/1765 vs 74F1764-1/1765-1

The 74F1764-1/1765-1, though as fast as the 74F1764/1765, differs from the 74F1764/1765 in the following respects:

a) they reduce the row address hold time by half-a-clock cycle, and

b) their outputs are optimized for first reflected wave switching as opposed to incident wave switching.

The specialized outputs eliminate the need for signal terminations in essentially all applications.

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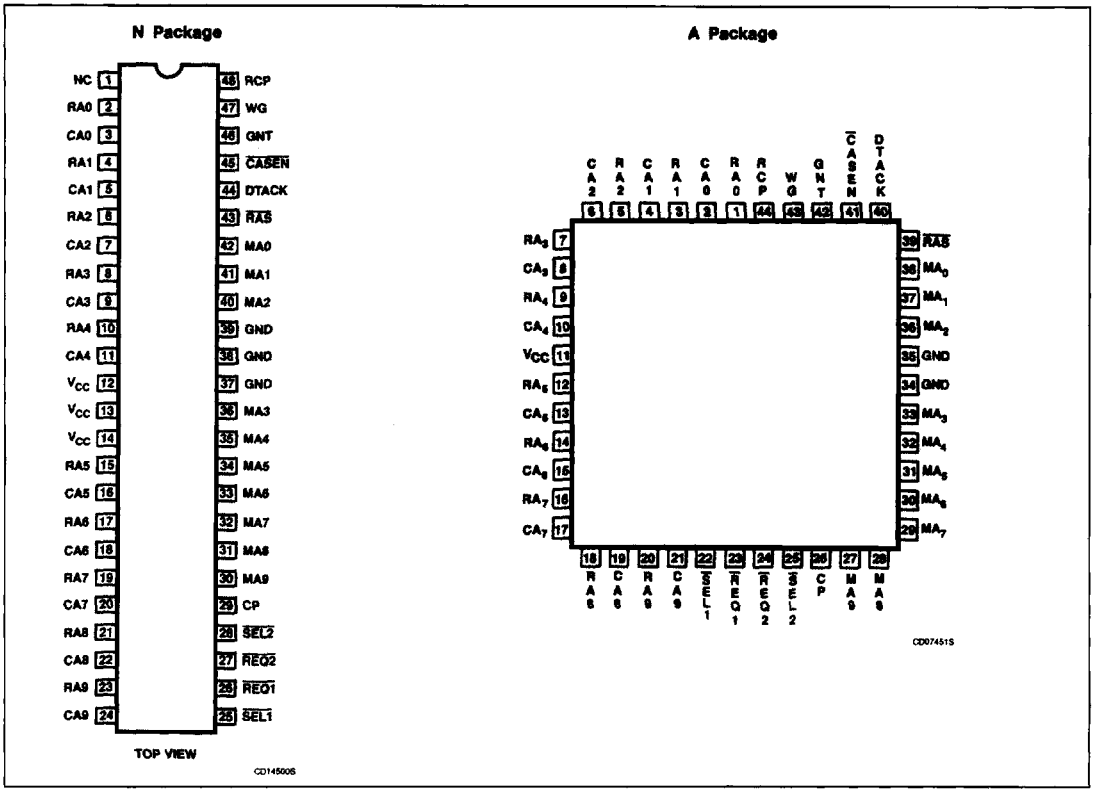
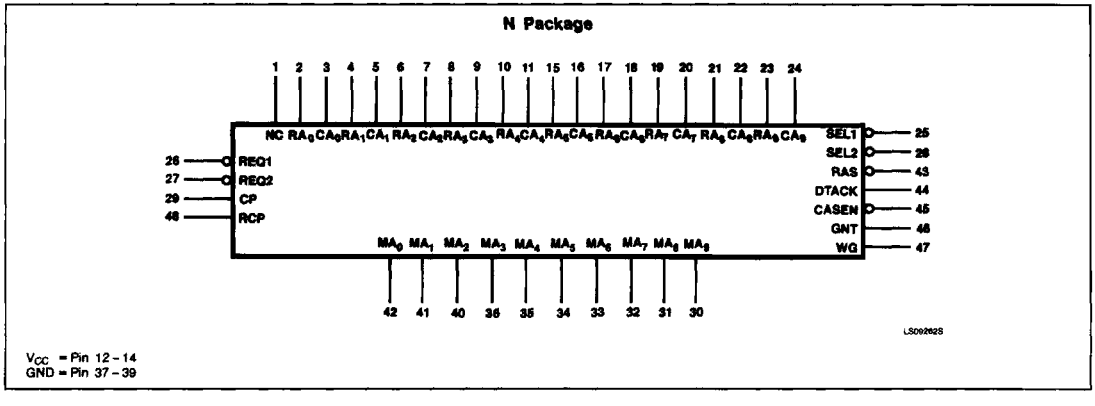
1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764/1765, 74F1764-1/1765-1

PIN CONFIGURATION



LOGIC SYMBOL



VCC = Pin 12 – 14
GND = Pin 37 – 39

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
RA_0	2	1	I	Address inputs used to generate memory row address
RA_1	4	3	I	
RA_2	6	5	I	
RA_3	8	7	I	
RA_4	10	9	I	
RA_5	15	12	I	
RA_6	17	14	I	
RA_7	19	16	I	
RA_8	21	18	I	
RA_9	23	20	I	
CA_0	3	2	I	Address inputs used to generate memory column address
CA_1	5	4	I	
CA_2	7	6	I	
CA_3	9	8	I	
CA_4	11	10	I	
CA_5	16	13	I	
CA_6	18	15	I	
CA_7	20	17	I	
CA_8	22	19	I	
CA_9	24	21	I	
$\overline{REQ}_1$	26	23	I	Memory access request from Microprocessor 1
$\overline{REQ}_2$	27	24	I	Memory access request from Microprocessor 2
CP	29	26	I	Clock input which determines the master timing
RCP	48	44	I	Refresh clock determines the period of refresh for each row after it is internally divided by 64
$\overline{SEL}_1$	25	22	O	Select signal is activated in response to active $\overline{REQ}_1$ input, indicating selection of Microprocessor 1
V_{CC}	12 – 14	11		Power supply +5V± 10%
GND	37 – 39	34 35		Ground
$\overline{SEL}_2$	28	25	O	Select signal is activated in response to active $\overline{REQ}_2$ input, indicating selection of Microprocessor 2
MA_0	42	38	O	Memory address output pins, designed to drive address lines of the DRAM
MA_1	41	37	O	
MA_2	40	36	O	
MA_3	36	33	O	
MA_4	35	32	O	
MA_5	34	31	O	
MA_6	33	30	O	
MA_7	32	29	O	
MA_8	31	28	O	
MA_9	30	27	O	
GNT	46	42	O	Grant output, activated upon start of a memory access cycle
$\overline{RAS}$	43	39	O	Row address strobe, used to latch the row address into the bank of DRAM (to be connected directly to the $\overline{RAS}$ inputs of the DRAMs)
WG	47	43	O	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
$\overline{CASEN}$	45	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs
DTACK	44	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has been met

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1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764/1765, 74F1764-1/1765-1

ARCHITECTURE

The 74F1764/1765 1 Megabit DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 'F1764/1765 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress. The arbitration is accomplished by sampling the $\overline{REQ}_1$ and $\overline{REQ}_2$ inputs on different edges of the CP clock. $\overline{REQ}_1$ is sampled on the rising edge and $\overline{REQ}_2$ on the falling edge (refer to Figures 1 – 4).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since $\overline{SEL}$ outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the $\overline{SEL}$ outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock should be set equal to:
(Tras (of the DRAM) + 16 – 5)/4 plus any system guard-band required.

For the F1764-1/1765-1 the CP clock input period should be equal to:
(Tras (of the DRAM) + 22 – 10)/4 plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a refresh cycle is in process, and there is only one active $\overline{REQ}$ input, the $\overline{SEL}$ output corresponding to the active input $\overline{REQ}$ will be asserted but the GNT output will not go High until after the completion of the refresh cycle (see Figures 10, 11 & 14, 15).

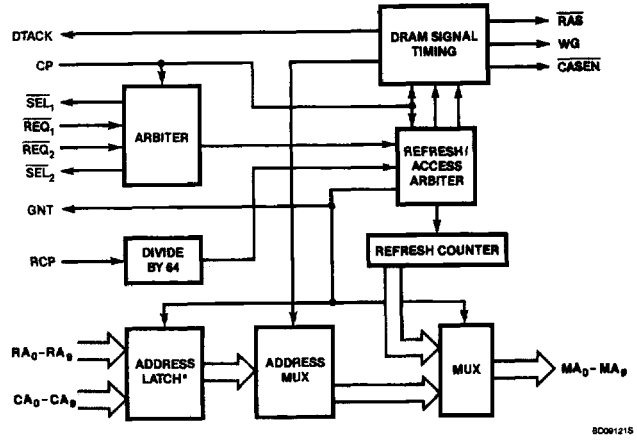
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the $\overline{SEL}$ output for the other processor will not be issued, though GNT is asserted at that time, because the other processor is performing an access cycle. This will ensure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the $\overline{SEL}$ output corresponding to the awaiting $\overline{REQ}$ input will be asserted, followed by the GNT output. If however, there were any pending refresh requests, assertion of the GNT output will be held OFF until the refresh request has been serviced.

When GNT goes High, the $RA_0 - RA_9$ and $CA_0 - CA_9$ address input to the 'F1764/F1764-1 are latched internally and the $RA_0 - RA_9$ signals are propagated to the $MA_0 - MA_9$ outputs. The address inputs are not latched by the F1765/F1765-1 and therefore, $RA_0 - RA_9$ inputs propagate directly to the $MA_0 - MA_9$ outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is asserted.

BLOCK DIAGRAM



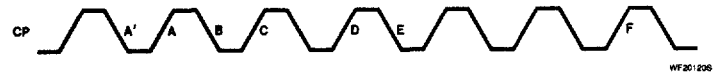
NOTE:
* The address input latch is available only on the 74F1764/F1764-1.

One clock cycle later, the $CA_0 - CA_9$ latch outputs on the 'F1764 or $CA_0 - CA_9$ inputs to the 'F1765 are selected and propagated to the $MA_0 - MA_9$ outputs. This occurs half a clock cycle earlier on the F1764-1/1765-1 (refer to Figures 3 & 4). The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

A half-clock cycle is again allowed for the $CA_0 - CA_9$ signals to propagate and stabilize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as $\overline{CAS}$ output or decoded with Higher-order address signals to produce multiple $\overline{CAS}$ signals. After $\overline{CASEN}$ is valid, the controller will wait for 2½ clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of approximately 4 clock cycles. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

All controller output signals are held in this final state until the selected processor withdraws its request by driving its $\overline{REQ}$ input High. When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

A refresh cycle is serviced by propagating the 10 refresh counter address signals to the $MA_0 - MA_9$ outputs. After a half-clock cycle the $\overline{RAS}$ output is asserted for four cycles and then negated for three clock cycles to meet the $\overline{RAS}$ precharge requirements of the DRAMs (see Figures 5 & 6).



A' $\overline{REQ}_2$ sampled

A $\overline{REQ}_1$ sampled
$\overline{SEL}_1$ triggered ($\overline{SEL}_1$ triggered by $\overline{REQ}_1$ sample circuitry) ($\overline{REQ}_2$ disabled by $\overline{SEL}_1$ circuitry)

B GNT triggered
$RA_0 - RA_9$ and $CA_0 - CA_9$ latched (Input address latch triggered by GNT circuitry)*
$RA_0 - RA_9$ propagate to $MA_0 - MA_9$ outputs

C $\overline{RAS}$ triggered

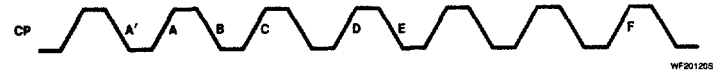
D WG triggered
$CA_0 - CA_9$ selected and propagated to $MA_0 - MA_9$ outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

* Only on the 'F1764.

Figure 1. Sequence of Events for $\overline{REQ}_1$ Memory Access Cycle for F1764/1765



A' $\overline{REQ}_2$ sampled
$\overline{SEL}_2$ triggered ($\overline{SEL}_2$ triggered by $\overline{REQ}_2$ sampling circuitry)

A $\overline{REQ}_1$ is not sampled (disabled by $\overline{SEL}_2$ circuitry)

B GNT triggered
$RA_0 - RA_9$ and $CA_0 - CA_9$ latched (Input address latch triggered by GNT circuitry)*
$RA_0 - RA_9$ propagate to $MA_0 - MA_9$ outputs

C $\overline{RAS}$ triggered

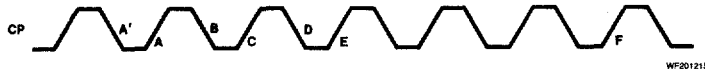
D WG triggered
$CA_0 - CA_9$ selected and propagated to $MA_0 - MA_9$ outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

* Only on the 'F1764.

Figure 2. Sequence of Events for $\overline{REQ}_2$ Memory Access Cycle for F1764/1765



A' $\overline{REQ}_2$ sampled

A $\overline{REQ}_1$ sampled
$\overline{SEL}_1$ triggered ($\overline{SEL}_1$ triggered by $\overline{REQ}_1$ sample circuitry) ($\overline{REQ}_2$ disabled by $\overline{SEL}_1$ circuitry)

B GNT triggered
$RA_0 - RA_9$ and $CA_0 - CA_9$ latched (Input address latch triggered by GNT circuitry)*
$RA_0 - RA_9$ propagate to $MA_0 - MA_9$ outputs

C $\overline{RAS}$ triggered

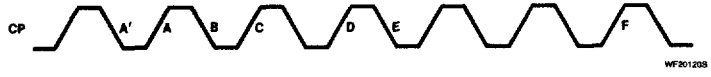
D WG triggered
$CA_0 - CA_9$ selected and propagated to $MA_0 - MA_9$ outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

* Only on the F1764-1.

Figure 3. Sequence of Events for $\overline{REQ}_1$ Memory Access Cycle for F1764-1/1765-1



A' $\overline{REQ}_2$ sampled
$\overline{SEL}_2$ triggered ($\overline{SEL}_2$ triggered by $\overline{REQ}_2$ sampling circuitry)

A $\overline{REQ}_1$ is not sampled (disabled by $\overline{SEL}_2$ circuitry)

B GNT triggered
$RA_0 - RA_9$ and $CA_0 - CA_9$ latched (Input address latch triggered by GNT circuitry)*
$RA_0 - RA_9$ propagate to $MA_0 - MA_9$ outputs

C $\overline{RAS}$ triggered

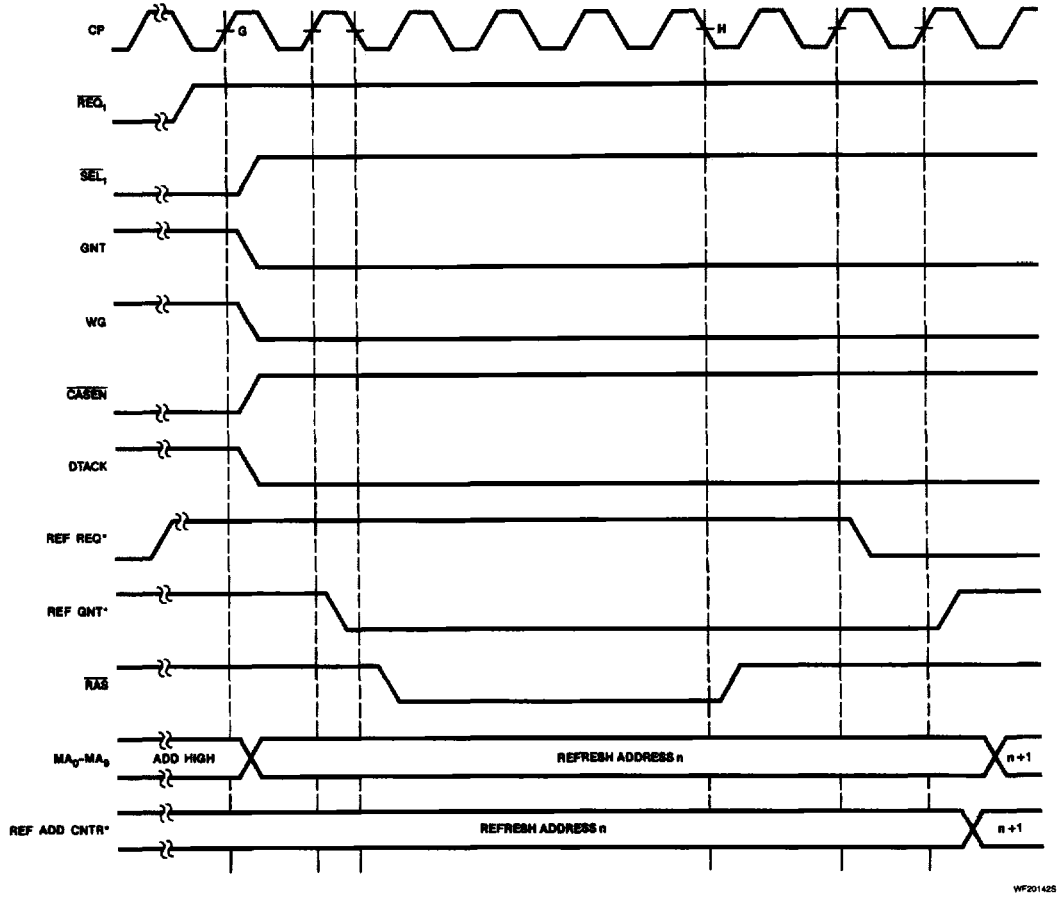
D WG triggered
$CA_0 - CA_9$ selected and propagated to $MA_0 - MA_9$ outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

* Only on the F1764-1.

Figure 4. Sequence of Events for $\overline{REQ}_2$ Memory Access Cycle for F1764-1/1765-1



NOTE:
* These are internal signals only.

Figure 5. Refresh Cycle Timing Following a $\overline{REQ}_1$ Memory Access Cycle

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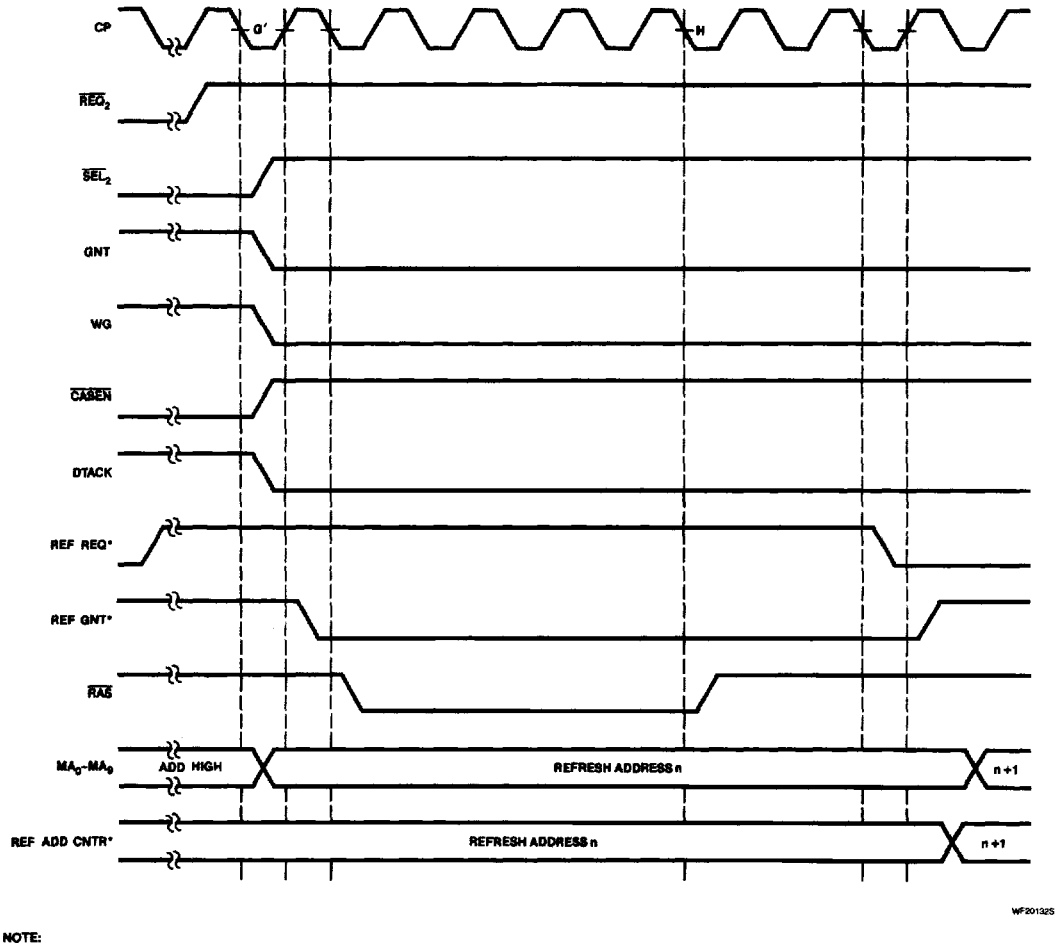


NOTE:
* These are internal signals only.

Figure 6. Refresh Cycle Timing Following a $\overline{REQ}_2$ Memory Access Cycle

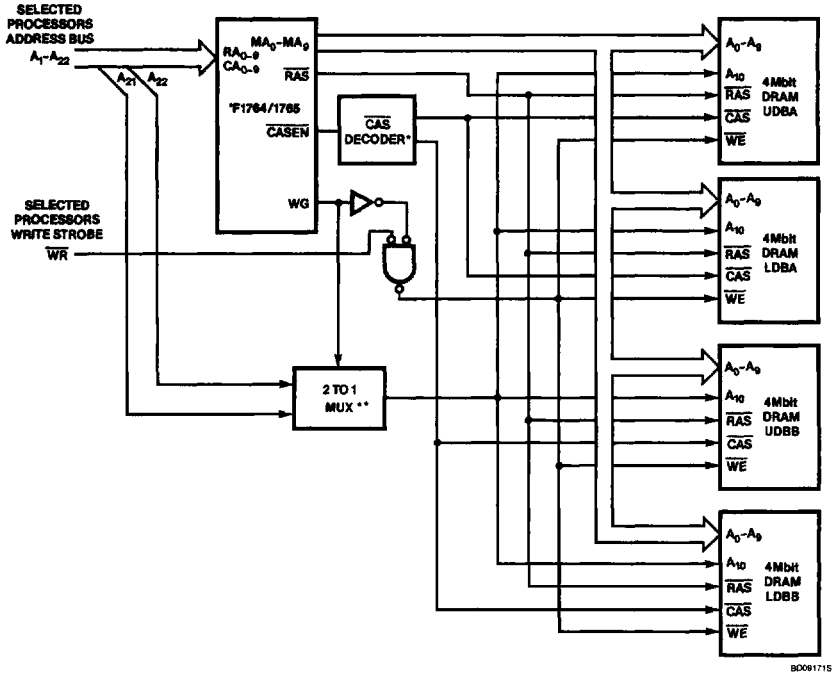
USING 74F1764/1765 AND 74F1764-1/1765-1 TO ADDRESS 4MBIT DRAMS

The addressing capabilities of the 1 Megabit DRAM dual-ported controllers can be extended to address 4Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 7 shows an application, using an external 2-to-1 multiplexer to address 4Mbit dynamic RAMs. The 10-bit internal refresh counter of the controller provides 1024 row addresses which more than meet the refreshing needs for most industry standard 4Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 1024 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 1024 row addresses.

The WG output of the controller should be used to multiplex between the external row and column addresses. However it is important that the propagation delay through the external multiplexer does not cause column address setup violations on the dynamic RAM.



NOTES:
* The $\overline{CAS}$ decode logic is not necessary if multiple $\overline{CAS}$ signals are not required. The application also does not show further decoding of multiple $\overline{CAS}$ signals to distinguish between Upper and Lower data bytes. If required, multiple $\overline{CAS}$ signal generation and Upper and Lower byte decoding can be accomplished as shown in Figures 16 – 18.
** Propagation delay through the multiplexer should be considered when using the controller for 4Mbit addressing.

Figure 7. Using the Controller to Address 1Mbit DRAMs

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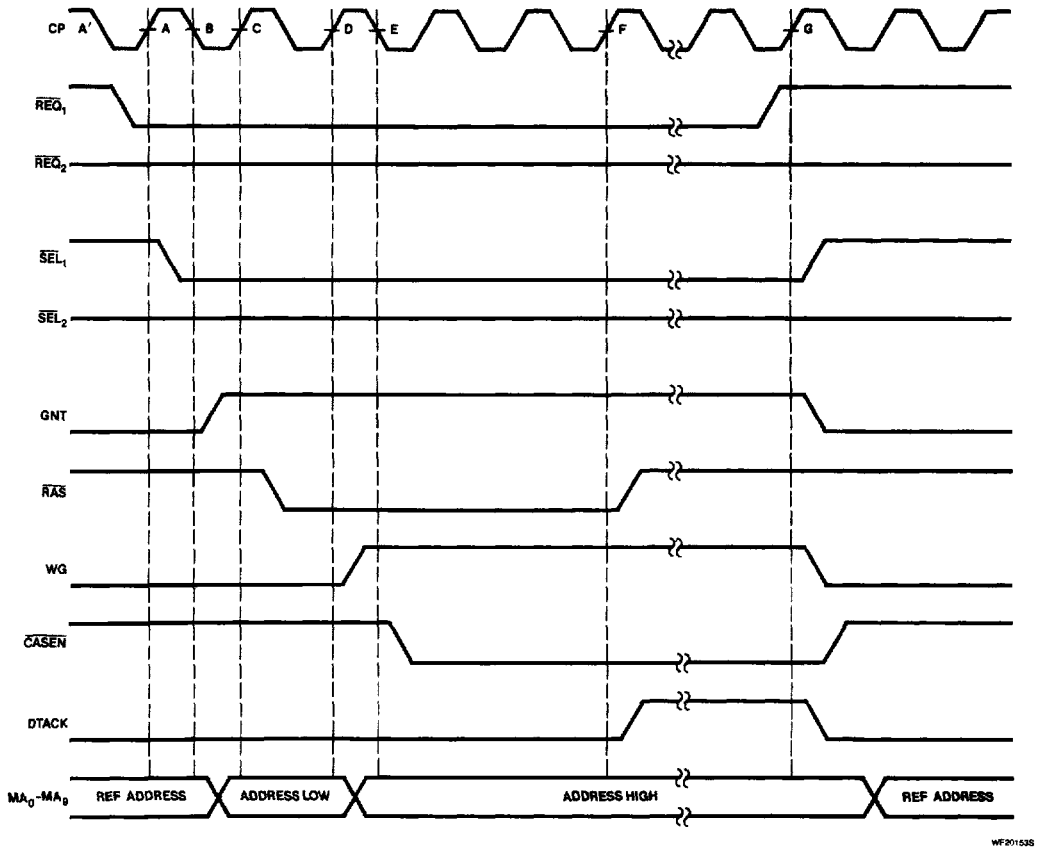

Figure 8. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing for F1764/1765

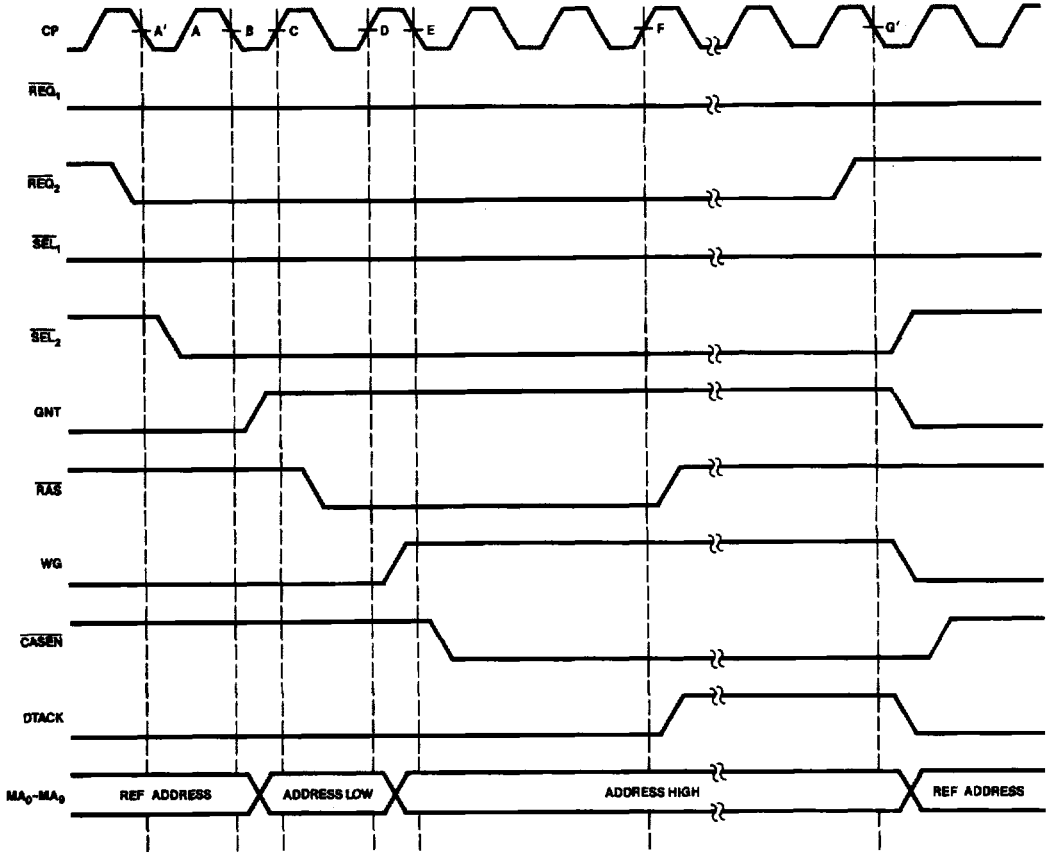

Figure 9. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing for F1764/1765

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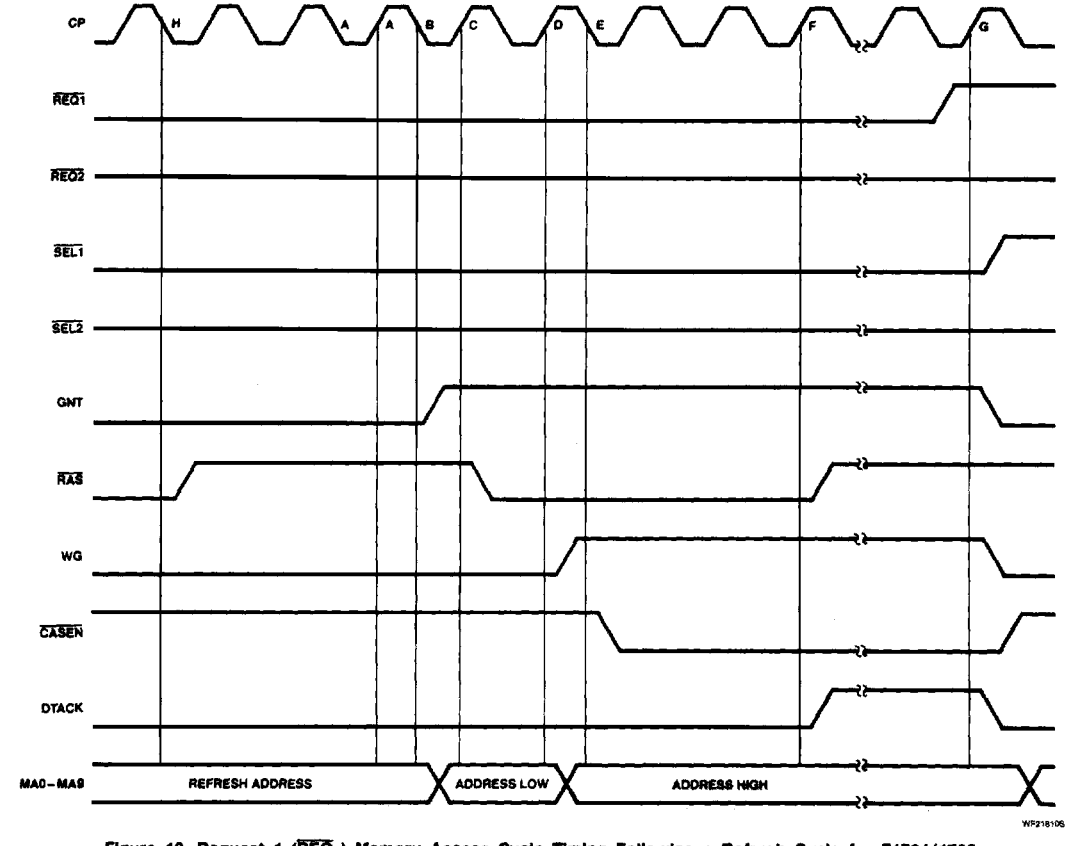


Figure 10. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing Following a Refresh Cycle for F1764/1765

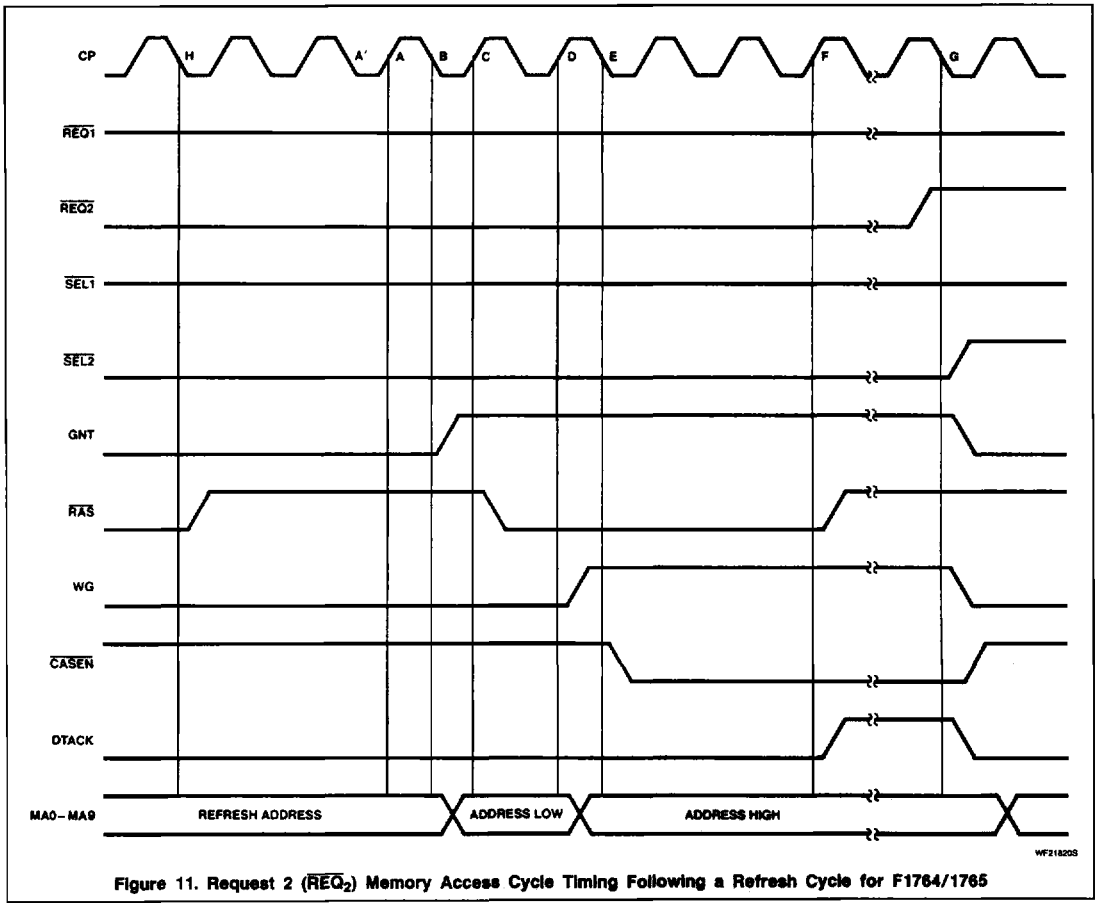


Figure 11. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing Following a Refresh Cycle for F1764/1765

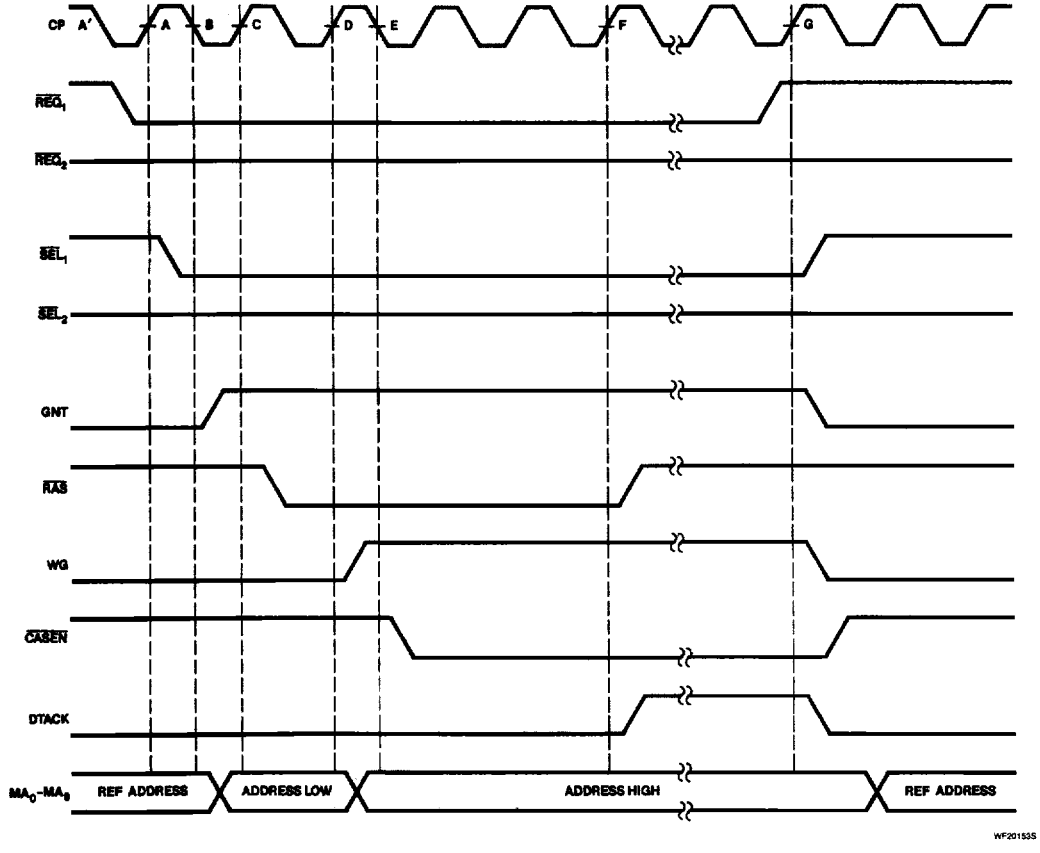


Figure 12. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing for F1764-1/1765-1

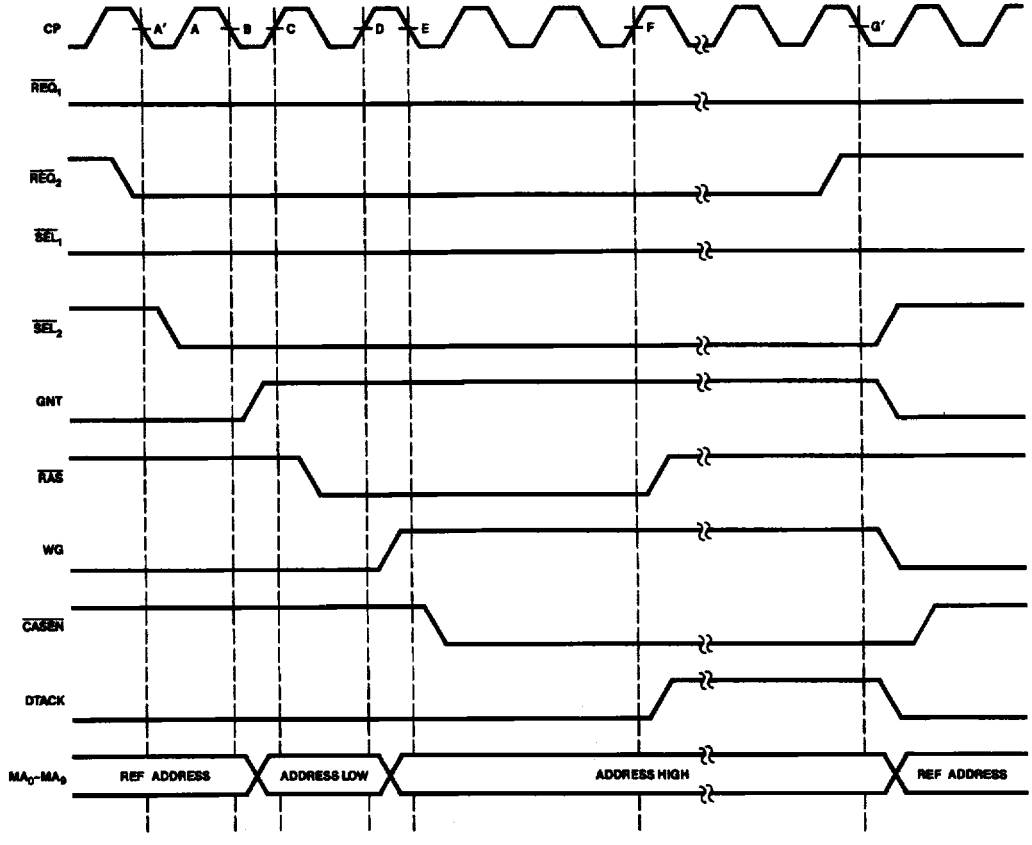


Figure 13. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing for F1764-1/1765-1

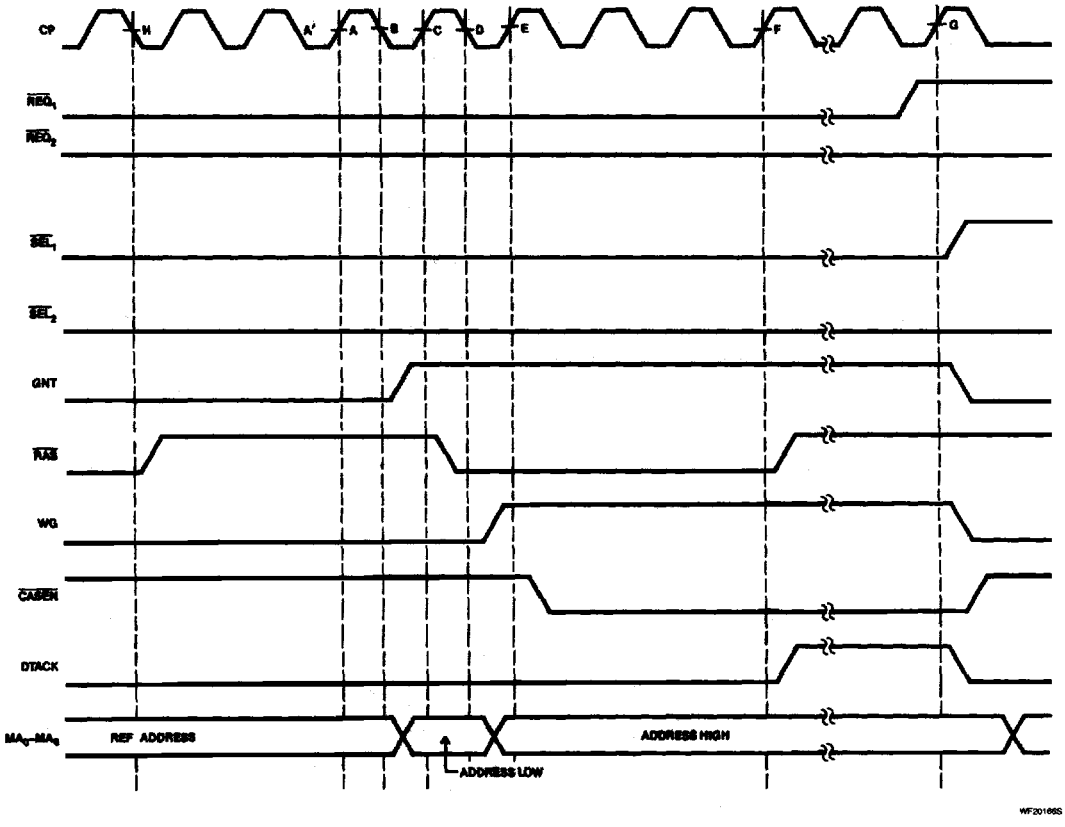


Figure 14. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing Following a Refresh Cycle for F1764-1/1765-1

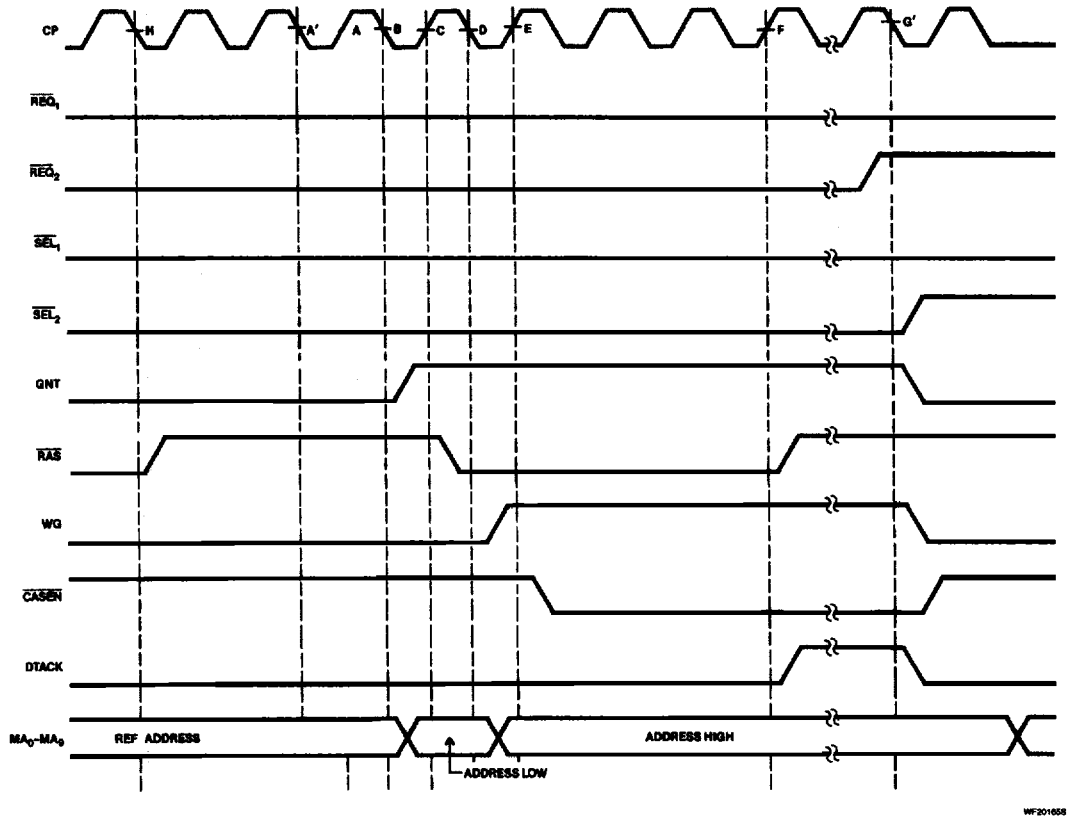


Figure 15. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing Following a Refresh Cycle for F1764-1/1765-1

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F1764/1765	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F1764/1765			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current[1]			−15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature	0		70	°C

NOTE:
1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for a detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F1764/1765			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
V_{OH2}[3]	High-level output voltage			I_{OH2}[3] = −35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{OL2}[4]	Low-level output voltage			I_{OL2}[4] = 60mA	±5%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OS}	Short-circuit output current[5]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				150	200	mA
		I_{CCL}					165	210	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Refer to Appendix A.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER[1]	74F1764/1765					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 300pF$, $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 300pF$, $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	100	150		100		MHz
t_{PLH}	Propagation delay CP(G) to $\overline{SEL}_1$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL}_1$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(G') to $\overline{SEL}_2$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(A') to $\overline{SEL}_2$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(B) to GNT	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G') to GNT	5	10	15	5	16	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(row address)	5 5	12 11	17 15	5 5	18 16	ns
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(D) to WG	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G') to WG	8	13	17	8	18	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(column address)	5 5	12 10	17 15	5 5	18 16	ns
t_{PLH}	Propagation delay CP(G or G') to $\overline{CASEN}$	7	17	23	7	25	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(F) to DTACK	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G') to DTACK	6	13	17	5	18	ns
	74F1765 Only						
t_{PLH} t_{PHL}	Propagation delay $RA_0 - RA_9$, $CA_0 - CA_9$ to $MA_0 - MA_9$	4 2	7 5	12 8	4 4	13 9	ns

NOTE:
1. For test conditions, see the AC waveforms.

AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER[2]	74F1764/1765					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 300pF$, $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 300pF$, $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP	2 2			2 2		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ}_1$, $\overline{REQ}_2$	2 2			3 3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	5 5			5 5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low	10 10			10 10		ns
	74F1764 Only						
$t_s(H)$ $t_s(L)$	Setup time, High or Low $RA_0 - RA_9$, $CA_0 - CA_9$ to CP($\downarrow$)	-4^1 -4			-5 -5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP($\downarrow$) to $RA_0 - RA_9$, $CA_0 - CA_9$	5 5			5 5		ns

NOTES:
1. These numbers indicate that the address inputs have a negative setup time and could be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.
2. For the test conditions, see the AC waveforms.

6

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F1764-1/1765-1	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F1764-1/1765-1			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current[1]			−20	mA
I_{OL}	Low-level output current[1]			8	mA
T_A	Operating free-air temperature	0		70	°C

NOTE:
1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for a detailed discussion.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F1764-1/1765-1			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −20mA	±10%V_{CC}	2.4	2.7		V
					±5%V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 8mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{OL2}[3]	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL2}[3] = 75mA	±5%V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.7	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.2	−0.6	mA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX			−80	−150	−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				120	165	mA
		I_{CCL}					125	170	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	74F1764-1/1765-1					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	150	175		100		MHz
t_{PLH}	Propagation delay CP(G) to $\overline{SEL}_1$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL}_1$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(G') to $\overline{SEL}_2$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A') to $\overline{SEL}_2$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(B) to GNT	9	12	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G') to GNT	20	23	26	17	28	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(row address)	11 14	14 18	17 22	10 13	19 24	ns
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	11	14	16	10	18	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	13	17	20	12	22	ns
t_{PLH}	Propagation delay CP(D) to WG	9	11	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G') to WG	20	23	26	19	26	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(column address)	12 14	14 18	17 21	11 13	19 23	ns
t_{PLH}	Propagation delay CP(G or G') to $\overline{CASEN}$	14	17	20	12	22	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	14	16	19	13	21	ns
t_{PLH}	Propagation delay CP(F) to DTACK	10	12	15	9	17	ns
t_{PHL}	Propagation delay CP(G or G') to DTACK	20	23	26	19	28	ns
	74F1765-1 Only						
t_{PLH} t_{PHL}	Propagation delay $RA_0 - RA_9$, $CA_0 - CA_9$ to $MA_0 - MA_9$	9 9	11 12	14 15	8 8	16 17	ns

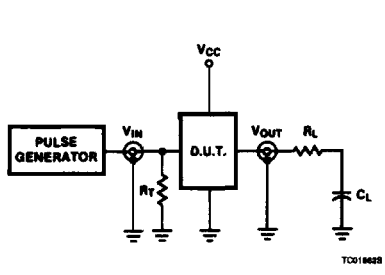
AC SETUP AND HOLD REQUIREMENTS

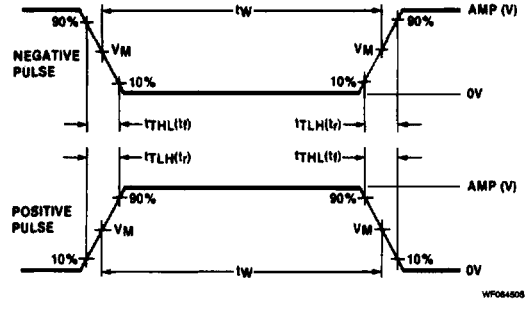
SYMBOL	PARAMETER	TEST CONDITIONS	74F1764-1/1765-1					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP	AC Waveforms	3	1		4		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ}_1$, $\overline{REQ}_2$		2	0		3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low		5	3		5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low		5			5		ns
	74F1764-1 Only							
$t_s(H)$ $t_s(L)$	Setup time, High or Low $RA_0 - RA_9$, $CA_0 - CA_9$ to CP(↓)	AC Waveforms	0	-1^1		1		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP(↓) to $RA_0 - RA_9$, $CA_0 - CA_9$		5	3		6		ns

NOTE:
1. These numbers indicate that the address inputs have a negative setup time and could be valid 1ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

6

TEST CIRCUIT AND WAVEFORMS





Test Circuit Simulating RAM Boards

V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC Characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATIONS

The 1 Megabit DRAM dual-ported controller can be designed into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (microcontrollers) and the data bus may differ in size.

Figure 16 shows two 68000 processors sharing a 4Meg × 8 (two banks each consisting of sixteen 1Meg × 1 devices) memory. Since the 68000 does not have a multiplexed address and data bus, the 'F1765/F1765-1 is appropriate.

Address bit (A_{21}) from either of the two 68000 processors distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

Upper and Lower Data Strobes ($\overline{UDS}$ and $\overline{LDS}$) from either of the two 68000 determine processors determine whether a byte or word transfer will take place. The additional circuitry is to ensure that $\overline{DTACK}$ to the 68000 is asserted only when it is selected.

Figure 17 shows two 8086 processors sharing 1MByte (two banks each consisting of sixteen 256K × 1 devices) of dynamic RAM. Using 'F1764/1764-1 in this application may eliminate the need for an external address latch.

Similarly, Figure 18 shows two 68020 processors sharing 4Mbyte of memory.

APPLICATIONS

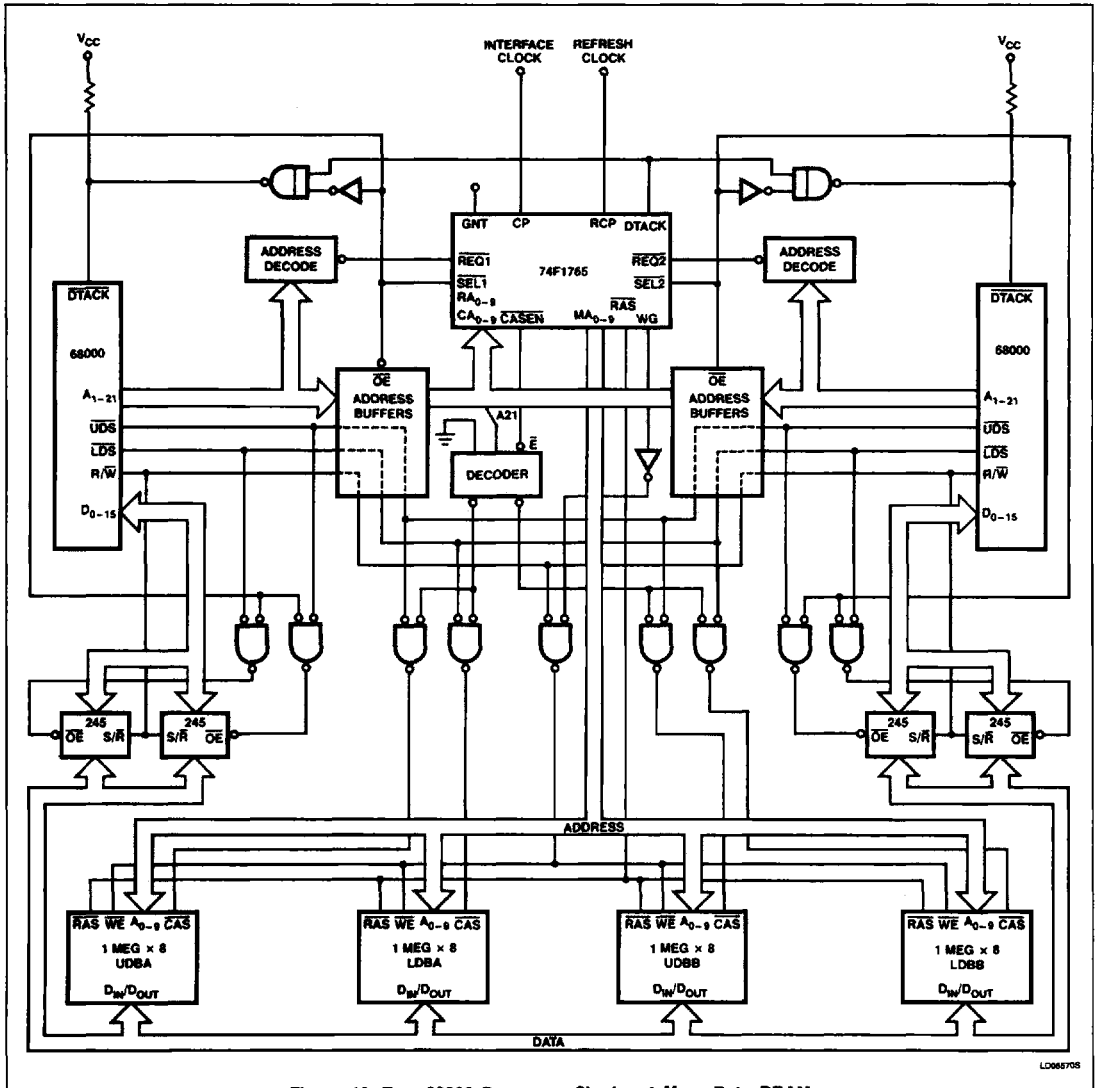
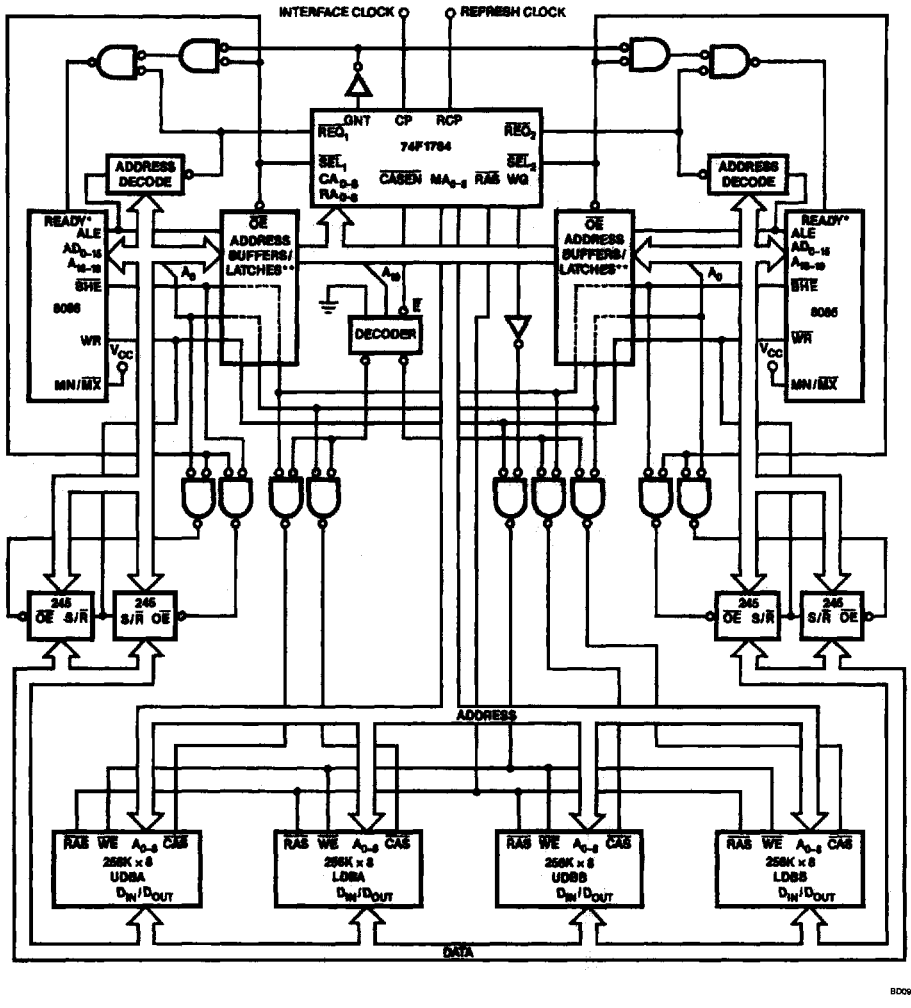


Figure 16. Two 68000 Processor Sharing 4 Mega-Byte DRAM

6

APPLICATIONS



NOTES:
* It might be necessary to synchronize READY by the 8284A. Please refer to the 8086 data sheet.
** Whether or not the 8086 address bus needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller.

Figure 17. Two 8086 Processors Sharing 1MBYTE of DRAM

APPLICATIONS

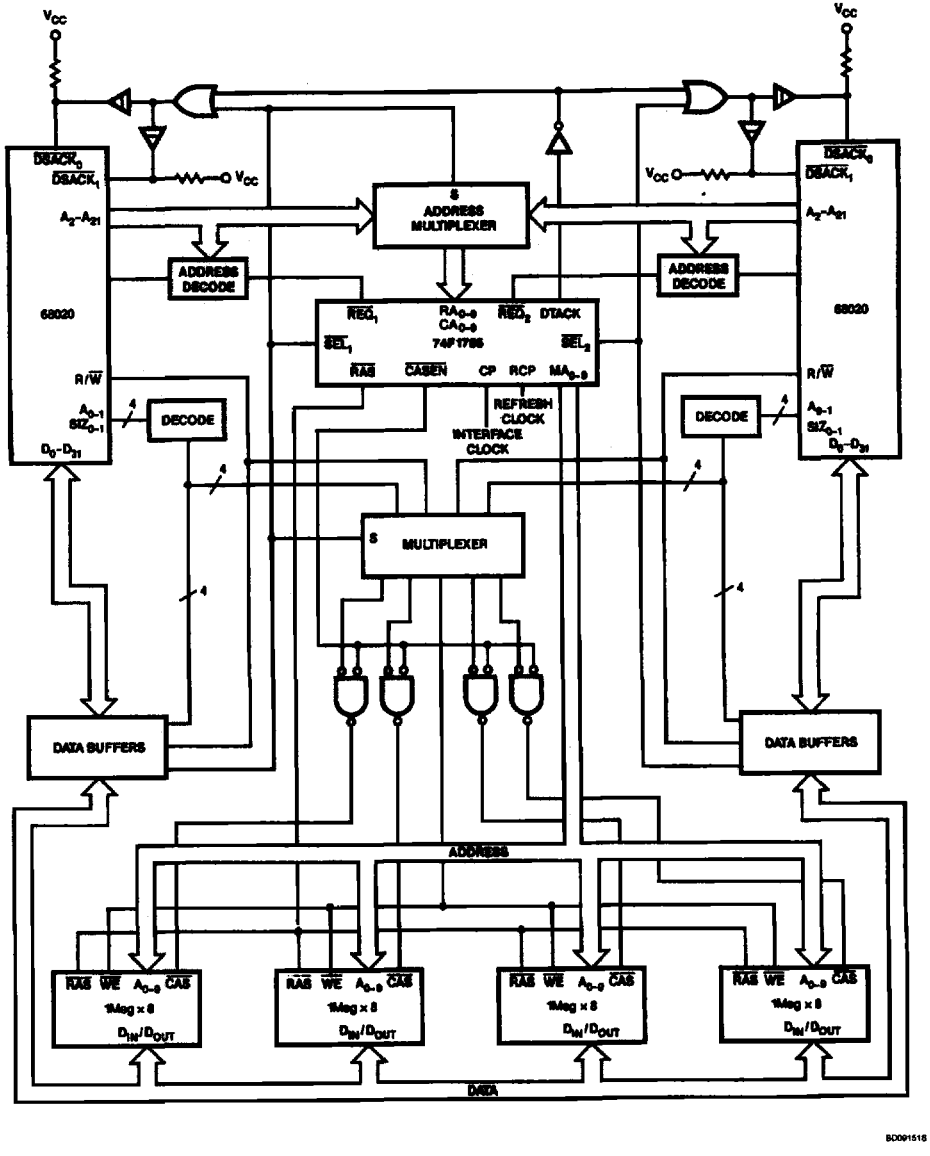


Figure 18. Two 68020 Processors Sharing 4MBYTE of DRAM

74F1764 FAMILY LINE DRIVING CHARACTERISTICS

The 74F1764/1765 are designed to provide incident wave switching in Dual-Inline-Package (DIP) or Zig-zag-Inline-Package (ZIP) housed memory arrays and first reflected wave switching in Single-Inline-Package (SIP) or Single-Inline-Module (SIM) housed arrays. The 74F1764-1/1765-1, on the other hand, are designed to provide first reflected wave switching with as wide a range of characteristic impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4 volts and must be pulled down to 0.8 volts or less on the incident wave, the DRAM Controller output must sink (4-0.8)/70A or 46mA at 0.8 volts. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be switched on the incident wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady state operation at these currents may result in electromigration).

Figures 1 – 4 show the output I/V characteristics of the DRAM Controller family of devices. These figures also demonstrate a graphical method for determining the incident wave (and first reflected wave) characteristics of the devices.

The suggested line termination for the 74F1764/1765 driving dual-in-line packaged or zig-zag packaged DRAMs is shown in Figure 8a. When driving single-in-line modules using the 74F1764/1765 or when driving any type of memory arrays with the 74F1764-1/1765-1, the schottky diode termination shown in Figure 8b can be used (most of these will need no termination at all).

Figures 5 – 7 are double exposures showing the High to Low and Low to High transitions while driving four banks of eight Dual-Inline-Packaged DRAMs. The signal line is unterminated in Figures 5 and 6, allowing the 74F1764/1765 to ring two volts below ground while the 74F1764-1/1765-1 make nice clean transitions. In Figure 7 the 74F1764/1765 is driving the same signal line but with one of its four branches terminated with its characteristic impedance in series with 300pF to ground (the worst of the four branches is shown).

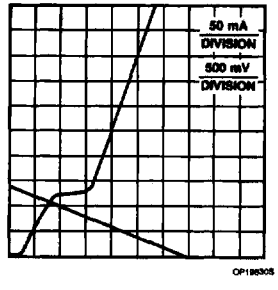


Figure 1. I-V Output Characteristics of the 74F1764/1765 in the Low State. Light Line is the I-V Curve of a 25Ω Transmission Line Settled to 3.5V (Typical for Recommended Termination). The High to Low Incident Wave on This Line Will Typically be to 0.8V

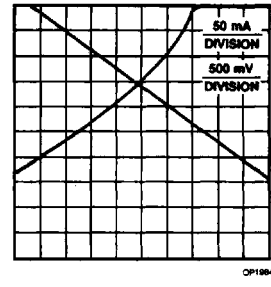


Figure 2. I-V Output Characteristics of the 74F1764/1765 in the High State. Light Line is the I-V Curve of a 35Ω Transmission Line Settled to 0.25V. The Incident Wave on the Low to High Transition Will Typically be to 2.4V on This Line. Any Line Over 35Ω Will Typically be Switched on the Incident Wave

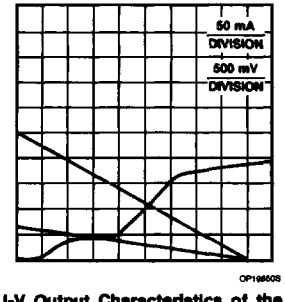


Figure 3. I-V Output Characteristics of the 74F1764-1/1765-1 in the Low State. Any Unterminated Line Impedance Between 18Ω and 70Ω (Both Shown) Will Typically Switch on the First Reflected Wave Without Violating the −1V Minimum Input Voltage Specification Typical of DRAMs

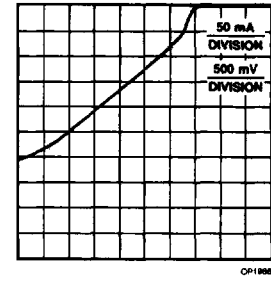


Figure 4. I-V Output Characteristics of the 74F1764-1/1765-1 While in the High State

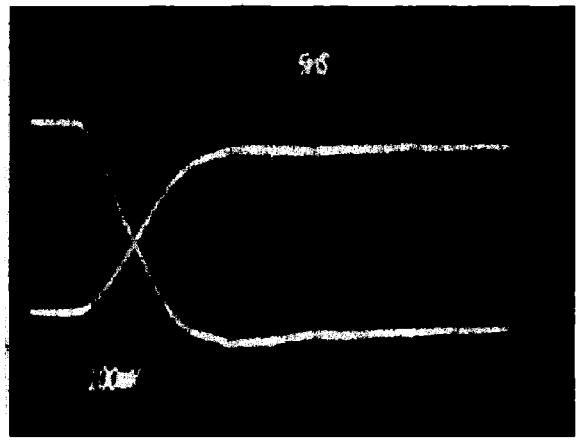


Figure 5. 74F1764-1/1765-1 Driving 32 DRAMs (Unterminated)

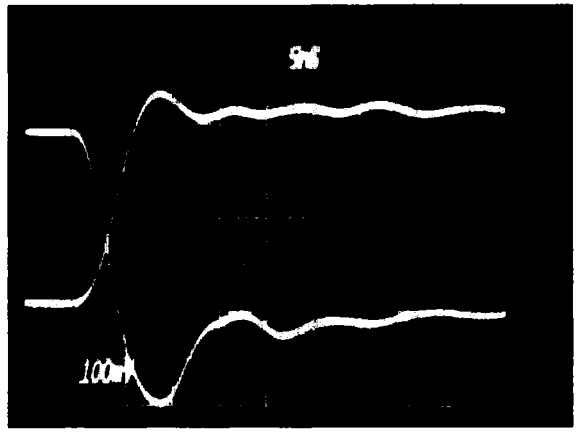


Figure 6. 74F1764/1765/1764-1/1765-1 Driving 32 DRAMs (Unterminated)

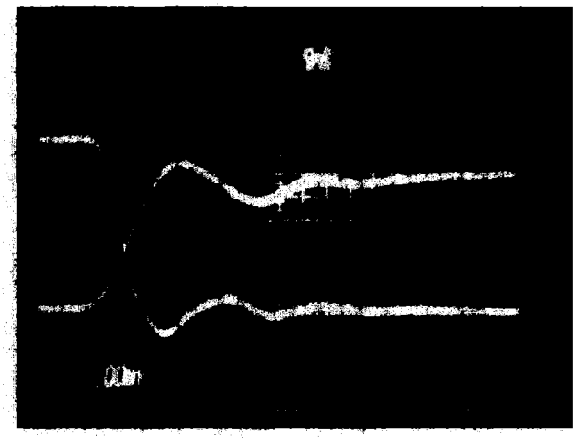
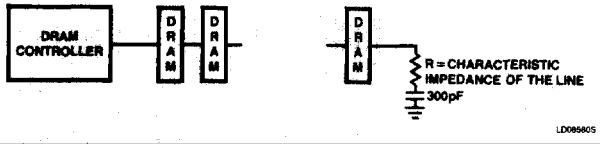


Figure 7. 74F1764/1765/1764-1/1765-1 Driving 32 DRAMs (Terminated as in Figure 8a)



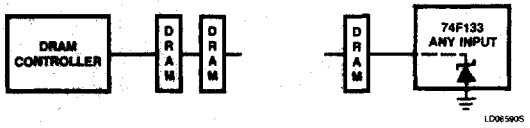


Figure 8