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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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PRELIMINARY DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD168105

MONOLITHIC 5-CHANNEL H BRIDGE DRIVER

DESCRIPTION

The μPD168105 is a monolithic 5-channel H bridge driver IC consisting of a CMOS controller and a MOS output stage. Because it uses a MOS process, this driver IC consumes less current and loses less voltage at the output stage than conventional driver ICs that use bipolar transistors. In addition, the μPD168105 employs P-channel MOSFETs in its output stage, eliminating the need for an on-chip the charge pump circuit. Therefore, the current consumption during circuit operation can significantly be reduced.

Of the five output channels, four channels are voltage drive type and the rest one is current drive type (linear drive).

The μPD168105 is housed in a 36-pin FLGA to decrease the mounting area and height. The μPD168105 allows combination of two stepper motors, one DC motor and one coil to work. Therefore, it is ideal for the motor driver of digital still cameras.

FEATURES

- Five H bridge circuits employing power MOSFETs
  Voltage drive type: 4 channels, current drive type (constant current linear drive): 1 channel
- Low current consumption due to elimination of charge pump circuit
- Input logic frequency: 100 kHz supported
- 3 V power supply supported
  Minimum operating supply voltage: 2.5 V
- Low voltage malfunction prevention circuit
  Internal circuit shutdown at V_{DD} < 2.3 V
- On-chip overheat protection circuit
- 36-pin plastic FLGA (4 x 4)

ORDERING INFORMATION

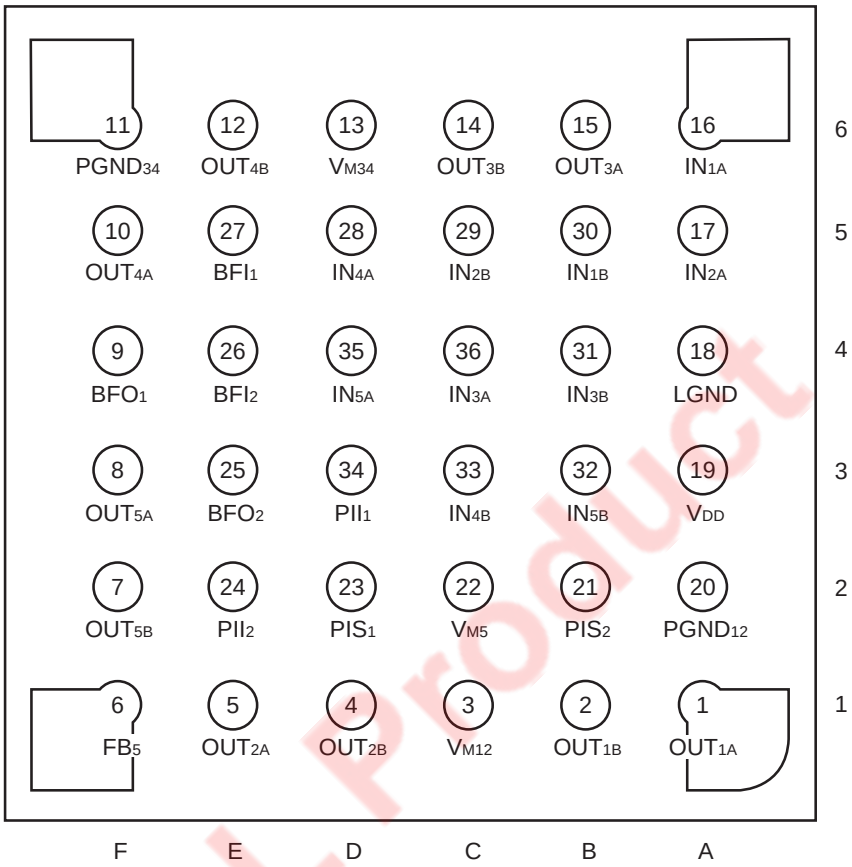
Part Number	Package	Packing Type
μPD168105FC-AA3-E1-A Note	36-pin plastic FLGA (4 x 4)	Embossed taping

Note Pb-free (This product does not contain Pb in external electrode and other parts).

Document No. S18620EJ1V0DS00 (1st edition)
Date Published March 2007 NS CP(N)
Printed in Japan

1. PIN CONNECTION (Bottom View)

Package: 36-pin plastic FLGA (4 x 4)

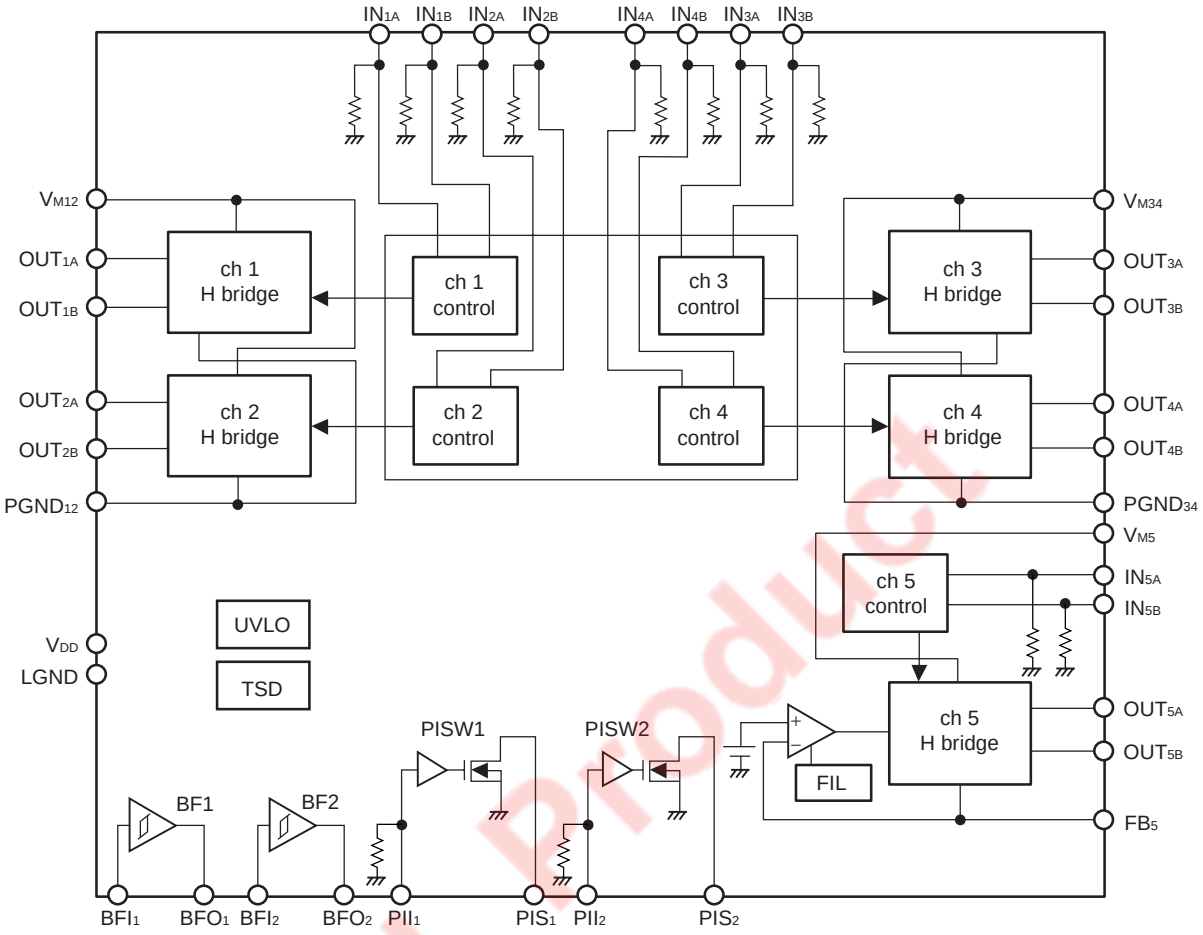


Caution Connect V_{M12}, V_{M34} and V_{M5} to make their potentials all the same, without becoming open (V_{M12}, V_{M34} and V_{M5} are connected internally).

2. PIN FUNCTIONS

Pin No.		Pin Name	Function
1	A1	OUT_{1A}	H bridge 1 output pin A
2	B1	OUT_{1B}	H bridge 1 output pin B
3	C1	V_{M12}	H bridge 1 to 5 power supply pin
4	D1	OUT_{2B}	H bridge 2 output pin B
5	E1	OUT_{2A}	H bridge 2 output pin A
6	F1	FB_5	Current sensing resistor connection pin 5
7	F2	OUT_{5B}	H bridge 5 output pin B
8	F3	OUT_{5A}	H bridge 5 output pin A
9	F4	BFO_1	Buffer amp 1 output pin
10	F5	OUT_{4A}	H bridge 4 output pin A
11	F6	$PGND_{34}$	H bridge 1 to 4 GND pin
12	E6	OUT_{4B}	H bridge 4 output pin B
13	D6	V_{M34}	H bridge 1 to 5 power supply pin
14	C6	OUT_{3B}	H bridge 3 output pin B
15	B6	OUT_{3A}	H bridge 3 output pin A
16	A6	IN_{1A}	H bridge 1 input pin A
17	A5	IN_{2A}	H bridge 2 input pin A
18	A4	LGND	Logic part GND pin
19	A3	V_{DD}	Logic part power supply pin
20	A2	$PGND_{12}$	H bridge 1 to 4 GND pin
21	B2	PIS_2	PI switch 2 output pin (open drain)
22	C2	V_{M5}	H bridge 1 to 5 power supply pin
23	D2	PIS_1	PI switch 1 output pin (open drain)
24	E2	PII_2	PI switch 2 input pin
25	E3	BFO_2	Buffer amp 2 output pin
26	E4	BFI_2	Buffer amp 2 input pin
27	E5	BFI_1	Buffer amp 1 input pin
28	D5	IN_{4A}	H bridge 4 input pin A
29	C5	IN_{2B}	H bridge 2 input pin B
30	B5	IN_{1B}	H bridge 1 input pin B
31	B4	IN_{3B}	H bridge 3 input pin B
32	B3	IN_{5B}	H bridge 5 input pin B
33	C3	IN_{4B}	H bridge 4 input pin B
34	D3	PII_1	PI switch 1 input pin
35	D4	IN_{5A}	H bridge 5 input pin A
36	C4	IN_{3A}	H bridge 3 input pin A

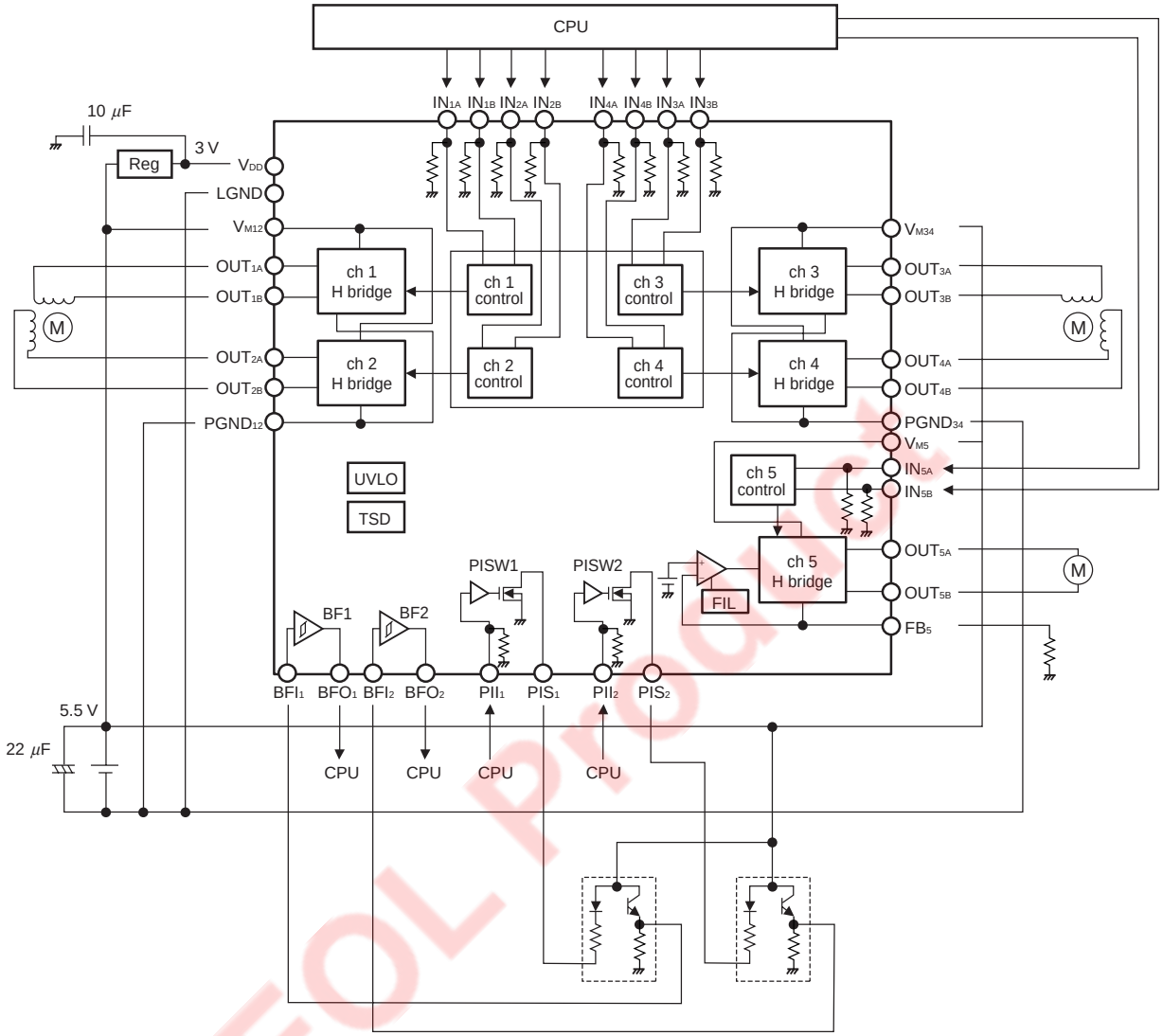
3. BLOCK DIAGRAM



Cautions 1. Connect V_{M12}, V_{M34} and V_{M5} to make their potentials all the same, without becoming open (V_{M12}, V_{M34} and V_{M5} are connected internally).

2. A pull-down resistor is connected to the following pins: IN_{1A}, IN_{1B}, IN_{2A}, IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}, PII_1, PII_2.

4. EXAMPLE OF STANDARD CONNECTION



Cautions 1. Connect V_{M12}, V_{M34} and V_{M5} to make their potentials all the same, without becoming open (V_{M12}, V_{M34} and V_{M5} are connected internally).

2. A pull-down resistor is connected to the following pins: IN_{1A}, IN_{1B}, IN_{2A}, IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}, PII_1, PII_2.

3. This circuit diagram is shown as an example of connection, and is not intended for mass production design.

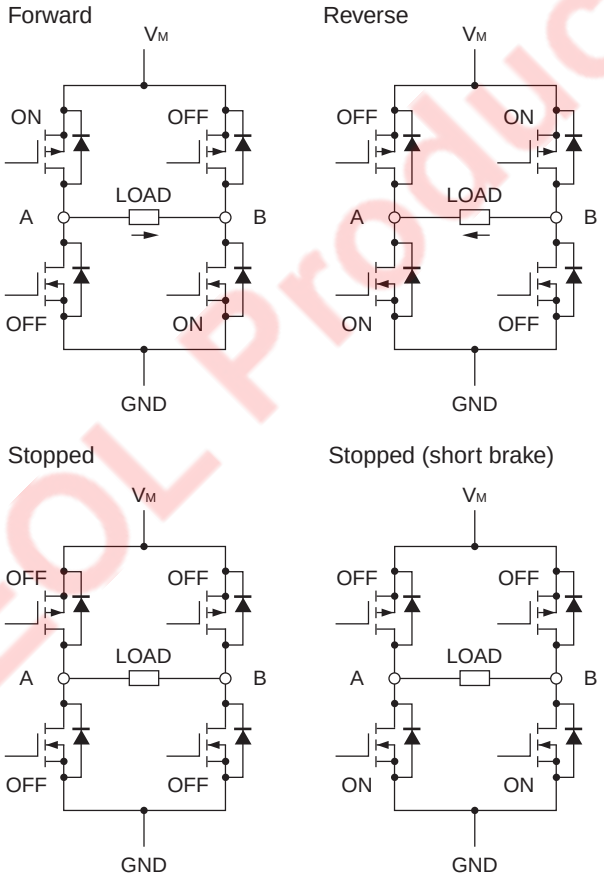
5. FUNCTION OPERATION TABLE

The logic of each channel is shown in the table below.

I/O Truth Table for Ch 1 to Ch 4

Input		Output		Output Status
$IN_{1A}/IN_{2A}/IN_{3A}/IN_{4A}$	$IN_{1B}/IN_{2B}/IN_{3B}/IN_{4B}$	OUT_A	OUT_B	
L	L	Hi-Z	Hi-Z	Stopped (output open, standby)
L	H	L	H	Reverse ($OUT_B \rightarrow OUT_A$)
H	L	H	L	Forward ($OUT_A \rightarrow OUT_B$)
H	H	L	L	Stopped (short brake)

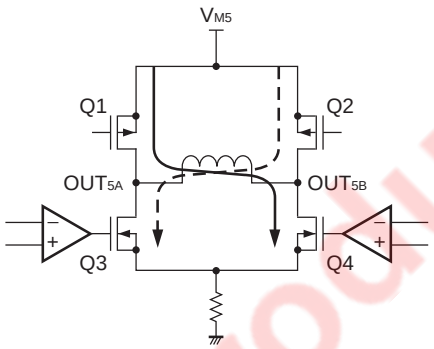
Remark H: High level, L: Low level, Hi-Z: High impedance



I/O Truth Table for Ch 5

Input		Output		H Bridge Output Status			
IN_{5A}	IN_{5B}	OUT_{5A}	OUT_{5B}	Q1	Q2	Q3	Q4
L	L	Hi-Z	Hi-Z	OFF	OFF	OFF	OFF
L	H	L (Linear)	H	OFF	ON	ON (Linear)	OFF
H	L	H	L (Linear)	ON	OFF	OFF	ON (Linear)
H	H	Hi-Z	Hi-Z	OFF	OFF	OFF	OFF

Remark H: High level, L: Low level, Hi-Z: High impedance



6. FUNCTION DEVELOPMENT

6.1 Standby Function

The μPD168105 does not have any standby function.

In order to contain self consumption current, shut down the IC operation by turning V_{DD} into GND level.

6.2 Test Function

The μPD168105 contains a test circuit used during product inspections.

The test circuit operates by setting all the signal of the input pins of ch 1 to ch 5 (IN_{1A}, IN_{1B}, IN_{2A}, IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}), buffer amp input pins (BFI_1, BFI_2), and PI switch input pins (PII_1, PII_2) to high level.

This function must not be used during normal use.

Caution When a test circuit operates, the arrangement and function of pin differ from those of this specification. Therefore, avoid a design in which signals of all the input pins (IN_{1A}, IN_{1B}, IN_{2A}, IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}, BFI_1, BFI_2, PII_1, PII_2) achieve high level at the same time.

6.3 Overheat Protection Function

This is a function to shut down a driver output, for preventing damages due to an increase of a chip temperature in μPD168105.

The overheat protection circuit operates when the temperature of a chip is 150°C or more. When overheat is detected, outputs of ch 1 to ch 5 stop (high impedance).

Caution Note that outputs of buffer amp output pins (BFO_1, BFO_2) and PI switch output pins (PIO_1, PIO_2) do not stop.

7. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_A = 25°C, glass epoxy 4-layer board of 100 mm x 100 mm x 1.6 mm with copper foil area of 50%)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	Control block	−0.5 to +4.0	V
	V_M	Motor block	−0.5 to +6.5	V
Input pin voltage	V_{IN}	IN_{1A}, IN_{1B}, IN_{2A}, IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}, BFI_1, BFI_2, PII_1, PII_2	−0.5 to V_{DD} + 0.5	V
Output pin voltage	V_{OUT}	ch 1 to ch 5	6.5	V
BF, PI output voltage	$V_{OUT(BF, PI)}$	BFO_1, BFO_2, PIS_1, PIS_2	V_{DD}	V
DC input current (PI)	$I_{IN(PI)}$	PIS pin	+0.1	A
DC output current 1 (ch 1, ch 2)	$I_{D(DC)1}$	DC	±0.27	A/ch
DC output current 2 (ch 3, ch 4)	$I_{D(DC)2}$	DC	±0.35	A/ch
DC output current 3 (ch 5)	$I_{D(DC)3}$	DC	±0.35	A/ch
Instantaneous output current 1 (ch 1, ch 2)	$I_{D(pulse)1}$	PW < 10 ms, Duty ≤ 20%	±0.6	A/ch
Instantaneous output current 2 (ch 3, ch 4)	$I_{D(pulse)2}$	PW < 10 ms, Duty ≤ 20%	±0.9	A/ch
Instantaneous output current 3 (ch 5)	$I_{D(pulse)3}$	PW < 10 ms, Duty ≤ 20%	±0.8	A/ch
Power consumption	P_T		0.78	W
Peak junction temperature **Note**	$T_{ch(MAX.)}$		150	°C
Storage temperature	T_{stg}		−55 to +150	°C

Note The overheat protection circuit operates at T_{ch} > 150°C. When overheat is detected, all circuits are stopped, while the outputs of buffer amp output pin (BFO_1, BFO_2) and PI switch output pin (PIO_1, PIO_2) are not.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = 25°C, glass epoxy 4-layer board of 100 mm x 100 mm x 1.6 mm with copper foil area of 50%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	Control block	2.5		3.6	V
	V_M	Motor block	2.7		6.0	V
Input voltage	V_{IN1}	IN_{1A}, IN_{1B}, IN_{2A}, IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}, BFI_1, BFI_2, PII_1, PII_2	0		V_{DD}	V
DC input current (PI)	$I_{IN(PI)}$	PIS pin			+0.05	A
DC output current 1 (ch 1, ch 2)	$I_{D(DC)1}$	DC	−0.2		+0.2	A/ch
DC output current 2 (ch 3, ch 4)	$I_{D(DC)2}$	DC	−0.34		+0.34	A/ch
DC output current 3 (ch 5)	$I_{D(DC)3}$	DC	−0.3		+0.3	A/ch
Instantaneous output current 1 (ch 1, ch 2)	$I_{D(pulse)1}$	PW < 10 ms, Duty ≤ 20%	−0.4		+0.4	A/ch
Instantaneous output current 2 (ch 3, ch 4)	$I_{D(pulse)2}$	PW < 10 ms, Duty ≤ 20%	−0.7		+0.7	A/ch
Instantaneous output current 3 (ch 5)	$I_{D(pulse)2}$	PW < 10 ms, Duty ≤ 20%	−0.6		+0.6	A/ch
Logic input frequency	f_{IN}				100	kHz
Operating temperature range	T_A		−10		75	°C
Peak junction temperature **Note**	$T_{ch(MAX.)}$				125	°C

Note The overheat protection circuit operates at T_{ch} > 150°C. When overheat is detected, all circuits are stopped, while the outputs of buffer amp output pin (BFO_1, BFO_2) and PI switch output pin (PIO_1, PIO_2) are not.

Electrical Characteristics (Unless otherwise specified, T_A = 25°C, V_{DD} = 3 V, V_M = 5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} pin current during operation	$I_{DD(ACT)}$				1.0	mA
V_M pin current in during operation	$I_{M(ACT)}$	V_M = 5.5 V, all control pins are low level			0.5	mA
High level input current	I_{IH}	$V_{IN} = V_{DD}$			60	μA
Low level input current	I_{IL}	V_{IN} = 0 V	−1.0			μA
V_M pin circuit leakage current Note	$I_{M(OFF)}$	V_M = 5.5 V, V_{DD} = 0 V			1	μA
Input pull-down resistor	R_{IND1}	IN_{1A}, IN_{1B}, IN_{2A}, IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}	50	125	200	kΩ
	R_{IND2}	PII_1, PII_2	150	300	600	kΩ
High level input voltage	V_{IH}	2.5 V ≤ V_{DD} ≤ 3.6 V, IN_{1A}, IN_{1B}, IN_{2A}, IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}, PII_1, PII_2	0.7 xV_{DD}			V
Low level input voltage	V_{IL}	2.5 V ≤ V_{DD} ≤ 3.6 V, IN_{1A}, IN_{1B}, IN_{2A}, IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}, PII_1, PII_2			0.3 xV_{DD}	V
H bridge on-resistance 1 (ch 1, ch 2)	R_{ON1}	I_M = 0.1 A, sum of the top and bottom stages		1.3	1.8	Ω
H bridge on-resistance 2 (ch 3, ch 4)	R_{ON2}	I_M = 0.1 A, sum of the top and bottom stages		1.4	1.8	Ω
H bridge on-resistance 3 (ch 5)	R_{ON3}	I_M = 0.1 A, sum of the top and bottom stages		1.3	2.0	Ω
Internal reference voltage	V_{FB5}	FB_5 pin input threshold voltage	0.1187	0.125	0.1313	V
Detection voltage at low voltage	V_{DDS}				2.3	V
Output turn on time	t_{ON}	R_M = 20 Ω, refer to **8. SWITCHING CHARACTERISTICS WAVEFORMS**		0.7	2.0	μs
Output turn off time	t_{OFF}	R_M = 20 Ω, refer to **8. SWITCHING CHARACTERISTICS WAVEFORMS**		0.2	0.5	μs
Rising time	t_r	R_M = 20 Ω, refer to **8. SWITCHING CHARACTERISTICS WAVEFORMS**		0.3		μs
Falling time	t_f	R_M = 20 Ω, refer to **8. SWITCHING CHARACTERISTICS WAVEFORMS**		0.1		μs
PISW on-resistance	$R_{ON(PI)}$	I = 0.1 A, PISW1, PISW2		5	10	Ω
BF high level input voltage	$V_{IH(BF)}$	During triangular wave 100 Hz input, BFI_1, BFI_2	0.9	1.3	1.7	V
BF low level input voltage	$V_{IL(BF)}$	During triangular wave 100 Hz input, BFI_1, BFI_2	0.6	1.0	1.4	V
BF HYS width	$V_{H(BF)1}$	During triangular wave 100 Hz input, BFI_1, BFI_2	0.1	0.3	0.5	V
	$V_{H(BF)2}$	During triangular wave 100 Hz input, BFI_1, BFI_2	(0.2)	(0.3)	(0.5)	V

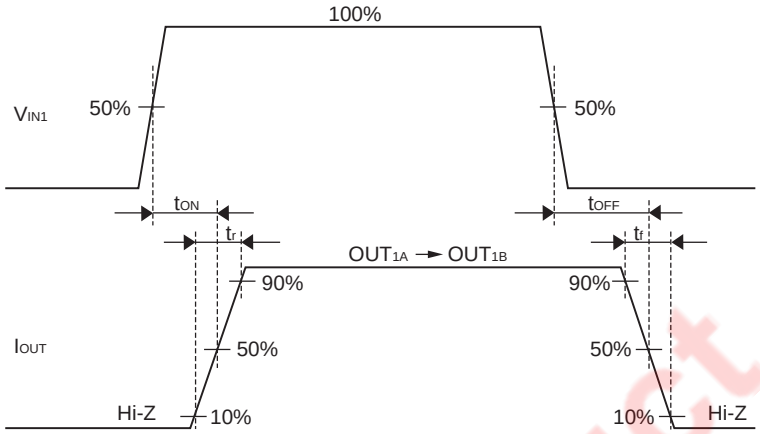
Note A breaking circuit which prevents V_M pin current from flowing during V_{DD} = 0 V is contained.

Remark The values shown in parentheses are those at the time of design, and is reference values.

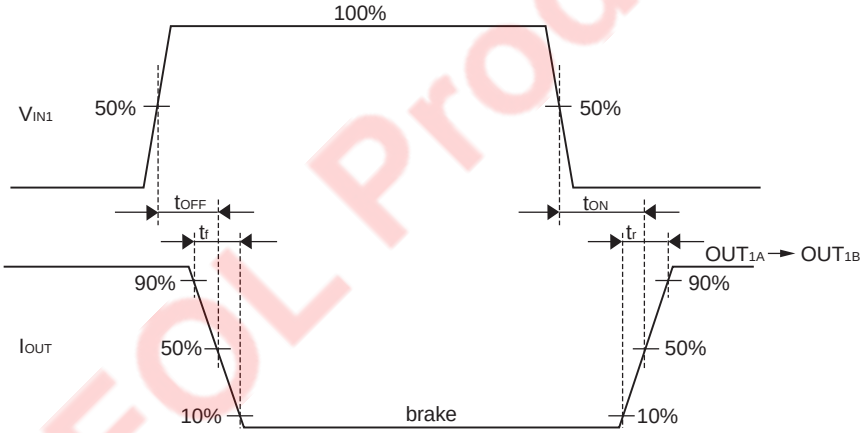
8. SWITCHING CHARACTERISTICS WAVEFORMS

H Bridge Switching Waveform

(1) IN_2 = "L"



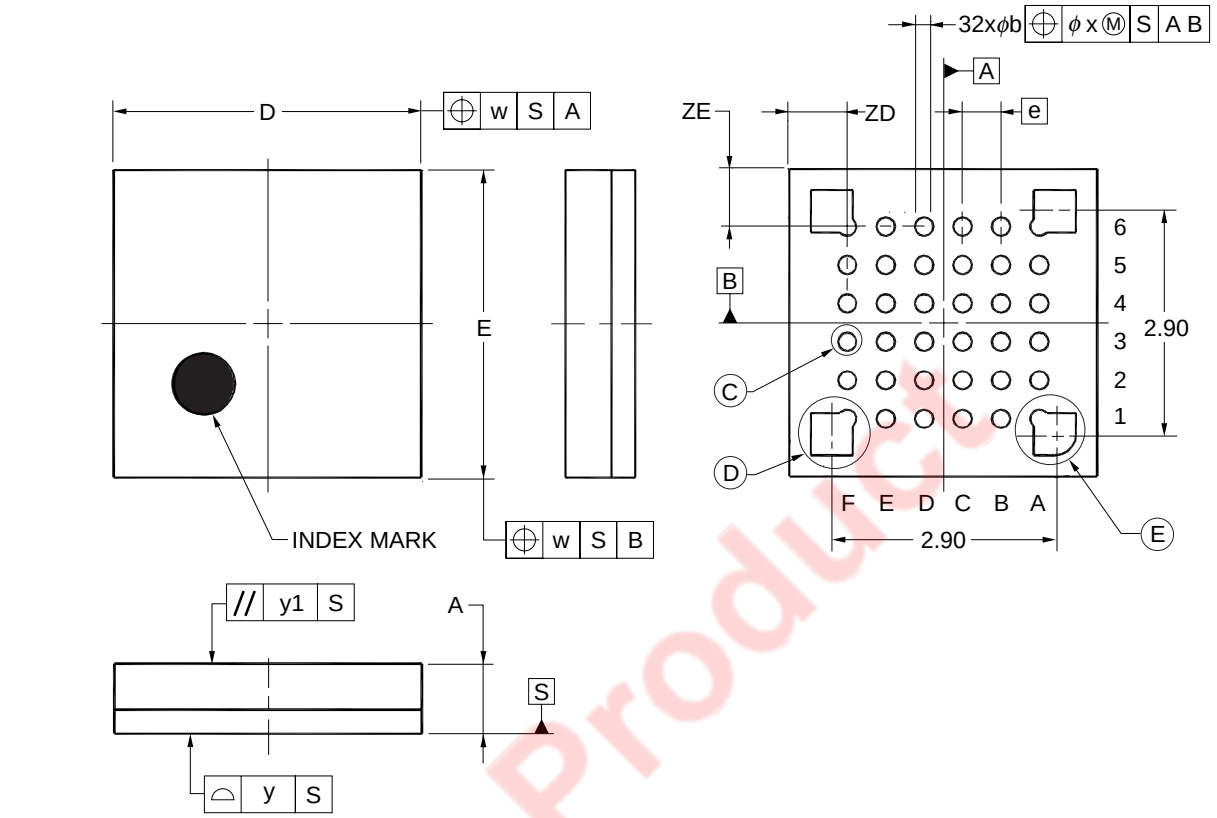
(2) IN_2 = "H"

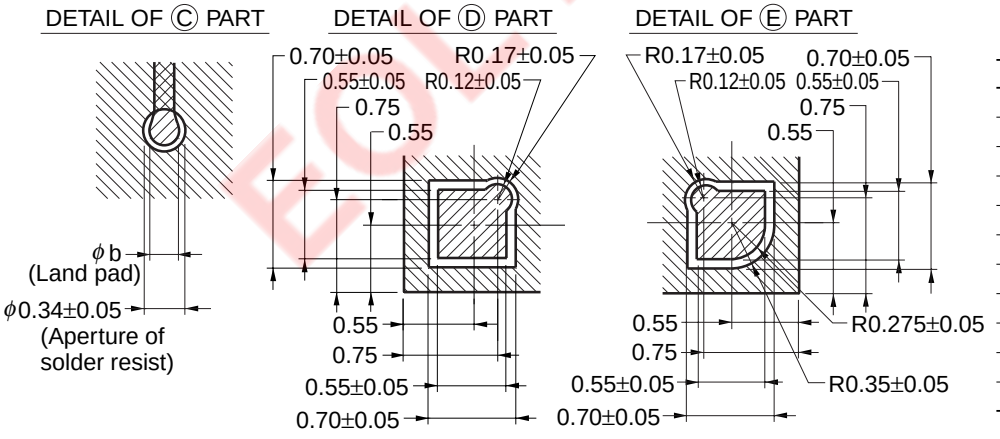


A high impedance period of approx. 50 ns is secured to prevent through current during mode selection.

9. PACKAGE DRAWING

36-PIN PLASTIC FLGA (4x4)





(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.20
e	0.50
A	0.91±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P36FC-50-AA3-2

10. RECOMMENDED SOLDERING CONDITIONS

The μD168105 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended, contact an NEC sales representative. For technical contents of the recommended soldering conditions, refer to the following:

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

μPD168105FC-AA3-E1-A [Note1]: 36-pin plastic FLGA (4 x 4)

Process	Conditions	Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds or less (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days [Note2] (after that, prebake at 125°C for 10 hours) , Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Precaution> Products other than in heat-resistant trays (such as those packaged in a magazine, taping, or non-thermal-resistant tray) cannot be baked in their package.	IR60-107-3

Notes 1. Pb-free (This product does not contain Pb in external electrode and other parts).

2. After opening the dry pack, store it a 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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