FUJITSU

PRODUCT PROFILE

MB85236-80/-10/-12

CMOS 1M x 9 NIBBLE MODE DRAM MODULE

The Fujitsu MB85236 is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of nine MB81C1001 devices. The MB85236 is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85236 are the same as the MB81C1001 devices which feature nibble mode operation. For ease of memory expansion, the MB85236 is offered in a 30-pad Single In-Line Memory Module (SIMM).

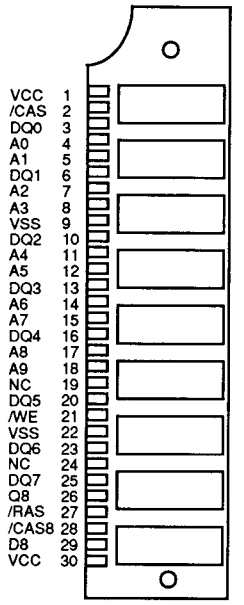
- Organization:
  1,048,576 words x 9 bit
- RAS Access time:
  80ns max. (MB85236-80)
  100ns max. (MB85236-10)
  120ns max. (MB85236-12)
- CAS Access Time:
  25ns max. (MB85236-80)
  25ns max. (MB85236-10)
  35ns max. (MB85236-12)
- Nibble Mode Cycle Time:
  50ns max. (MB85236-80)
  55ns max. (MB85236-10)
  60ns max. (MB85236-12)
- Nibble Mode Operation
- Active Power:
  3465mW max. (MB85236-80)
  2970mW max. (MB85236-10)
  2475mW max. (MB85236-12)
- Standby Power:
  50mW max. (CMOS Level)
  99mW max. (TTL Level)
- Single +5V Supply ±10% Tolerance
- TTL Compatible I/O
- Decoupling Capacitor:
  0.22µF, 9pcs
- JEDEC Standard Package Outline:
  30-pin SIP (MB85236-XX PL)
  30-pad SIMM (MB85236-XX PS)

PRELIMINARY

PLASTIC PACKAGE
MSS-30P-P03

PLASTIC PACKAGE
MSP-30P-P04

PAD ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Rating
Supply Voltage	VCC	-1.0 to +7.0	V
Input Voltage	VIN	-1.0 to +7.0	V
Output Voltage	VOUT	-1.0 to +7.0	V
Short Circuit Output Current	IOUT	±50	mA
Power Dissipation	PD	9.0	W
Storage Temperature	TSTG	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CAPACITANCE (TA=25°C,f=1MHz)

PARAMETER	SYMBOL	VALUE		UNIT
		Typ	Max	
Input Capacitance, A0-9	CIN1	-	60	pF
Input Capacitance, /RAS	CIN2	-	49	pF
Input Capacitance, /CAS	CIN3	-	49	pF
Input Capacitance,/CAS8	CIN4	-	9	pF
Input Capacitance, /WE	CIN5	-	48	pF
Input Capacitance,D8	CIN6	-	8	pF
I/O Capacitance, DQ0-7	CI/O	-	14	pF
Output Capacitance, Q8	COUT	-	10	pF

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DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted) *

PARAMETER		SYMBOL	CONDITIONS	VALUE			UNIT	NOTE
				Min	Typ	Max		
Output High Level		VOH	IOH= -5mA	2.4	-	-	V	
Output Low Level		VOL	IOL=4.2mA	-	-	0.4	V	
Input Leakage Current		IIL1 (/CAS8, D8)	0V ≤VIN ≤5.5V; 4.5≤VCC≤5.5V	-10	-	10	µA	
		IIL2 (Others)	VSS=0V; all other pins not under test=0V	-30		30		
Output Leakage Current		IOL	0V ≤VOUT ≤5.5V; Data out disabled	-10	-	10	µA	
Operating Current (Average Power Supply Current)	MB85236-80	ICC1	/RAS & /CAS cycling; tRC=min.	-	-	630	mA	*
	MB85236-10					540		
	MB85236-12					450		
Standby Current (Power Supply Current)	TTL Level	ICC2	/RAS=/CAS=VIH	-	-	18	mA	
	CMOS Level		/RAS=/CAS ≥ VCC -0.2V			9		
Ref. Current # 1 (Average Power Supply Current)	MB85236-80	ICC3	/CAS=VIH, /RAS cycling; tRC=min.	-	-	585	mA	*
	MB85236-10					495		
	MB85236-12					405		
Nibble Mode Current	MB85236-80	ICC4	/RAS=VIL, /CAS cycling tPC=min.	-	-	405	mA	*
	MB85236-10					360		
	MB85236-12					297		
Ref. Current # 2 (Average Power Supply Current)	MB85236-80	ICC5	/RAS cycling; /CAS - before -/RAS; tRC=min.	-	-	585	mA	*
	MB85236-10					495		
	MB85236-12					405		

* Refer to MB81C1001 data sheet electricals for an explanation of notes.
* ICC depends on the output load conditions and cycle rate. The specific values are obtained with the output open.

AC CHARACTERISTICS

(At recommended operating conditions otherwise noted.) * Notes 1, 2, 3

PARAMETER	SYM	MB85236-80		MB85236-10		MB85236-12		UNIT	NOTE
		Min	Max	Min	Max	Min	Max		
Time Between Refresh	tREF	-	8.2	-	8.2	-	8.2	ms	
Random Read/Write Cycle Time	tRC	155	-	180	-	210	-	ns	
Access Time From /RAS	tRAC	-	80	-	100	-	120	ns	4,7
Access Time From /CAS	tCAC	-	25	-	25	-	35	ns	5,7
Column Address Access Time	tAA	-	45	-	50	-	60	ns	6,7
Output Hold Time	tOH	7	-	7	-	7	-	ns	
Output Buffer Turn On Delay Time	tON	5	-	5	-	5	-	ns	
Output Buffer Turn Off Delay Time	tOFF	-	25	-	25	-	25	ns	8
Input Transition Time	tT	3	50	3	50	3	50	ns	
/RAS Precharge Time	tRP	65	-	70	-	80	-	ns	
/RAS Pulse Width	tRAS	80	100K	100	100K	120	100K	ns	
/RAS Hold Time	tRSH	25	-	25	-	35	-	ns	
/RAS To /CAS Precharge Time	tCRP	0	-	0	-	0	-	ns	
/CAS To /RAS Delay Time	tRCD	22	55	25	70	25	85	ns	9,10
/CAS Pulse Width	tCAS	25		25	-	35	-	ns	
/CAS Hold Time	tCSH	80	-	100	-	120	-	ns	
/CAS Precharge Time(C-B-R Refresh)	tCPN	10	-	10	-	10	-	ns	15
Row Addresss Setup Time	tASR	0	-	0	-	0	-	ns	
Row Address Hold Time	tRAH	12	-	15	-	15	-	ns	
Column Address Setup Time	tASC	0	-	0	-	0	-	ns	
Column Address Hold Time	tCAH	15	-	15	-	20	-	ns	
/RAS to Column Address Delay Time	tRAD	17	35	20	50	20	60	ns	11
Column Address To /RAS Lead Time	tRAL	45	-	50	-	60	-	ns	
Read Command Setup Time	tRCS	0	-	0	-	0	-	ns	
Read Command Hold Time/Reference to /RAS	tRRH	0	-	0	-	0	-	ns	12
Read Command Hold Time/Reference to /CAS	tRCH	0	-	0	-	0	-	ns	12
Write Command Setup Time	tWCS	0	-	0	-	0	-	ns	13
Write Command Hold Time	tWCH	15	-	15	-	20	-	ns	
/WE Pulse Width	tWP	15	-	15	-	20	-	ns	
Write Command To /RAS Lead Time	tRWL	22	-	25	-	30	-	ns	
Write Command To /CAS Lead Time	tCWL	17	-	20	-	25	-	ns	
Data Input Setup Time	tDS	0	-	0	-	0	-	ns	
Data Input Hold Time	tDH	15	-	15	-	20	-	ns	
/RAS Precharge Time to /CAS Active Time Low (Refresh Cycle)	tRPC	0	-	0	-	0	-	ns	
/CAS Set Up Time (For C-B-R Refresh)	tCSR	0	-	0	-	0	-	ns	

* Refer to MB81C1001 data sheet electricals for an explanation of notes.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions otherwise noted.) Notes 1, 2, 3

PARAMETER	SYM	MB85236-80		MB85236-10		MB85236-12		UNIT	NOTE
		Min	Max	Min	Max	Min	Max		
/CAS Hold Time (For C-B-R Refresh)	tCHR	15	-	15	-	20	-	ns	
/CAS to /WE Delay time	tCWD	25	-	25	-	35	-	ns	13,15
/RAS To /WE Delay Time	tRWD	80	-	100	-	120	-	ns	13,15
Column Address to /WE Delay Time	tAWD	45	-	50	-	60	-	ns	13,15
Nibble Mode Read/Write Cycle Time	tNC	45	-	45	-	60	-	ns	
Nibble Mode Read-Modify-Write Cycle Time	tNRWC	67	-	70	-	85	-	ns	15
Access Time From /CAS Precharge	tNPA	-	40	-	40	-	55	ns	7,14
Nibble Mode /CAS Precharge Time	tNCP	10	-	10	-	15	-	ns	
Read-Modify-Write Cycle Time	tRWC	182	-	210	-	245	-	ns	15

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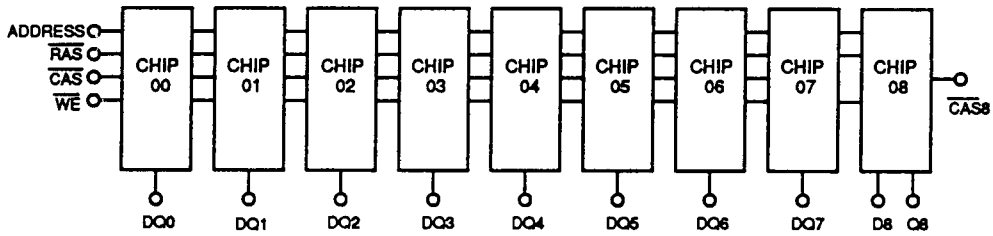
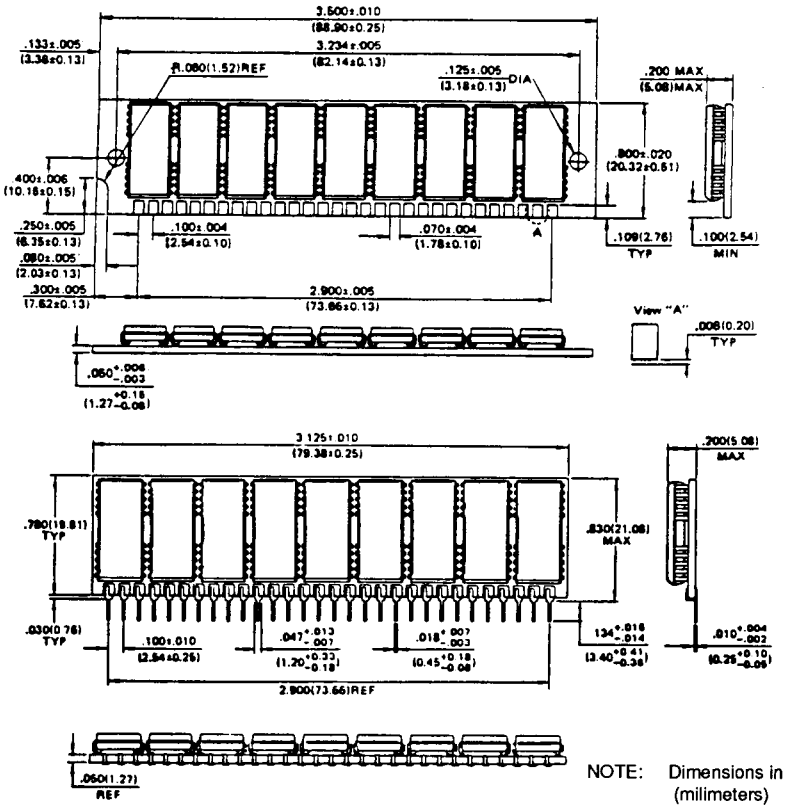
Notes:

1. An Initial Pause (RAS = CAS = VIH) of 200µs is required after power-up followed by any eight RAS - only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
2. AC characteristics assume tT = 5nS.
3. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also transition times are measured between VIH (min) and VIL (max).
4. Assumes that TRCD < tRCD (max), tRAD < tRAD (max). If rRCD is greater than the maximum recommended value shown in this table, tRAC will be increased by the amount that tRCD exceeds the value shown.
5. If tRCD > tRCD (max), tRAD > tRAD (max), and tASC > tAA - tCAC - tT, access time is tCAC.
6. If tRAD > tRAD (max) and tASC < tAA - tCAC -tT, access time is tAA.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. tOFF is specified that output buffer changes to high impedance state.
9. Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specific tRCD (max) limit, access time is controlled exclusively by tCAC or tAA.
10. tRCD (min) = tRAH (min) + 2TT + tASC (min).
11. Operation within the tRAD (max) limit ensures that tRAC (max) can be met. tRAD (max) is specified as a reference point only; if tRAD is greater than the specified tRAD (max) limit, access time is controlled exclusively by tCAC or tAA.
12. Either tRRH or tRCH must be satisfied for a read cycle.
13. tWSC, tCWD, tRWD and tWAD are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If tWCS > tWCS (min.), the cycle is an early write cycle and D8 pin will maintain high impedance state throughout the entire cycle. If tCWD > tCWD (min), tRWD > tRWD (min) and tAWD > tAWD (min), the data from the selected cell will appear at the D8 pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear to D8 pin, and write operation can be exected by satisfying tRWL, tCWL and tRAL specifications.
14. tNPA is access time from the selection of a new column address (that is caused by changing CAS / CAS8 from "L" to "H"). Therefore, if tNCP is long, tNPA is longer than tNPA (max).
15. For parity bit only.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS



NOTE: Dimensions in inches and (milimeters)

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