HARRIS

HM-65162

2048 x 8 Asynchronous CMOS Static RAM

Features

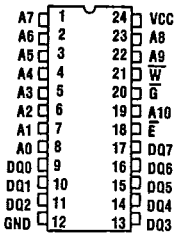
- Fast Access Time..... 55/70/90ns Max.
- Low Standby Current.....50μA Max.
- Low Operating Current..... 70mA Max.
- Data Retention at 2.0 Volts.....20μA Max.
- TTL Compatible Inputs and Outputs
- JEDEC Approved Pinout (2716, 6116 Type)
- No Clocks or Strobes Required
- Wide Temperature Range..... -55°C to +125°C
- Equal Cycle and Access Time
- Single 5 Volt Supply
- Gated Inputs - No Pull-up or Pull-down Resistors Required

Description

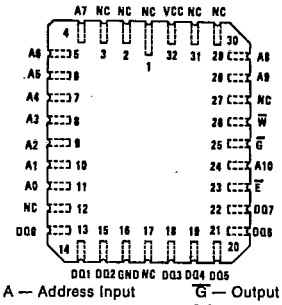
The HM-65162 is a CMOS 2048 x 8 bit Static Random Access Memory manufactured using the Harris advanced SAJI VI process. The device utilizes asynchronous circuit design for fast cycle times and ease of use. The pinout is the JEDEC 24 pin, 8-bit wide standard which allows easy memory board layouts with the flexibility to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162 is ideally suited for use in microprocessor based systems with its 8-bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Pinouts

DIP
TOP VIEW

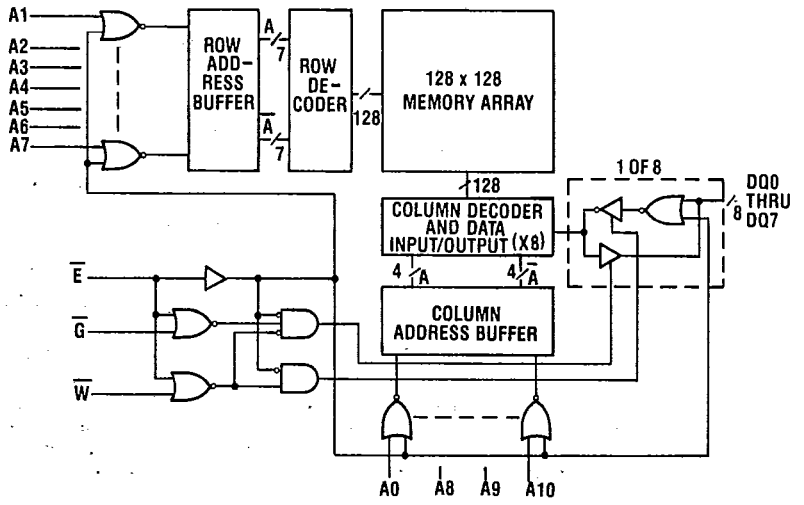


LCC
TOP VIEW



A — Address Input
DQ — Data Input/Output
$\overline{E}$ — Chip Enable
$\overline{G}$ — Output Enable
$\overline{W}$ — Write Enable
NC — No Connect

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage (VCC - GND) ..... -0.3V to +7.0 Volts
Input or Output Voltage Applied ..... (GND -0.3V) to (VCC +0.3V)
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 7°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 47°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65162S-9 ..... -40°C to +85°C

D.C. Electrical Specifications ADVANCE INFORMATION

VCC = 5V ± 10%; T_A = HM-65162S-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current	—	100	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current	—	8	mA	$\overline{E}$ = 2.2V, IO = 0
ICCEN	Enabled Supply Current	—	70	mA	$\overline{E}$ = 0.8V, IO = 0
ICCOP	Operating Supply Current (Note 3)	—	70	mA	$\overline{E}$ = 0.8V, IO = 0, f = 1MHz
ICCDR	Data Retention Supply Current	—	40	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC -0.3V
VCCDR	Data Retention Supply Voltage	2.0	—	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC +0.3V	V	
VOL	Output Low Voltage	—	0.4	V	IO = 4.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC = GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC = GND, f = 1MHz

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

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A.C. Electrical Specifications ADVANCE INFORMATION VCC = 5V ± 10%; T_A = HM-65162S-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	Read Cycle Time	55	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	55	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	55	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2,4)
(5) TGLQV	Output Enable Access Time	—	35	ns	(Notes 1, 4)
(6) TGLQX	Output Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Enable Output Disable Time	—	35	ns	(Notes 2, 4)
(8) TGHQZ	Output Enable Output Disable Time	—	30	ns	(Notes 2, 4)
(9) TAVQX	Output Hold From Address Change	5	—	ns	(Notes 1, 4)
WRITE CYCLE					
(10) TAVAX	Write Cycle Time	55	—	ns	(Notes 1, 4)
(11) TELWH	Chip Selection to End of Write	45	—	ns	(Notes 1, 4)
(12) TAVWL	Address Setup Time	5	—	ns	(Notes 1, 4)
(13) TWLWH	Write Enable Pulse Width	40	—	ns	(Notes 1, 4)
(14) TWHAX	Write Enable Read Setup Time	10	—	ns	(Notes 1, 4)
(15) TGHQZ	Output Enable Output Disable Time	—	30	ns	(Notes 2, 4)
(16) TWLQZ	Write Enable Output Disable Time	—	30	ns	(Notes 2, 4)
(17) TDVWH	Data Setup Time	25	—	ns	(Notes 1, 4)
(18) TWHDX	Data Hold Time	10	—	ns	(Notes 1, 4)
(19) TWHQX	Write Enable Output Enable Time	0	—	ns	(Notes 1, 4)
(20) TWLEH	Write Enable Pulse Setup Time	45	—	ns	(Notes 1, 4)
(21) TDVEH	Chip Enable Data Setup Time	25	—	ns	(Notes 1, 4)
(22) TAVWH	Address Valid to End of Write	45	—	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... -0.3 to +7.0 Volts
Input or Output Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 7°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 47°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65162B-8 ..... -55°C to +125°C
HM-65162B-9 ..... -40°C to +85°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65162B-8 -55°C to +125°C
HM-65162B-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current	—	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current	—	8	mA	$\overline{E}$ = 2.2V, IO = 0
ICCEN	Enabled Supply Current	—	70	mA	$\overline{E}$ = 0.8V, IO = 0
ICCOP	Operating Supply Current (Note 3)	—	70	mA	$\overline{E}$ = 0.8V, IO = 0, f = 1MHz
ICCDR	Data Retention Supply Current	—	20	µA	IO = 0, VCC = 2.0, $\overline{E}$ = VCC -0.3V
VCCDR	Data Retention Supply Voltage	2.0	—	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
IIOZ	Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC+0.3	V	
VOL	Output Low Voltage	—	0.4	V	IO = 4.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CIO	Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

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A.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65162B-8 -55°C to +125°C
HM-65162B-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	Read Cycle Time	70	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	70	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	70	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(5) TGLQV	Output Enable Access Time	—	50	ns	(Notes 1, 4)
(6) TGLQX	Output Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Enable Output Disable Time	—	35	ns	(Notes 2, 4)
(8) TGHQZ	Output Enable Output Disable Time	—	35	ns	(Notes 2, 4)
(9) TAVQX	Output Hold from Address Change	5	—	ns	(Notes 1, 4)
WRITE CYCLE					
(10) TAVAX	Write Cycle Time	70	—	ns	(Notes 1, 4)
(11) TELWH	Chip Selection to End of Write	45	—	ns	(Notes 1, 4)
(12) TAVWL	Address Setup Time	10	—	ns	(Notes 1, 4)
(13) TWLWH	Write Enable Pulse Width	40	—	ns	(Notes 1, 4)
(14) TWHAX	Write Enable Read Setup Time	10	—	ns	(Notes 1, 4)
(15) TGHQZ	Output Enable Output Disable Time	—	35	ns	(Notes 2, 4)
(16) TWLQZ	Write Enable Output Disable Time	—	40	ns	(Notes 2, 4)
(17) TDVWH	Data Setup Time	30	—	ns	(Notes 1, 4)
(18) TWHDX	Data Hold Time	10	—	ns	(Notes 1, 4)
(19) TWHQX	Write Enable Output Enable Time	0	—	ns	(Notes 2, 4)
(20) TWLEH	Write Enable Pulse Setup Time	40	—	ns	(Notes 1, 4)
(21) TDVEH	Chip Enable Data Setup Time	30	—	ns	(Notes 1, 4)
(22) TAVWH	Address Valid to End of Write	50	—	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage (VCC - GND) ..... -0.3V to +7.0 Volts
Input or Output Voltage Applied ..... (GND -0.3V) to (VCC +0.3V)
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 7°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 47°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65162-8 ..... -55°C to +125°C
HM-65162-9 ..... -40°C to +85°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65162-8 -55°C to +125°C
HM-65162-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current	—	100	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current	—	8	mA	$\overline{E}$ = 2.2V, IO = 0
ICCEN	Enabled Supply Current	—	70	mA	$\overline{E}$ = 0.8V, IO = 0
ICCOP	Operating Supply Current (Note 3)	—	70	mA	$\overline{E}$ = 0.8V, IO = 0, f = 1MHz
ICCDR	Data Retention Supply Current	—	40	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC -0.3V
VCCDR	Data Retention Supply Voltage	2.0	—	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC +0.3V	V	
VOL	Output Low Voltage	—	0.4	V	IO = 4.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC = GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC = GND, f = 1MHz

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65162-8 -55°C to +125°C
HM-65162-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	Read Cycle Time	90	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	90	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	90	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(5) TGLQV	Output Enable Access Time	—	65	ns	(Notes 1, 4)
(6) TGLQX	Output Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Enable Output Disable Time	—	50	ns	(Notes 2, 4)
(8) TGHQZ	Output Enable Output Disable Time	—	40	ns	(Notes 2, 4)
(9) TAVQX	Output Hold From Address Change	5	—	ns	(Notes 1, 4)
WRITE CYCLE					
(10) TAVAX	Write Cycle Time	90	—	ns	(Notes 1, 4)
(11) TELWH	Chip Selection to End of Write	55	—	ns	(Notes 1, 4)
(12) TAVWL	Address Setup Time	10	—	ns	(Notes 1, 4)
(13) TWLWH	Write Enable Pulse Width	55	—	ns	(Notes 1, 4)
(14) TWHAX	Write Enable Read Setup Time	10	—	ns	(Notes 1, 4)
(15) TGHQZ	Output Enable Output Disable Time	—	40	ns	(Notes 2, 4)
(16) TWLQZ	Write Enable Output Disable Time	—	50	ns	(Notes 2, 4)
(17) TDVWH	Data Setup Time	30	—	ns	(Notes 1, 4)
(18) TWHDX	Data Hold Time	15	—	ns	(Notes 1, 4)
(19) TWHQX	Write Enable Output Enable Time	0	—	ns	(Notes 2, 4)
(20) TWLEH	Write Enable Pulse Setup Time	55	—	ns	(Notes 1, 4)
(21) TDVEH	Chip Enable Data Setup Time	30	—	ns	(Notes 1, 4)
(22) TAVWH	Address Valid to End of Write	65	—	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage (VCC - GND) ..... -0.3V to +7.0 Volts
Input or Output Voltage Applied ..... (GND -0.3V) to (VCC +0.3V)
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 7°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 47°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65162C-8 ..... -55°C to +125°C
HM-65162C-9 ..... -40°C to +85°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65162C-8 -55°C to +125°C
HM-65162C-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current	—	900	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current	—	8	mA	$\overline{E}$ = 2.2V, IO = 0
ICCEN	Enabled Supply Current	—	70	mA	$\overline{E}$ = 0.8V, IO = 0
ICCOP	Operating Supply Current (Note 3)	—	70	mA	$\overline{E}$ = 0.8V, IO = 0, f = 1MHz
ICCDR	Data Retention Supply Current	—	300	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC -0.3V
VCCDR	Data Retention Supply Voltage	2.0	—	V	
II	Input Leakage Current	-5.0	+5.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-5.0	+5.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC +0.3V	V	
VOL	Output Low Voltage	—	0.4	V	IO = 4.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC = GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC = GND, f = 1MHz

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

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A.C. Electrical Specifications

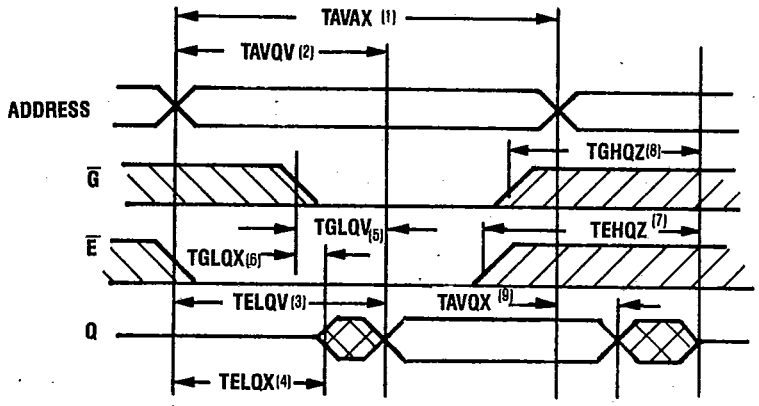
VCC = 5V ± 10%; T_A = HM-65162C-8 -55°C to +125°C
HM-65162C-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	Read Cycle Time	90	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	90	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	90	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(5) TGLQV	Output Enable Access Time	—	65	ns	(Notes 1, 4)
(6) TGLQX	Output Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Enable Output Disable Time	—	50	ns	(Notes 2, 4)
(8) TGHQZ	Output Enable Output Disable Time	—	40	ns	(Notes 2, 4)
(9) TAVQX	Output Hold From Address Change	5	—	ns	(Notes 1, 4)
WRITE CYCLE					
(10) TAVAX	Write Cycle Time	90	—	ns	(Notes 1, 4)
(11) TELWH	Chip Selection to End of Write	55	—	ns	(Notes 1, 4)
(12) TAVWL	Address Setup Time	10	—	ns	(Notes 1, 4)
(13) TWLWH	Write Enable Pulse Width	55	—	ns	(Notes 1, 4)
(14) TWHAX	Write Enable Read Setup Time	10	—	ns	(Notes 1, 4)
(15) TGHQZ	Output Enable Output Disable Time	—	40	ns	(Notes 2, 4)
(16) TWLQZ	Write Enable Output Disable Time	—	50	ns	(Notes 2, 4)
(17) TDVWH	Data Setup Time	30	—	ns	(Notes 1, 4)
(18) TWHDX	Data Hold Time	15	—	ns	(Notes 1, 4)
(19) TWHQX	Write Enable Output Enable Time	0	—	ns	(Notes 2, 4)
(20) TWLEH	Write Enable Pulse Setup Time	55	—	ns	(Notes 1, 4)
(21) TDVEH	Chip Enable Data Setup Time	30	—	ns	(Notes 1, 4)
(22) TAVWH	Address Valid to End of Write	65	—	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Read Cycle

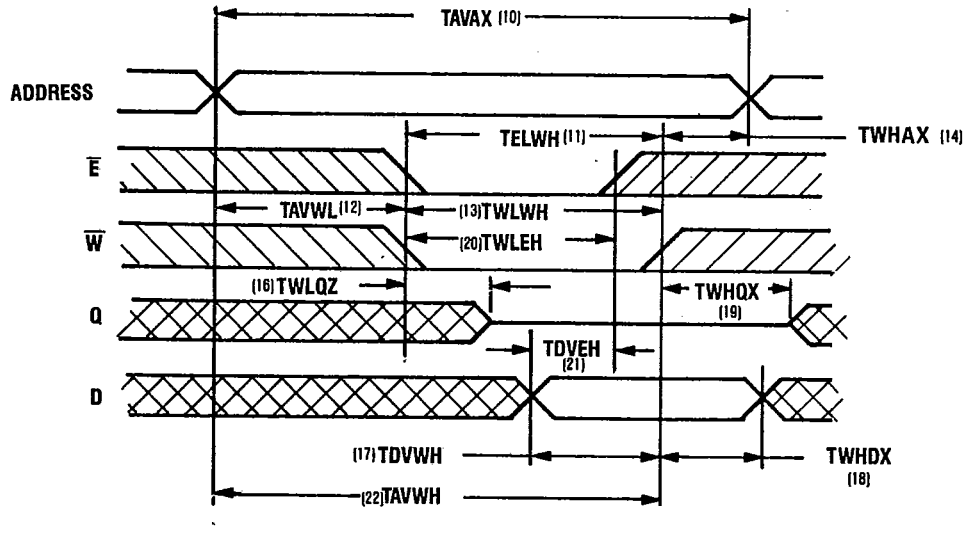


NOTE: $\overline{W}$ IS HIGH FOR A READ CYCLE

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be ≤ VIL and $\overline{W}$ ≥ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

Write Cycles

WRITE CYCLE I



NOTE: $\overline{G}$ IS LOW THROUGHOUT WRITE CYCLE

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of $\overline{W}$. (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied. (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

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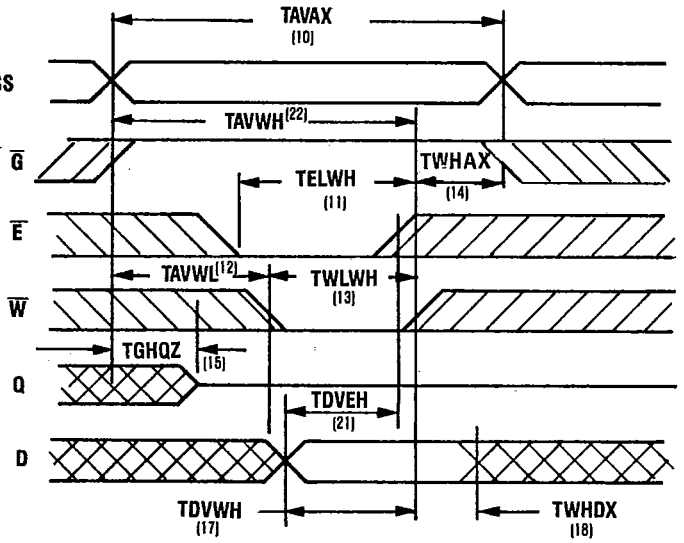
WRITE CYCLE II



In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.