Integrated Device Technology Inc

CMOS STATIC RAM PLASTIC SIP MODULE (16K x 5-BIT)

IDT7MP564

FEATURES:

- 81,920-bit CMOS static RAM module with decoupling capacitor
- High speed: 20ns max.
- Low power consumption: 1.1W typ.
- IDT7MP564 package options reduce overall height
- Utilizes IDT6167s—high-performance 16K RAMs produced with advanced CEMOS™
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (± 10%) power supply
- Inputs and outputs directly TTL-compatible

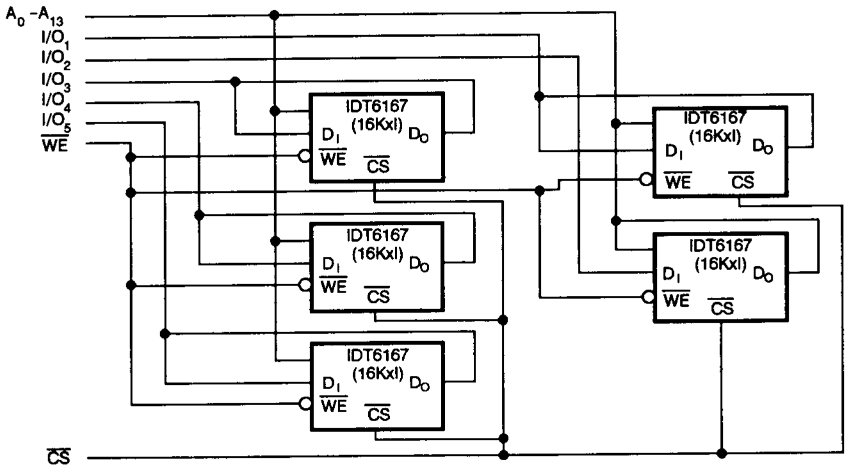
DESCRIPTION:

The IDT7MP564 is an 80K (16,384 x 5-bit) high-speed CMOS static RAM constructed on an epoxy laminate substrate using 5 IDT6167 (16,384 x 1-bit) CMOS static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to use of the IDT6167 RAMs, fabricated in IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

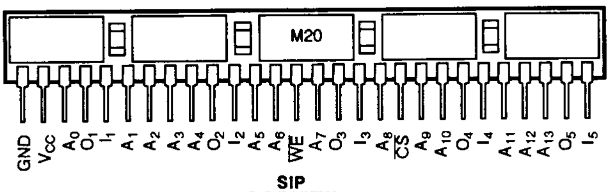
The IDT7MP564 is available with access times as fast as 20ns, with maximum power consumption of only 2.2 watts. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit automatically goes to, and remains in, a standby mode as long as $\overline{CS}$ remains high, consuming only 963mW maximum. Substantially lower power levels can be achieved in the I_{SB1} mode (less than 138mW max.).

All inputs and outputs of the IDT7MP564 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SIP
SIDE VIEW

PIN NAMES

$A_0 - A_{13}$	Addresses	$\overline{WE}$	Write Enable
$I/O_1 - I/O_5$	Data Inputs/Outputs	V_{CC}	Power
$\overline{CS}$	Chip Select	GND	Ground

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TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = -1.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MP564 MIN.	TYP.[1]	MAX.	UNIT
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	–	15	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	–	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	–	200	400	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f_{MAX}	–	200	400	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	–	80	175	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $\leq$ 0.2V	–	5	25	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	–	V

NOTES:

1. V_{CC} = 5V, T_A = +25°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A=+25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	22	pF

NOTE:

1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

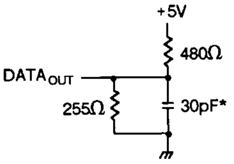


Figure 1. Output Load

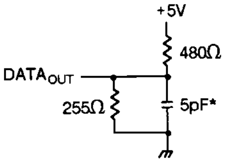


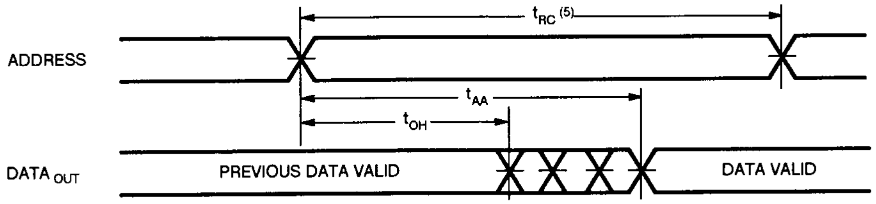
Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig

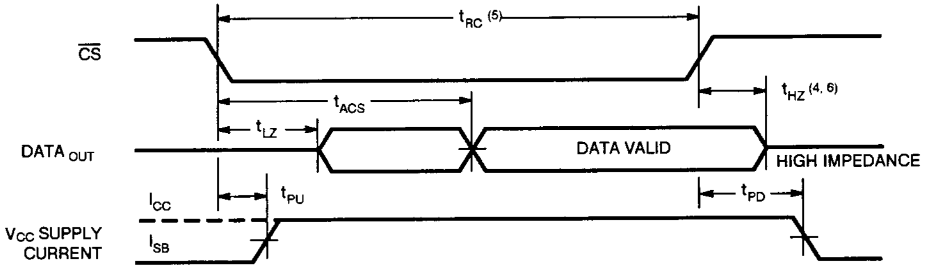
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MP564L20 MIN.	IDT7MP564L20 MAX.	IDT7MP564L25 MIN.	IDT7MP564L25 MAX.	IDT7MP564L35 MIN.	IDT7MP564L35 MAX.	IDT7MP564L45 MIN.	IDT7MP564L45 MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	35	–	45	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Select to Output in Low Z	3	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z	–	10	–	10	–	15	–	20	ns
t_{PU}	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time	–	20	–	25	–	35	–	45	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	20	–	25	–	35	–	45	–	ns
t_{CW}	Chip Select to End of Write	15	–	20	–	30	–	40	–	ns
t_{AW}	Address Valid to End of Write	15	–	20	–	30	–	40	–	ns
t_{AS}	Address Set-up Time	2	–	3	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	13	–	17	–	25	–	35	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	3	–	ns
t_{DW}	Data Valid to End of Write	13	–	15	–	20	–	25	–	ns
t_{DH}	Data Hold Time	2	–	3	–	3	–	3	–	ns
t_{WZ}	Write Enable to Output in High Z	–	7	–	10	–	15	–	20	ns
t_{OW}	Output Active from End of Write	0	–	0	–	0	–	0	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



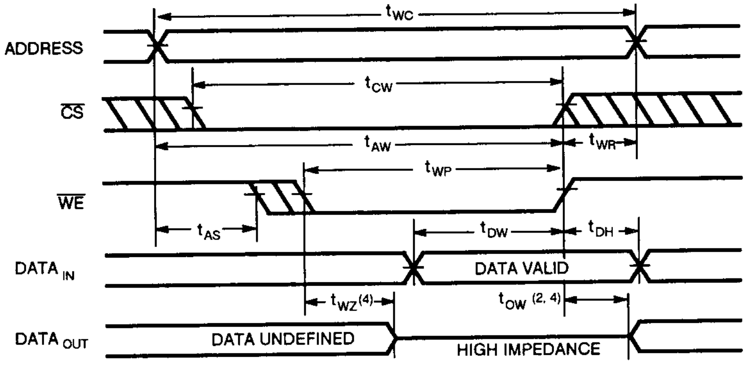
TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



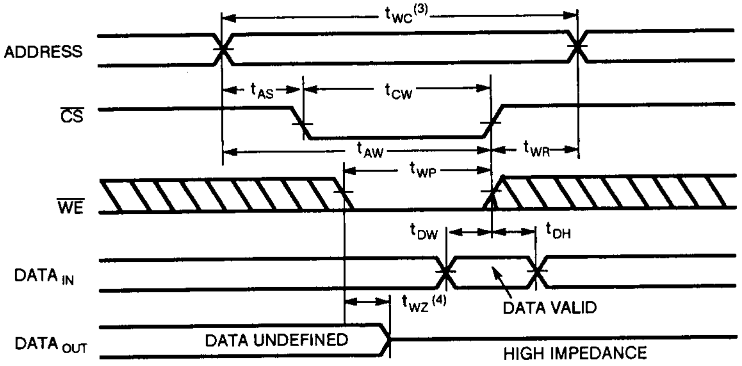
NOTES:

1. $\overline{WE}$ is high for read cycle.
2. $\overline{CS}$ is low for read cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed, operating voltage and temperature, t_{HZ} will be less than or equal to t_{LZ}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



NOTES:

1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. IF $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

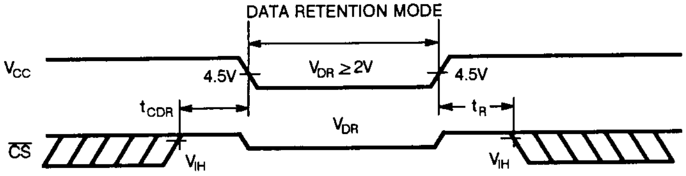
LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $\leq$ 0.2V	– –	10(2) 15(3)	300(2) 400(3)	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	–	–	ns
t_R	Operation Recovery Time		t_{RC}(4)	–	–	ns

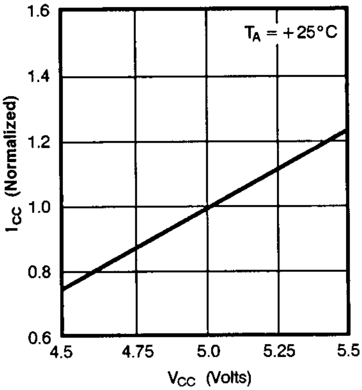
NOTES:

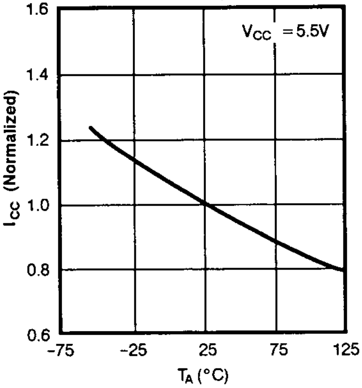
1. T_A = +25°C
2. @ V_{CC} = 2V
3. @ V_{CC} = 3V
4. t_{RC} = Read Cycle Time

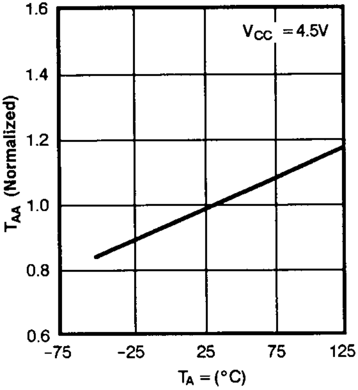
LOW V_{CC} DATA RETENTION WAVEFORMS

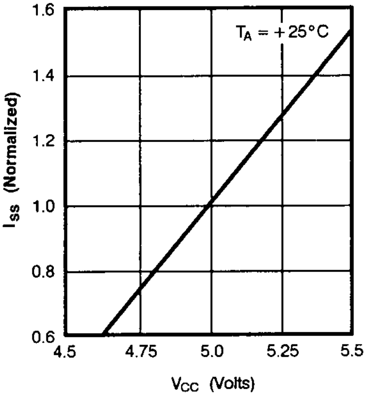


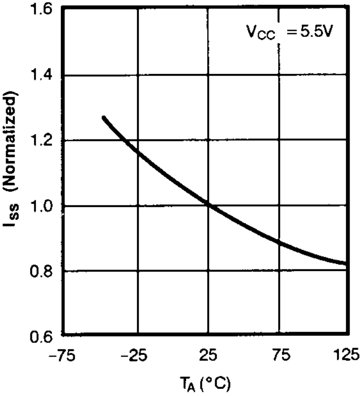
NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

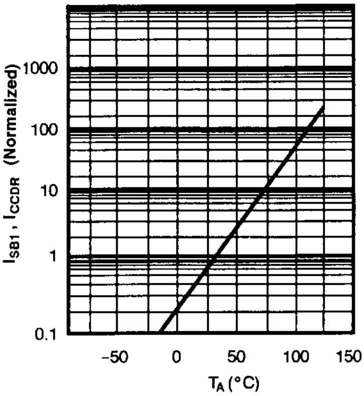

Supply Current vs. Voltage

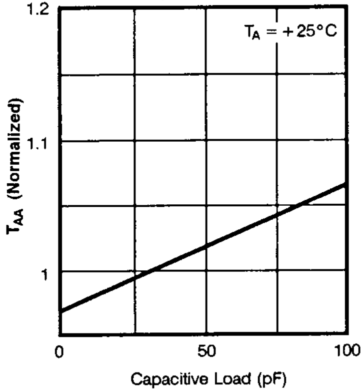

Supply Current vs. Ambient Temperature


Address Access Time vs. Ambient Temperature


Standby Power Supply Current vs. Voltage


Standby Power Supply Current vs. Ambient Temperature


Full Standby Power Supply Current Data Retention Current vs. Ambient Temperature


Address Access Time vs. Capacitive Load

ORDERING INFORMATION