ML4832

Electronic Dimming Ballast Controller

GENERAL DESCRIPTION

The ML4832 is a complete solution for a dimmable/non-dimmable, high power factor, high efficiency electronic ballast. The BiCMOS ML4832 contains controllers for "boost" type power factor correction as well as for a dimming ballast.

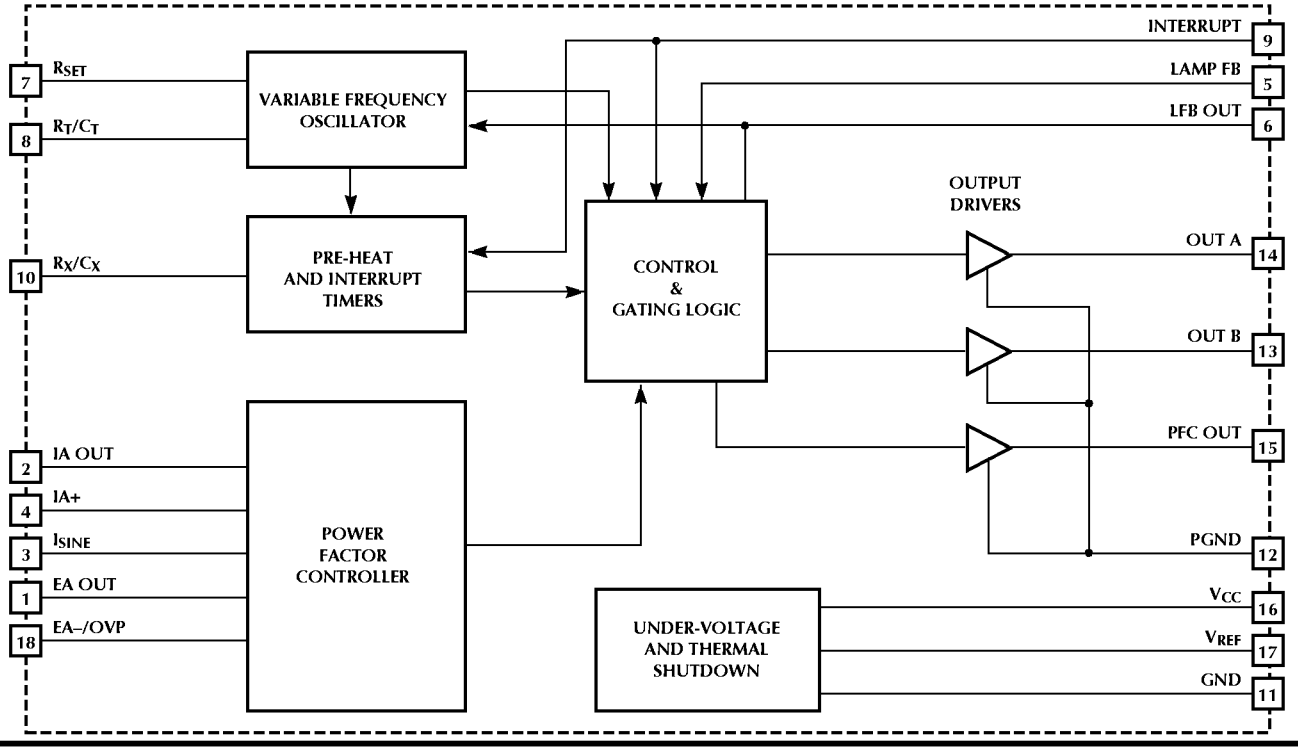
The power factor circuit uses the average current sensing method with a gain modulator and overvoltage protection. This system produces a power factor of better than 0.99 with low input current THD at > 95% efficiency. Special care has been taken in the design of the ML4832 to increase system noise immunity by using a high amplitude oscillator, and a current-fed multiplier. An overvoltage protection comparator inhibits the PFC section in the event of a lamp out or lamp failure condition.

The ballast section provides for programmable starting scenarios with programmable preheat and lamp out-of-socket interrupt times. The IC controls lamp output through frequency modulation using lamp current feedback.

FEATURES

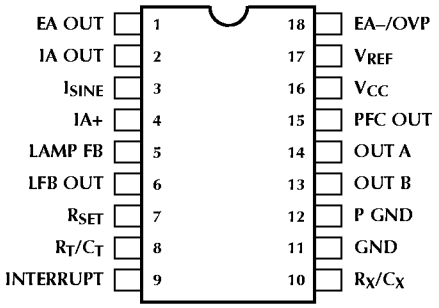
- Complete power factor correction and dimming ballast control in one IC
- Low distortion, high efficiency continuous boost, average current sensing PFC section
- Programmable start scenario for rapid or instant start lamps
- Lamp current feedback for dimming control
- Variable frequency dimming and starting
- Programmable restart for lamp out condition to reduce ballast heating
- Over-temperature shutdown replaces external heat sensor for safety
- PFC overvoltage comparator eliminates output "runaway" due to load removal
- Large oscillator amplitude and gain modulator improves noise immunity
- Low start-up current < 0.5mA

BLOCK DIAGRAM



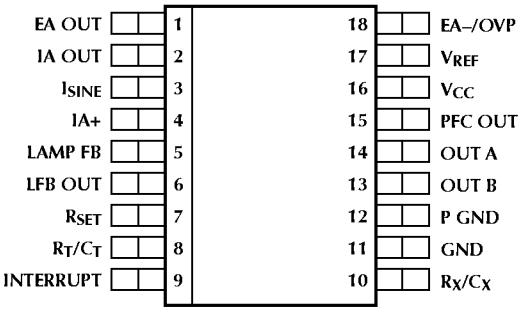
PIN CONFIGURATION

ML4832
18-Pin DIP (P18)



TOP VIEW

ML4832
18-Pin SOIC (S18)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	EA OUT	PFC error amplifier output and compensation node
2	IA OUT	Output and compensation node of the PFC average current transconductance amplifier
3	I_{SINE}	PFC gain modulator input
4	IA+	Non-inverting input of the PFC average current transconductance amplifier and peak current sense point of the PFC cycle by cycle current limit comparator
5	LAMP FB	Inverting input of an error amplifier used to sense (and regulate) lamp arc current. Also the input node for dimming control.
6	LFB OUT	Output from the lamp current error transconductance amplifier used for lamp current loop compensation
7	R_{SET}	External resistor which sets oscillator F_{MAX}, and R_X/C_X charging current
8	R_T/C_T	Oscillator timing components
9	INTERRUPT	Input used for lamp-out detection and restart. A voltage greater than 7.5 volts resets the chip and causes a restart after a programmable interval.
10	R_X/C_X	Sets the timing for the preheat, dimming lockout, and interrupt
11	GND	Ground
12	P GND	Power ground for the IC
13	OUT B	Ballast MOSFET drive output
14	OUT A	Ballast MOSFET drive output
15	PFC OUT	Power Factor MOSFET drive output
16	V_{CC}	Positive supply for the IC
17	V_{REF}	Buffered output for the 7.5V voltage reference
18	EA–/OVP	Inverting input to PFC error amplifier and OVP comparator input

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 60mA
Output Current, Source or Sink (OUTA, OUTB, PFC OUT)
DC 250mA
Output Energy (capacitive load per cycle) 1.5mJ
Gain Modulator I_{SINE} Input 10mA
Analog Inputs ..... −0.3V to V_{CC} −2V
IA+ Input Voltage ..... −3V to 2V
Maximum Forced Voltage
(EA OUT, LFB OUT) ..... −0.3V to 7.7V
Maximum Forced Current
(EA OUT, IA OUT, LFB OUT) ..... ±20mA
Maximum Forced Voltage
(IA OUT) ..... −0.3V to 7.5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 260°C
Thermal Resistance (θ_{JA})
Plastic PDIP ..... 70°C/W
Plastic SOIC ..... 100°C/W

OPERATING CONDITIONS

Temperature Range
ML4832C ..... 0°C to 85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_{SET} = 22.1kΩ, R_T = 15.8kΩ, C_T = 1.5nF, C (V_{CC}) = 1µF, I_{SINE} = 200µA, V_{CC} = 12.5V, T_A = Operating Temperature Range (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PFC CURRENT SENSE AMPLIFIER					
Small Signal Transconductance		40	90	120	µ℧
Output Low	I_{SINE} = 0mA, $V_{EA\ OUT}$ = 0V, V_{IA+} = −0.3V, R_L = ∞		0.2	0.4	V
Output High	I_{SINE} = 1.5mA, $V_{EA-/OVP}$ = V_{IA+} = 0V, R_L = ∞	6.3	6.8		V
Source Current	I_{SINE} = 1.5mA, $V_{EA-/OVP}$ = V_{IA+} = 0V, $V_{IA\ OUT}$ = 6V, T_J = 25°C	−0.05	−0.15	−0.25	mA
Sink Current	I_{SINE} = 0mA, $V_{IA\ OUT}$ = 0.3V, V_{IA+} = −0.6V $V_{EA\ OUT}$ = 0V, $V_{EA-/OVP}$ = 5V, T_J = 25°C	0.03	0.07	0.16	mA
PFC VOLTAGE FEEDBACK AMPLIFIER/LAMP CURRENT AMPLIFIER					
Input Bias Current			−0.3	−1.0	µA
Small Signal Transconductance		30	55	90	µ℧
Input Voltage Range		−0.3		5.0	V
Output Low	V_{LAMPFB} = $V_{EA-/OVP}$ = 3V, R_L = ∞		0.2	0.4	V
Output High	V_{LAMPFB} = $V_{EA-/OVP}$ = 2V, R_L = ∞	7.1	7.5	7.8	V
Source Current	V_{LAMPFB} = $V_{EA-/OVP}$ = 0V, $V_{EA\ OUT}$ = $V_{LFB\ OUT}$ = 7V, T_J = 25°C	−0.06	−0.15	−0.30	mA
Sink Current	V_{LAMPFB} = $V_{EA-/OVP}$ = 5V, $V_{EA\ OUT}$ = $V_{LFB\ OUT}$ = 0.3V, T_J = 25°C	0.06	0.12	0.28	mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN MODULATOR					
Output Voltage (V_{MUL})	I_{SINE} = 100µA, $V_{EA OUT}$ = 3V		85		mV
	I_{SINE} = 300µA, $V_{EA OUT}$ = 3V		260		mV
	I_{SINE} =100µA, $V_{EA OUT}$ = 6V		200		mV
	I_{SINE} = 300µA, $V_{EA OUT}$ = 6V		600		mV
Output Voltage Limit	I_{SINE} = 1.5mA, $V_{EA-/OVP}$ = 0V	0.9	1	1.1	V
Offset Voltage	I_{SINE} = 0µA, $V_{EA-/OVP}$ = 0V			15	mV
	I_{SINE} = 150µA, $V_{EA-/OVP}$ = 3V			15	mV
I_{SINE} Input Voltage	I_{SINE} = 200µA	0.8	1.4	1.8	V
PFC CURRENT — LIMIT COMPARATOR					
Current-Limit Threshold		-0.85	-1.0	-1.15	V
Propagation Delay	100mV step and 100mV overdrive		100		ns
OSCILLATOR					
Initial Accuracy	T_A = 25°C	72	76	80	kHz
Voltage Stability	V_{CCZ} - 4.0V < V_{CC} < V_{CCZ} - 0.5V		1		%
Temperature Stability			2		%
Total Variation	Line, temperature	69		83	kHz
Ramp Valley to Peak			2.5		V
C_T Charging Current	V_{LAMPFB} = 3V, $V_{RT/CT}$ = 2.5V, $V_{RX/CX}$ = 0.9V (Preheat)	-90	-113	-130	µA
	V_{LAMPFB} = 3V, $V_{RT/CT}$ = 2.5V, RX/CX = Open	-180	-230	-260	µA
C_T Discharge Current	$V_{RT/CT}$ = 2.5V	4.0	5.5	7.0	mA
Output Drive Deadtime		0.64	0.91	1.30	µs
REFERENCE SECTION					
Output Voltage	T_A = 25°C, I_O = 1mA	7.4	7.5	7.6	V
Line regulation	V_{CCZ} - 4.0V < V_{CC} < V_{CCZ} - 0.5V		8	25	mV
Load regulation	1mA < I_O < 5mA		2	15	mV
Temperature stability			0.4		%
Total Variation	Line, load, temp	7.35		7.65	V
Output Noise Voltage	10Hz to 10kHz		50		µV
Long Term Stability	T_J= 125°C, 1000 hrs		5		mV
PREHEAT AND INTERRUPT TIMER (R_X = 680KΩ, C_X = 4.7µF)					
Initial Preheat Period			0.8		s
Subsequent Preheat Period			0.7		s
Start Period			1.2		s
Interrupt Period			5.7		s
Pin 10 Charging Current		-24	-28	-33	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PREHEAT AND INTERRUPT TIMER (R_X = 680KΩ, C_X = 4.7µF) CONTINUED					
Pin 10 Open Circuit Voltage	V_{CC} < Start-up threshold	0.4	0.7	1.0	V
Pin 10 Maximum Voltage		7.0	7.3	7.7	V
Input Bias Current	$V_{RX/CX}$ = 1.2V			0.1	µA
Preheat Lower Threshold		1.05	1.22	1.36	V
Preheat Upper Threshold		4.4	4.77	5.15	V
Interrupt Recovery Threshold		1.05	1.22	1.36	V
Start Period End Threshold		6.05	6.6	7.35	V
INTERRUPT INPUT					
Interrupt Threshold		7.15	7.4	7.65	V
Input Bias Current				0.1	µA
R_{SET} Voltage		2.4	2.5	2.6	V
OVP COMPARATOR					
OVP Threshold		2.65	2.75	2.85	V
Hysteresis		0.20	0.25	0.27	V
Propagation Delay			1.4		µs
OUTPUTS					
Output Voltage Low	I_{OUT} = 20mA		0.1	0.2	V
	I_{OUT} = 200mA		1.0	2.0	V
Output Voltage High	I_{OUT} = −20mA	V_{CC} − 0.2	V_{CC} − 0.1		V
	I_{OUT} = −200mA	V_{CC} − 2.0	V_{CC} − 1.0		V
Output Voltage Low in UVLO	I_{OUT} = 10mA, V_{CC} 8V			0.2	V
Output Rise/Fall Time	C_L = 1000pF		20		ns
UNDER-VOLTAGE LOCKOUT AND BIAS CIRCUITS					
IC Shunt Voltage (V_{CCZ})	I_{CC} = 15mA	14.2	15.0	15.8	V
Start-up Current	V_{CC} = Start-up threshold −0.2V		0.34	0.48	mA
Operating Current	V_{CC} = 12.5V, V_{EA+} = 0V, $V_{EA-/OVP}$ = V_{LAMPFB} = 2.3V, EA OUT = open R_T = 16.2kΩ, R_{SET} = 22.1kΩ V_{CC} = 12.5V, C_L = 0		5.5	8.0	mA
Start-up Threshold		V_{CC} − 1.2	V_{CCZ} − 1.0	V_{CC} − 0.8	V
Shutdown Threshold		V_{CC} − 5.5	V_{CCZ} − 5.0	V_{CC} − 4.5	V
Shutdown Temperature (T_J)			120		°C
Hysteresis (T_J)			30		°C

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.

FUNCTIONAL DESCRIPTION

OVERVIEW

The ML4832 consists of an average current controlled continuous boost power factor front end section with a flexible ballast control section. Start-up and lamp-out retry timing are controlled by the selection of external timing components, allowing for control of a wide variety of different lamp types. The ballast section controls the lamp power using frequency modulation (FM) with additional programmability provided to adjust the VCO frequency range. This allows for the IC to be used with a variety of different output networks.

POWER FACTOR SECTION

The ML4832 power factor section is an average current sensing boost mode PFC control circuit which is architecturally similar to that found in the ML4821. For detailed information on this control architecture, please refer to Application Note 16 and the ML4821 data sheet.

GAIN MODULATOR

The ML4832 gain modulator provides high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a series resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

The output of the gain modulator appears on the positive terminal of the IA amplifier to form the reference for the current error amplifier. Please refer to Figure 1.

$$V_{MUL} = \frac{[I_{SINE} \times (VEA - 0.7V)]}{3.4mA} \quad (1)$$

where: I_{SINE} is the current in the dropping resistor,
VEA is the output of the error amplifier (Pin 1).

The output of the gain modulator is limited to 1.0V.

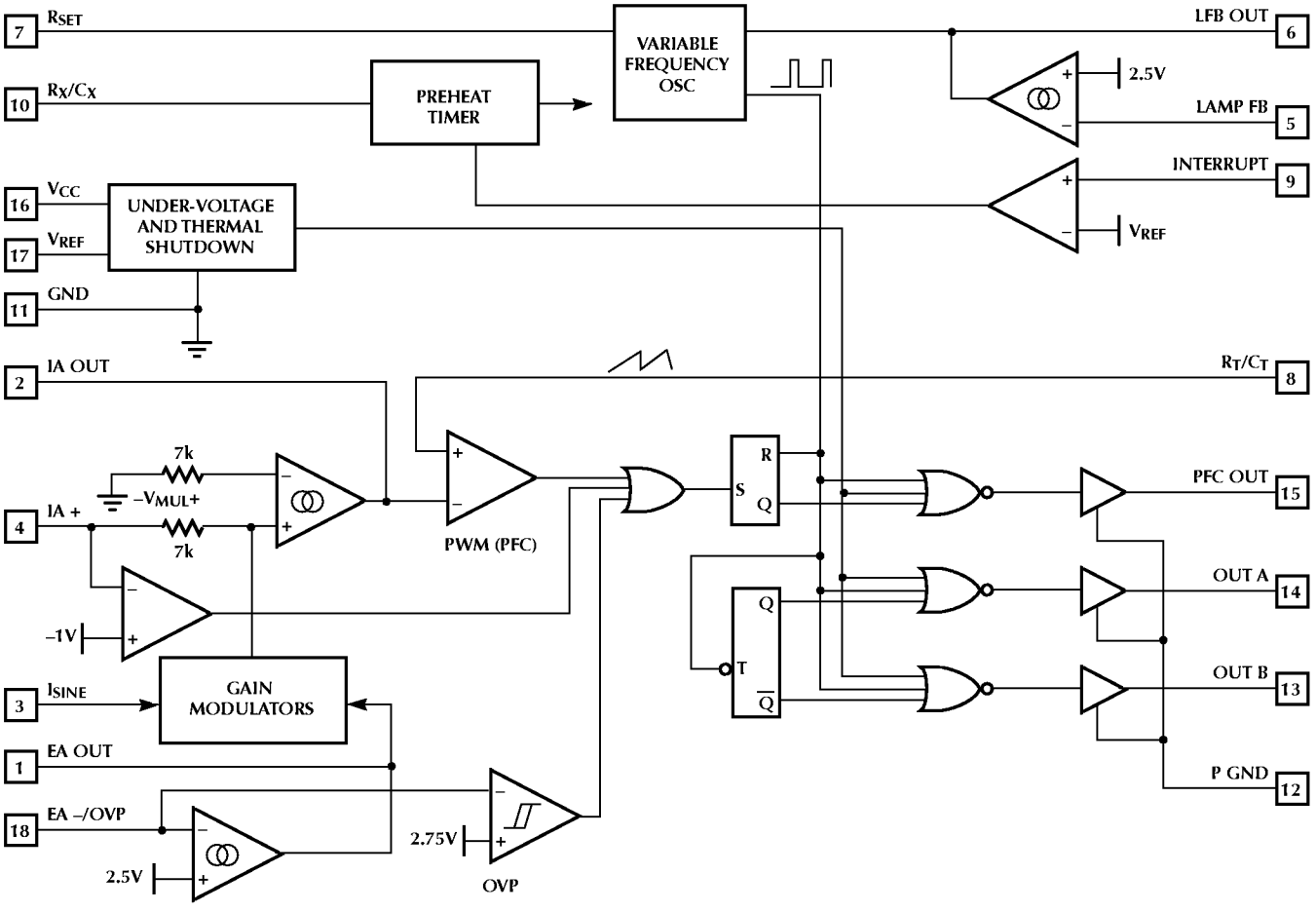


Figure 1. ML4832 Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

AVERAGE CURRENT AND OUTPUT VOLTAGE REGULATION

The PWM regulator in the PFC control section will act to offset the positive voltage caused by the multiplier output by producing an offsetting negative voltage on the current sense resistor at IA+. A cycle-by-cycle current limit is included to protect the MOSFET from high speed current transients. When the voltage at IA+ goes negative by more than 1V, the PWM cycle is terminated.

For more information on compensating the average current and boost voltage error amplifier loops, see ML4821 data sheet.

OVERVOLTAGE PROTECTION AND INHIBIT

The OVP pin serves to protect the power circuit from being subjected to excessive voltages if the load should change suddenly (lamp removal). A divider from the high voltage DC bus sets the OVP trip level. When the voltage on EA–/OVP exceeds 2.75V, the PFC transistors are inhibited. The ballast section will continue to operate.

TRANSCONDUCTANCE AMPLIFIERS

The PFC voltage feedback, PFC current sense, and the loop current amplifiers are all implemented as operational transconductance amplifiers. They are designed to have low small signal forward transconductance such that a large value of load resistor (R1) and a low value ceramic capacitor (<1µF) can be used for AC coupling (C1) in the frequency compensation network. The compensation network shown in Figure 2 will introduce a zero and a pole at:

$$f_Z = \frac{1}{2\pi R_1 C_1} \qquad f_P = \frac{1}{2\pi R_1 C_2} \qquad (2)$$

Figure 3 shows the output configuration for the operational transconductance amplifiers.

A DC path to ground or V_{CC} at the output of the transconductance amplifiers will introduce an offset error.

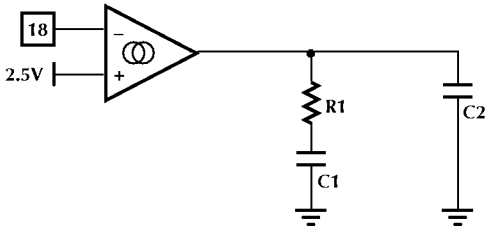


Figure 2. Compensation Network

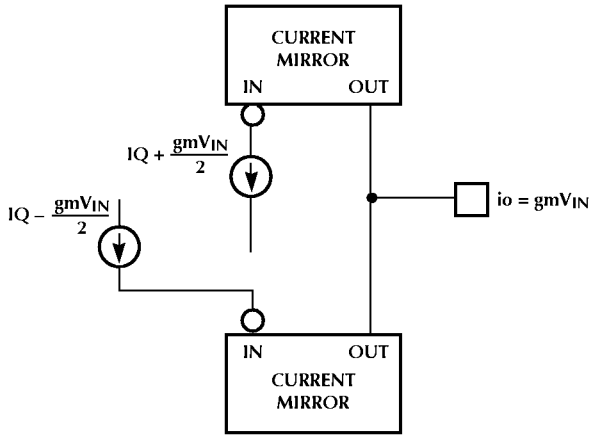


Figure 3. Output Configuration

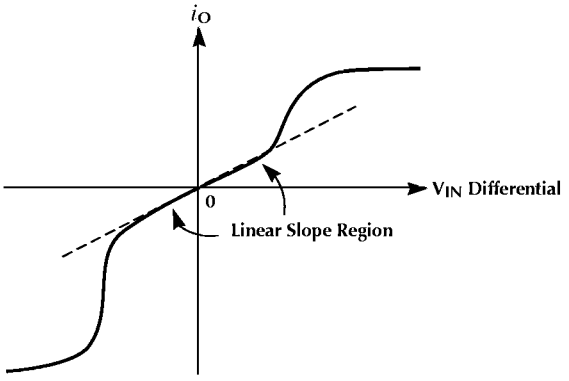


Figure 4. Transconductance Amplifier Characteristics

FUNCTIONAL DESCRIPTION (Continued)

The magnitude of the offset voltage that will appear at the input is given by $V_{OS} = io/gm$. For an io of 1mA and a gm of 0.05 µmhos the input referred offset will be 20mV. Capacitor C1 as shown in Figure 2 is used to block the DC current to minimize the adverse effect of offsets.

Slew rate enhancement is incorporated into all of the operational transconductance amplifiers in the ML4832. This improves the recovery of the circuit in response to power up and transient conditions. The response to large signals will be somewhat non-linear as the transconductance amplifiers change from their low to high transconductance mode. This is illustrated in Figure 4.

BALLAST OUTPUT SECTION

The IC controls output power to the lamps via frequency modulation with non-overlapping conduction. This means that both ballast output drivers will be low during the discharging time t_{DIS} of the oscillator capacitor C_T.

OSCILLATOR

The VCO frequency ranges are controlled by the output of the LFB amplifier. As lamp current decreases, LFB OUT rises in voltage, causing the C_T charging current to decrease, thereby causing the oscillator frequency to decrease. Since the ballast output network attenuates high frequencies, the power to the lamp will be increased.

The oscillator frequency is determined by the following equations:

$$F_{OSC} = \frac{1}{t_{CHG} + t_{DIS}} \quad (3)$$

and

$$t_{CHG} = R_T C_T \ln\left(\frac{V_{REF} + I_{CH} R_T - V_{TL}}{V_{REF} + I_{CH} R_T - V_{TH}}\right) \quad (4)$$

The oscillator's minimum frequency is set when $I_{CH} = 0$ where:

$$F_{OSC} \cong \frac{1}{0.51 \times R_T C_T} \quad (5)$$

This assumes that $t_{CHG} >> t_{DIS}$.

When LFB OUT is high, $I_{CH} = 0$ and the minimum frequency occurs. The charging current varies according to two control inputs to the oscillator:

1. The output of the preheat timer
2. The voltage at LFB OUT

In preheat condition, charging current is fixed at

$$I_{CHG(PREHEAT)} = \frac{2.5}{R_{SET}} \quad (6)$$

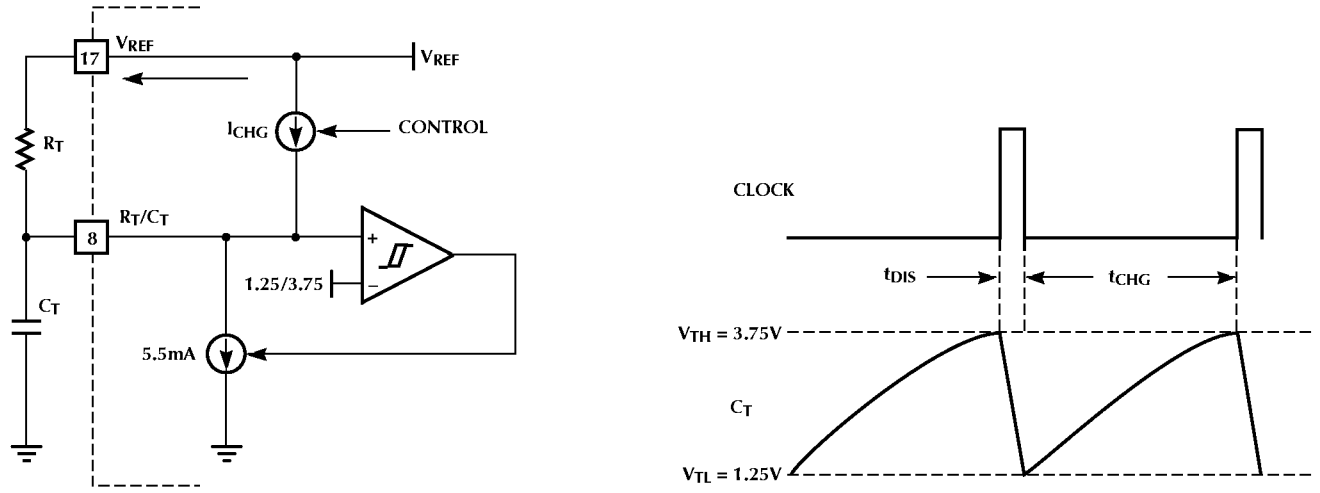


Figure 5. Oscillator Block Diagram and Timing

FUNCTIONAL DESCRIPTION (Continued)

In running mode, charging current decreases as the V_{PIN6} rises from 0V to V_{OH} of the LAMP FB amplifier. The highest frequency will be attained when I_{CHG} is highest, which is attained when LFB OUT is at 0V:

$$I_{CHG(0)} = \frac{5}{R_{SET}} \quad (7)$$

Highest lamp power, and lowest output frequency are attained when LFB OUT is at its maximum output voltage (V_{OH}).

In this condition, the minimum operating frequency of the ballast is set per (5) above.

For the IC to be used effectively in dimming ballasts with higher Q output networks a larger C_T value and lower R_T value can be used, to yield a smaller frequency excursion over the control range ($V_{LFB\ OUT}$). The discharge current is set to 5.5mA. Assuming that $I_{DIS} >> I_{RT}$:

$$t_{DIS(VCO)} \cong 600 \times C_T \quad (8)$$

IC BIAS, UNDER-VOLTAGE LOCKOUT AND THERMAL SHUTDOWN

The IC includes a shunt regulator which will limit the voltage at V_{CC} to 15V (V_{CCZ}). The IC should be fed with a current limited source, typically derived from the ballast transformer auxiliary winding. When V_{CC} is below V_{CCZ} – 1.1V, the IC draws less than 0.48mA of quiescent current and the outputs are off. This allows the IC to start using a "bleed resistor" from the rectified AC line.

To help reduce ballast cost, the ML4832 includes a temperature sensor which will inhibit ballast operation if the IC's junction temperature exceeds 120°C. In order to use this sensor in lieu of an external sensor, care should be taken when placing the IC to ensure that it is sensing temperature at the physically appropriate point in the ballast. The ML4832's die temperature can be estimated with the following equation:

$$T_J \cong T_A \times P_D \times 65°C/W \quad (9)$$

STARTING, RE-START, PREHEAT AND INTERRUPT

The lamp starting scenario implemented in the ML4832 is designed to maximize lamp life and minimize ballast heating during lamp out conditions.

The circuit in Figure 7 controls the lamp starting scenarios: Filament preheat and lamp out interrupt. C_X is charged with a current of $I_{RSET}/4$ and discharged through R_X. The voltage at C_X is initialized to 0.7V (V_{BE}) at power up. The time for C_X to rise to 4.8V is the filament preheat time. During that time, the oscillator charging current (I_{CHG}) is $2.5/R_{SET}$. This will produce a high frequency for filament preheat, but will not produce sufficient voltage to ignite the lamp.

After cathode heating, the inverter frequency drops to F_{MIN} causing a high voltage to appear to ignite the lamp. If the voltage does not drop when the lamp is supposed to have ignited, the lamp voltage feedback coming into pin 9 rises to above V_{REF}, the C_X charging current is shut off and the inverter is inhibited until C_X is discharged by R_X to the 1.2V threshold. Shutting off the inverter in this manner prevents the inverter from generating excessive heat when

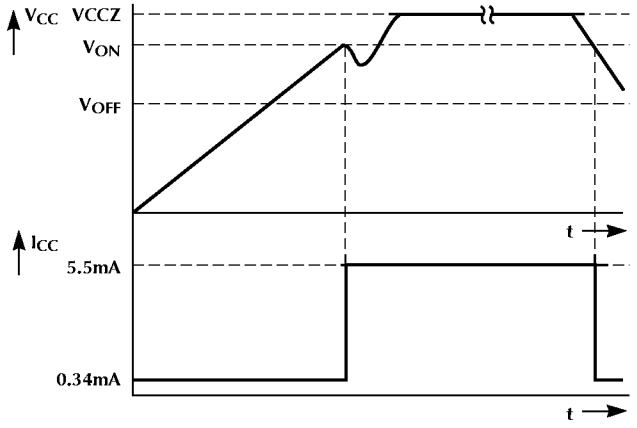


Figure 6. Typical VCC and ICC Waveforms when the ML4832 is Started with a Bleed Resistor from the Rectified AC Line and Bootstrapped from an Auxiliary Winding.

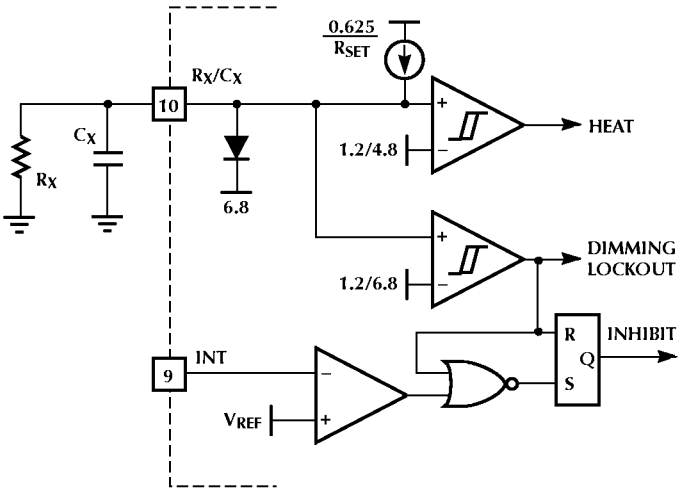


Figure 7. Lamp Preheat and Interrupt Timers

FUNCTIONAL DESCRIPTION (Continued)

the lamp fails to strike or is out of socket. Typically this time is set to be fairly long by choosing a large value of R_X.

LFB OUT is ignored by the oscillator until C_X reaches 6.8V threshold. The lamps are therefore driven to full power and then dimmed. The C_X pin is clamped to about 7.5V.

A summary of the operating frequencies in the various operating modes is shown below.

OPERATING MODE	OPERATING FREQUENCY
Preheat	[F(MAX) to F(MIN)] / 2
Dimming Lock-out	F(MIN)
DIMMING CONTROL	F(MIN) TO F(MAX)

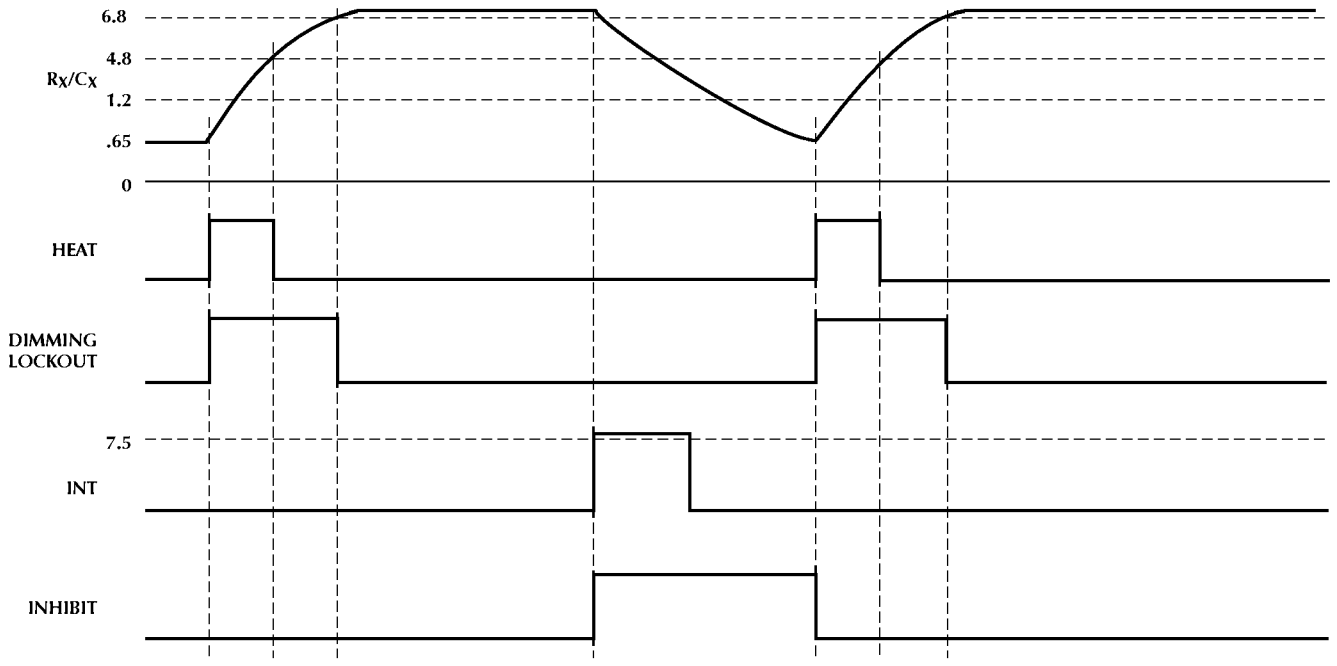


Figure 8. Lamp Starting and Restart Timing

TYPICAL APPLICATIONS

Figures 9 and 10 show ballast schematics, both non-dimming and dimming. These are power-factor corrected 60W ballasts designed to operate two series connected F32T8 fluorescent lamps. Both Schematics, Figures 9 and 10, are of previously published ML4831 circuits that have been modified for ML4832 compatibility. The value changes and component additions made for ML4832 compatibility were for different amplifier compensation, bootstrap/bias and protection and do not effect the validity of the circuit description, operational information or equations.

TO CONVERT FROM AN EXISTING NON-DIMMING ML4831 TO THE ML4832:

Resistors			
Change:	R4	to	51kΩ, 1/4W, 5% carbon film
	R6, R7	to	866kΩ, 1/4W, 1%, metal film
	R7	to	75kΩ, 1/4W, 5%, carbon film
	R18	to	470Ω, 1/4W, 5%, carbon film
	R13	to	5.76kΩ, 1/4W, 1%, metal film
	R14	to	499kΩ, 1/4W, 5%, carbon film
Add:	R24		75kΩ, 1/4W, 5%, carbon film
	R22		51Ω, 1/4W, 5%, carbon film
	R23		100Ω, 1/4W, 5%, carbon film
Delete:	R9		
Capacitors			
Change:	C5	to	10nF, 63V, 10% ceramic
	C7	to	180pF, 100V, 5% ceramic
	C11	to	1nF, 100V, 10% ceramic
	C12	to	100nF, 100V, 10% ceramic
	C18	to	100µF, 16V, 20% electrolytic
	C20	to	100µF, 25V, 20% electrolytic
Add:	C23		33nF, 50V, 20% ceramic
Magnetics			
Change:	T1	to	TSD-882

TO CONVERT FROM AN EXISTING DIMMING ML4831 TO THE ML4832:

Resistors			
Change:	R4	to	51kΩ, 1/4W, 5% carbon film
	R6, R11	to	866kΩ, 1/4W, 1%, metal film
	R7	to	75kΩ, 1/4W, 5%, carbon film
	R18	to	470Ω, 1/4W, 5%, carbon film
	R13	to	5.76kΩ, 1/4W, 1%, metal film
	R14	to	499kΩ, 1/4W, 5%, carbon film
	R26	to	200kΩ, 1/4W, 5%, carbon film
Add:	R32		75kΩ, 1/4W, 5%, carbon film
	R30		51Ω, 1/4W, 5%, carbon film
	R31		100Ω, 1/4W, 5%, carbon film
Delete:	R9		
Capacitors			
Change:	C5	to	10nF, 63V, 10% ceramic
	C7	to	180pF, 100V, 5% ceramic
	C25	to	1nF, 100V, 10% ceramic
	C12	to	100nF, 100V, 10% ceramic
	C24	to	100µF, 16V, 20% electrolytic
	C20	to	100µF, 25V, 20% electrolytic
Add:	C27		33nF, 50V, 20% ceramic
	C26		100nF, 100V, 10% ceramic
Diodes			
Delete:	D10, D13		
Magnetics			
Change:	T1	to	TSD-882

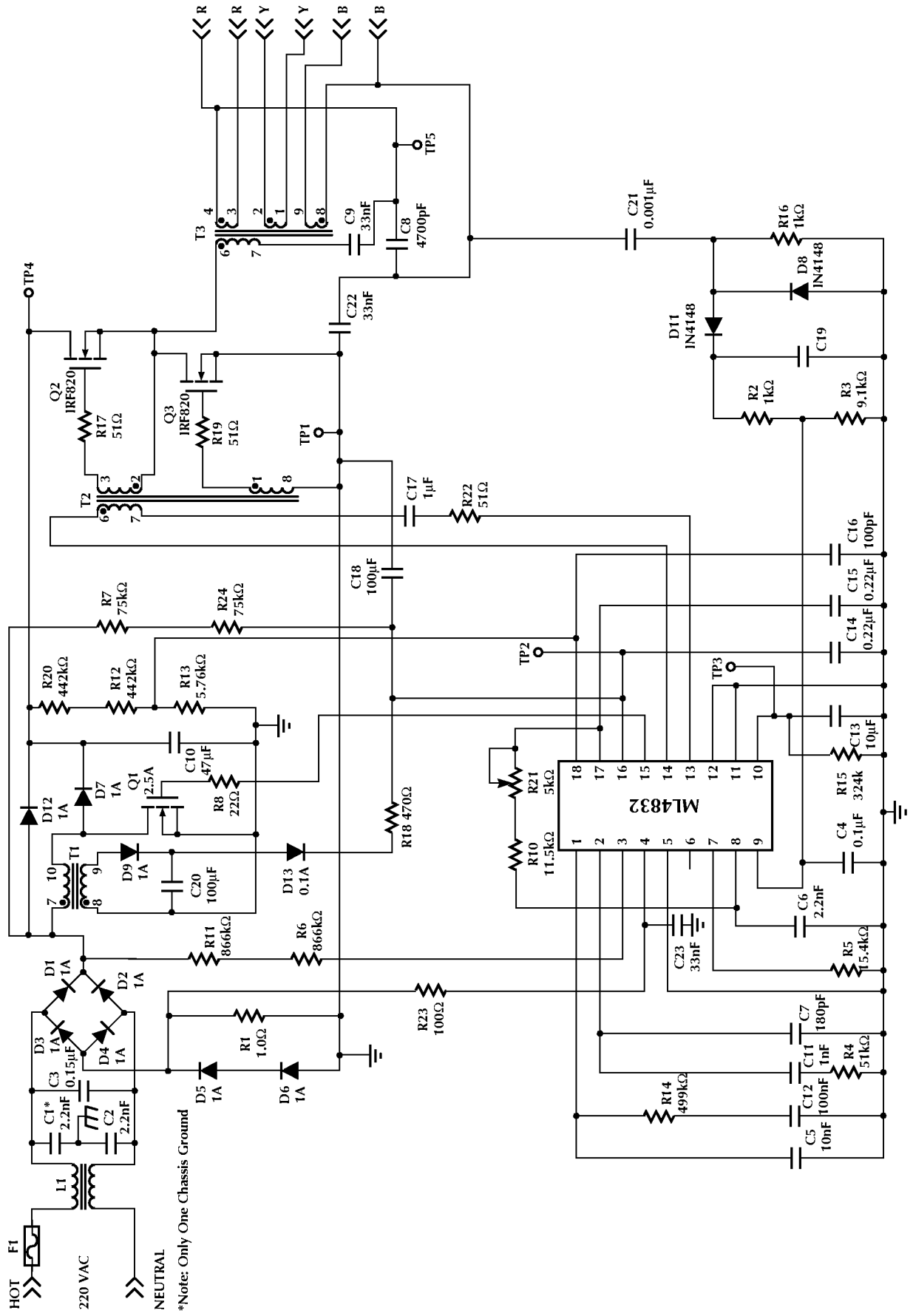


Figure 9. 220V Non-Dimming Ballast

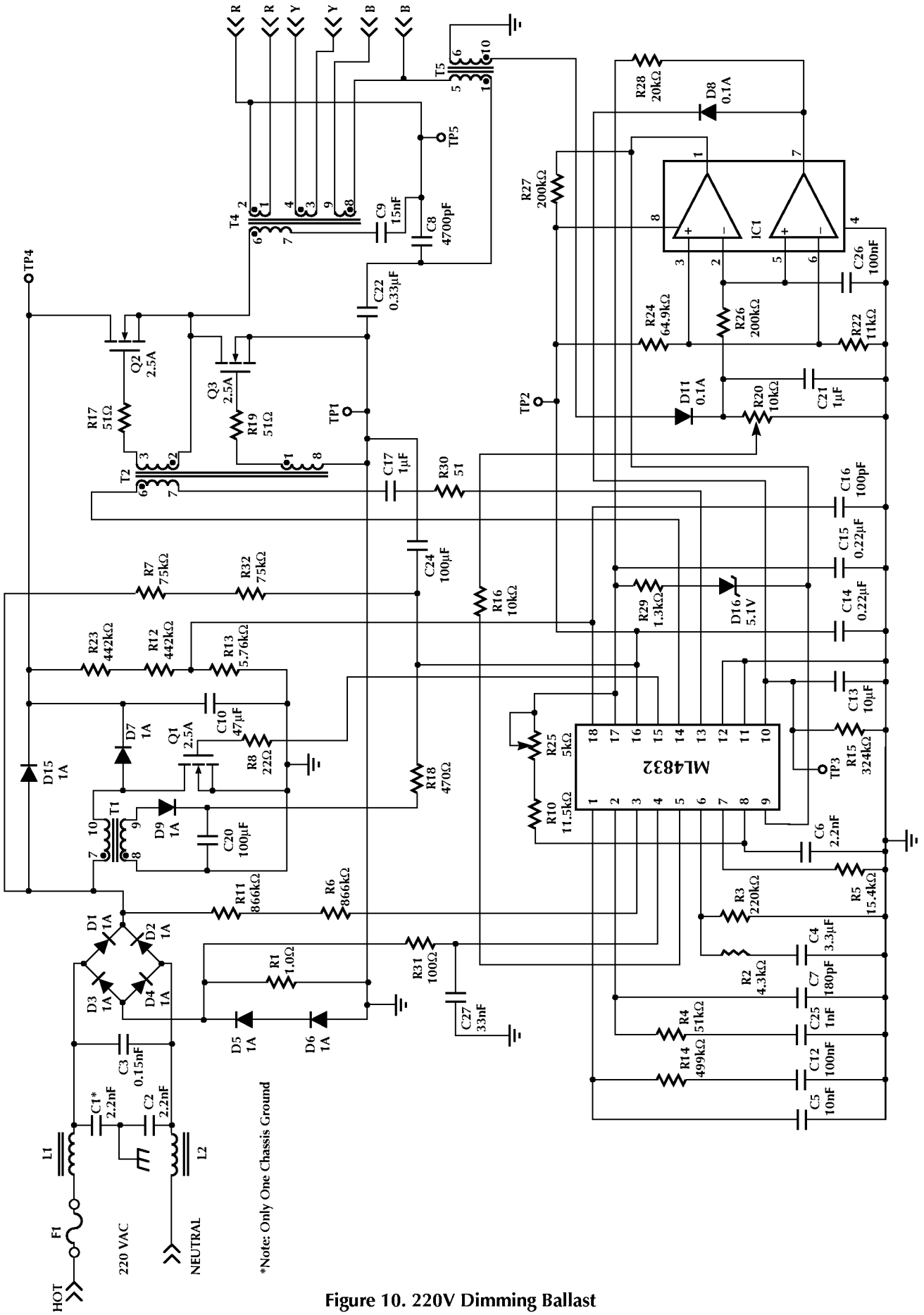
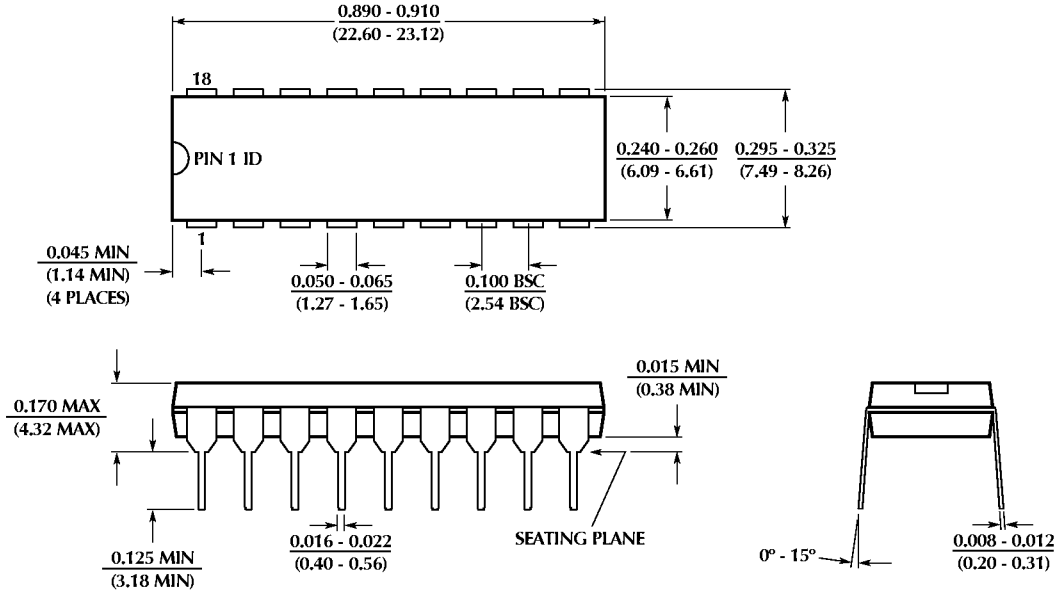


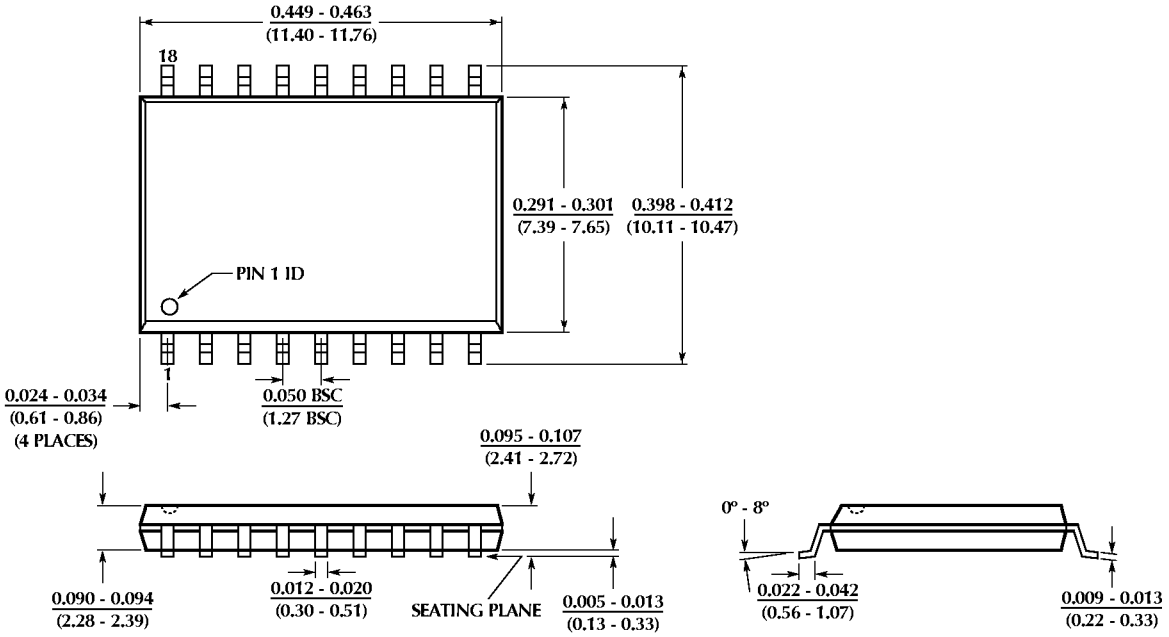
Figure 10. 220V Dimming Ballast

PHYSICAL DIMENSIONS inches (millimeters)

Package: P18
18-Pin PDIP



Package: S18
18-Pin SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4832CP	0°C to 85°C	Molded PDIP (P18)
ML4832CS	0°C to 85°C	SOIC (S18)

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Micro Linear

To receive a price quote or to request a product sample, call or send e-mail to your local representative.

When sending e-mail, be sure to include the Micro Linear part number and whether you want a price quote or a sample in the subject line.

(i.e. subject: Sample request - ML part#xxxx)

Click here to find your local representative