SN54ALS963, SN54ALS964, SN74ALS963, SN74ALS964
DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

D2881, NOVEMBER 1985

- Serial-to-Parallel and Parallel-to-Serial Conversions
- Parallel I/O Registers
- Data Exchangeable Between I/O Register and Shift Register
- Choice of Synchronous and/or Asynchronous Clear
- Independent or Dual Register Clocking
- Functionally Similar to National Semiconductor DM74LS962
- Dependable Texas Instruments Quality and Reliability

description

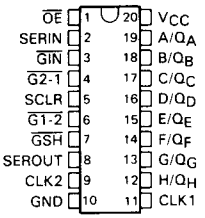
The 'ALS963 and 'ALS964 each contain an 8-bit shift register in parallel with an 8-bit I/O register. In addition to serial-to-parallel and parallel-to-serial conversions, these devices are capable of exchanging data between the shift and I/O registers. Control lines determine the mode of operation as shown in the function table.

The 'ALS963 features individual shift and I/O register clock inputs whereas the 'ALS964 features simultaneous register clocking through a single clock input. Clocking in both cases is achieved by positive transitions at the clock inputs.

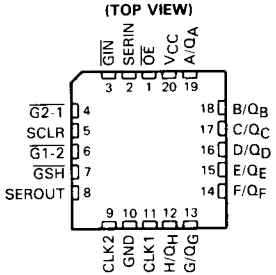
The clear function for the 'ALS963 is synchronous (active high). The 'ALS964 features active-high synchronous and asynchronous clearing.

The SN54ALS963 and SN54ALS964 are characterized for operation over the full military of −55°C to 125°C. The SN74ALS963 and SN74ALS964 are characterized for operation from 0°C to 70°C.

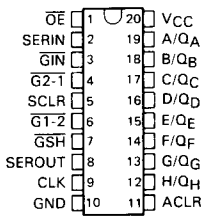
SN54ALS963 . . . JT PACKAGE
SN74ALS963 . . . DW OR NT PACKAGE
(TOP VIEW)



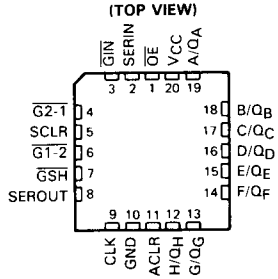
SN54ALS963 . . . FK PACKAGE
SN74ALS963 . . . FN PACKAGE
(TOP VIEW)



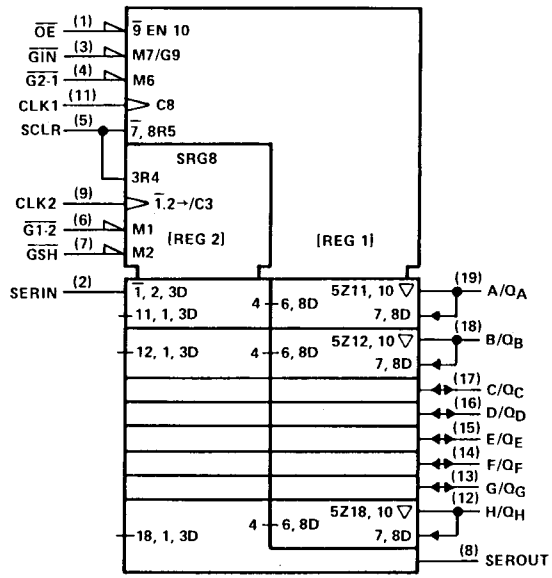
SN54ALS964 . . . JT PACKAGE
SN74ALS964 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS964 . . . FK PACKAGE
SN74ALS964 . . . FN PACKAGE
(TOP VIEW)

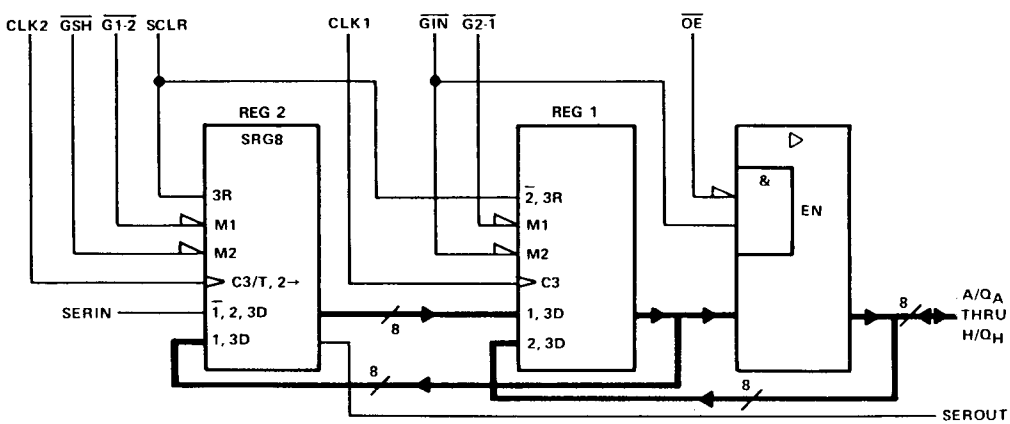


'ALS963 logic symbol†

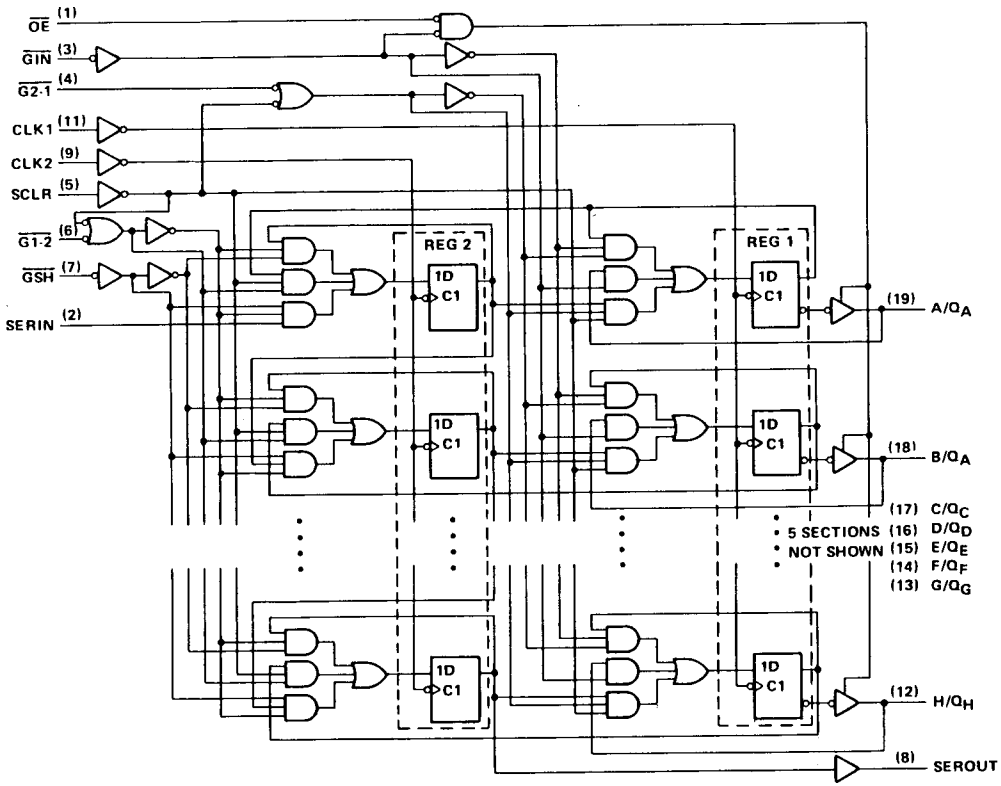


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS963 register-level logic diagram



'ALS963 gate-level logic diagram (positive logic)



'ALS963
FUNCTION TABLE

INPUTS								A/QA THROUGH H/QH	OPERATION OR FUNCTION
$\overline{OE}$	$\overline{GIN}$	$\overline{GE\text{-}1}$	$\overline{G1\text{-}2}$	$\overline{GSH}$	CLK1	CLK2	SCLR		
H	H	H	H	H	X	X	L	HI-Z	All data stable
L	H	H	H	H	X	X	L	OUTPUT	All data stable
X	L	H	H	H	↑	X	L	INPUT	Enter data from I/O into Reg 1
H	H	L	H	H	↑	X	L	HI-Z	Copy data from Reg 2 to Reg 1
L	H	L	H	H	↑	X	L	OUTPUT	Copy data from Reg 2 to Reg 1
X	L	L	H	H	↑	↑	L	INPUT	Reg 1 ORs data from Reg 2 and I/O
H	H	H	L	X	X	↑	L	HI-Z	Copy data from Reg 1 to Reg 2
L	H	H	L	X	X	↑	L	OUTPUT	Copy data from Reg 1 to Reg 2
X	L	H	L	X	↑	↑	L	INPUT	Copy data from Reg 1 to Reg 2, enter new data from I/O into Reg 1
H	H	L	L	X	↑	↑	L	HI-Z	Exchange data between registers
L	H	L	L	X	↑	↑	L	OUTPUT	Exchange data between registers
X	L	L	L	X	↑	↑	L	INPUT	Copy data from Reg 1 to Reg 2, Reg 1 ORs data from Reg 2 and I/O
H	H	H	H	L	X	↑	L	HI-Z	Shift data in Reg 2
L	H	H	H	L	X	↑	L	OUTPUT	Shift data in Reg 2
X	L	H	H	L	↑	↑	L	INPUT	Shift data in Reg 2, enter new data from I/O into Reg 1
H	H	L	H	L	↑	↑	L	HI-Z	Copy data from Reg 2 to Reg 1, shift data in Reg 2
L	H	L	H	L	↑	↑	L	OUTPUT	Copy data from Reg 2 to Reg 1, shift data in Reg 2
X	L	L	H	L	↑	↑	L	INPUT	Reg 1 ORs data from Reg 2 and I/O, shift data in Reg 2
X	H	X	X	X	↑	X	H		Synchronously clear Reg 1
X	X	X	X	X	X	↑	H		Synchronously clear Reg 2
X	H	X	X	X	↑	↑	H		Synchronously clear both registers
X	L	X	X	X	↑	↑	H	INPUT	Enter data from I/O into Reg 1 and synchronously clear Reg 2
X	L	X	X	X	↑	X	H	INPUT	Enter data from I/O into Reg 1

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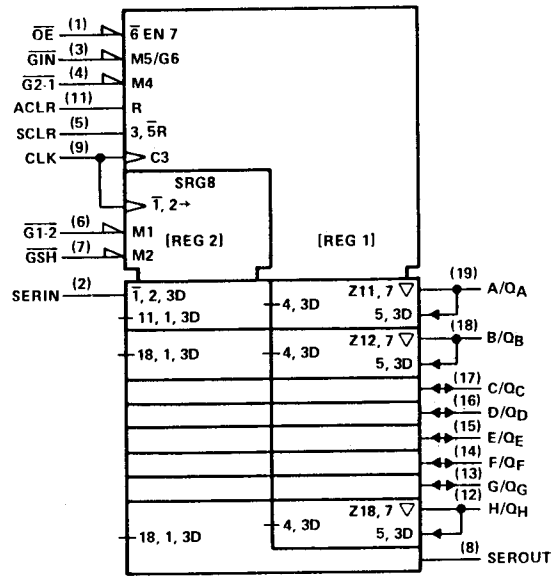
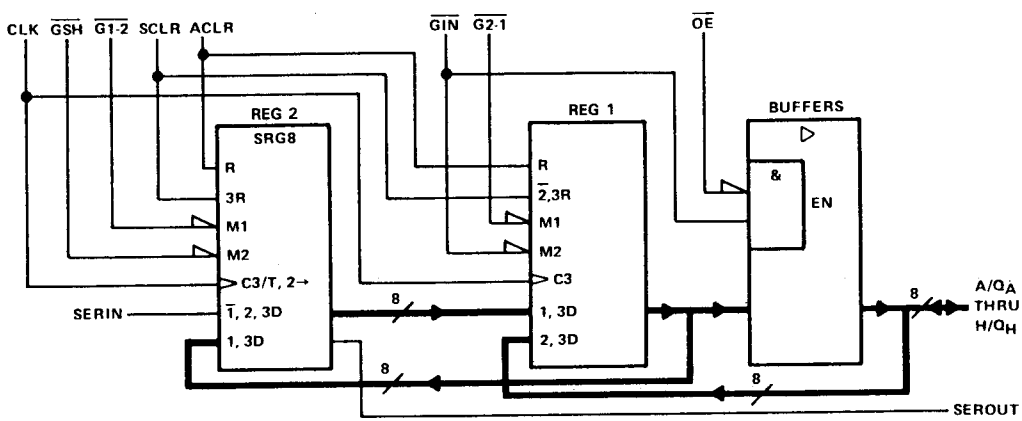
'ALS964 logic symbol†

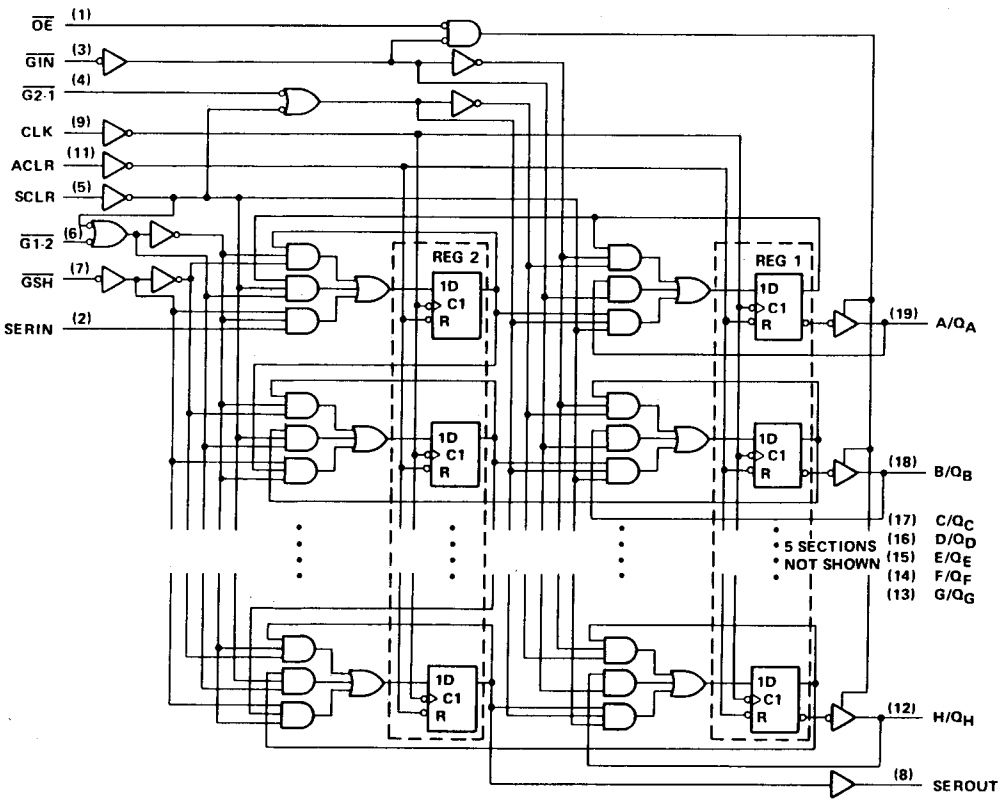


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS964 register-level logic diagram



'ALS964 gate-level logic diagram (positive logic)



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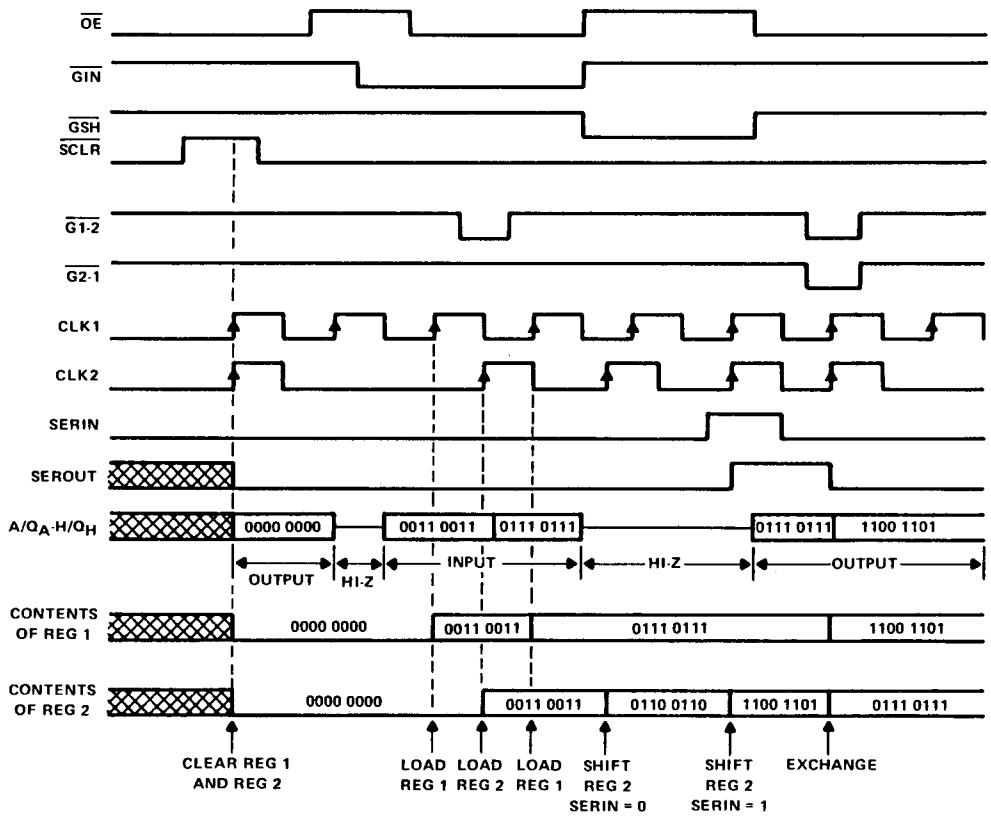
'ALS964
FUNCTION TABLE

INPUTS								A/QA THROUGH H/QH	OPERATION OR FUNCTION
$\overline{OE}$	$\overline{GIN}$	$\overline{G2\text{-}1}$	$\overline{G1\text{-}2}$	$\overline{GSH}$	CLK	ACLR	SCLR		
H	H	H	H	H	X	L	L	HI-Z	All data stable
L	H	H	H	H	X	L	L	OUTPUT	All data stable
X	L	H	H	H	↑	L	L	INPUT	Enter data from I/O into Reg 1
H	H	L	H	H	↑	L	L	HI-Z	Copy data from Reg 2 to Reg 1
L	H	L	H	H	↑	L	L	OUTPUT	Copy data from Reg 2 to Reg 1
X	L	L	H	H	↑	L	L	INPUT	Reg 1 ORs data from Reg 2 and I/O
H	H	H	L	X	↑	L	L	HI-Z	Copy data from Reg 1 to Reg 2
L	H	H	L	X	↑	L	L	OUTPUT	Copy data from Reg 1 to Reg 2
X	L	H	L	X	↑	L	L	INPUT	Copy data from Reg 1 to Reg 2, enter new data from I/O into Reg 1
H	H	L	L	X	↑	L	L	HI-Z	Exchange data between registers
L	H	L	L	X	↑	L	L	OUTPUT	Exchange data between registers
X	L	L	L	X	↑	L	L	INPUT	Copy data from Reg 1 to Reg 2, Reg 1 ORs data from Reg 2 and I/O
H	H	H	H	L	↑	L	L	HI-Z	Shift data in Reg 2
L	H	H	H	L	↑	L	L	OUTPUT	Shift data in Reg 2
X	L	H	H	L	↑	L	L	INPUT	Shift data in Reg 2, enter new data from I/O into Reg 1
H	H	L	H	L	↑	L	L	HI-Z	Copy data from Reg 2 to Reg 1, shift data in Reg 2
L	H	L	H	L	↑	L	L	OUTPUT	Copy data from Reg 2 to Reg 1, shift data in Reg 2
X	L	L	H	L	↑	L	L	INPUT	Reg 1 ORs data from Reg 2 and I/O, shift data in Reg 2
X	H	X	X	X	↑	L	H		Synchronously clear Reg 1 and Reg 2
X	X	X	X	X	X	H	X		Asynchronously clear Reg 1 and Reg 2
X	L	X	X	X	↑	L	H	INPUT	Enter data from I/O into Reg 1 and synchronously clear Reg 2

'ALS963 typical sequence

Illustrated below is the following sequence:

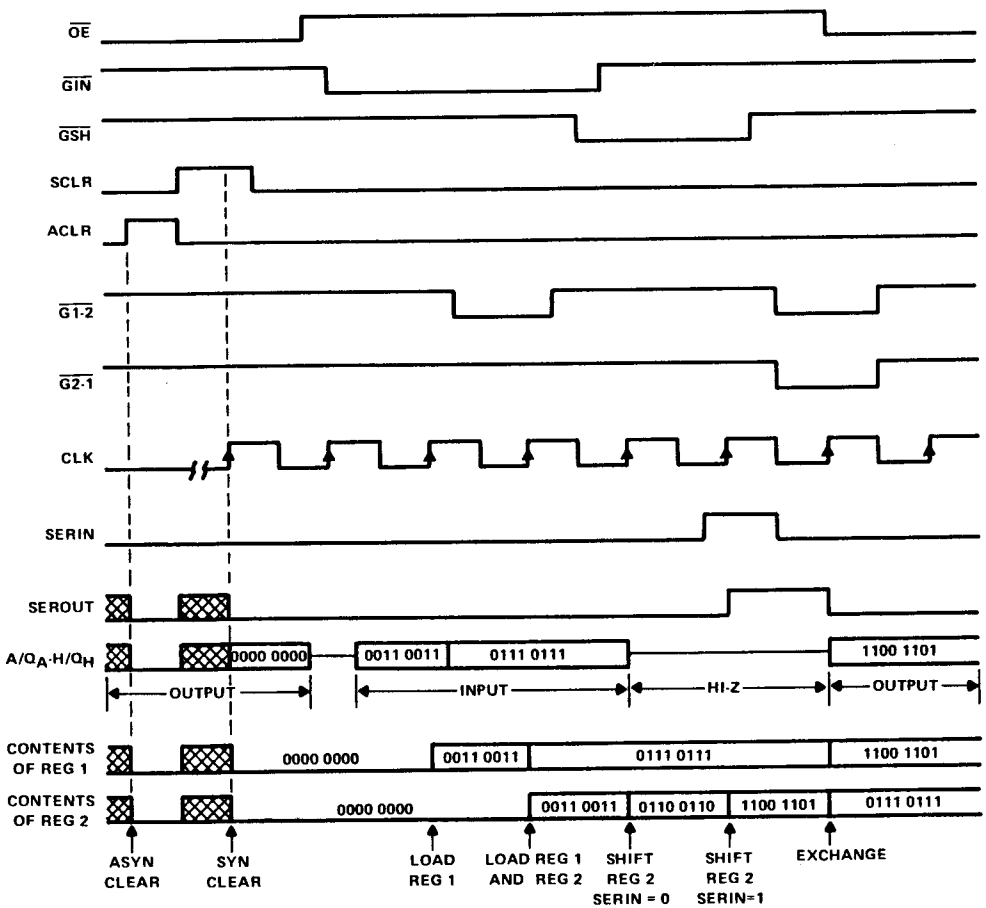
1. Clear both registers to zero.
2. Input 0011 0011 in Reg 1.
3. Transfer 0011 0011 from Reg 1 to Reg 2.
4. Input 0111 0111 into Reg 1.
5. Shift contents of Reg 2, SERIN = 0
6. Shift contents of Reg 2, SERIN = 1
7. Exchange contents of Reg 1 with Reg 2.



'ALS964 typical sequence

Illustrated below is the following sequence:

1. Asynchronously clear Reg 1 and Reg 2 to zero, operate, then synchronously clear.
2. Input 0011 0011 into Reg 1.
3. Transfer 0011 0011 from Reg 1 to Reg 2 and input 0111 0111 into Reg 1.
4. Shift contents of Reg 2, SERIN = 0
5. Shift contents of Reg 2, SERIN = 1
6. Exchange contents of Reg 1 with Reg 2.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS963, SN54ALS964 . . . . . −55°C to 125°C
SN74ALS963, SN74ALS964 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

'ALS963 recommended operating conditions

			SN54ALS963			SN74ALS963			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current	SEROUT			8			16	mA
		Q_A thru Q_H			12			24	
f_{clock}	Clock frequency (at 50% duty cycle)		0		25	0		25	MHz
t_w	Pulse duration	CLK1 high or low	20			20			ns
		CLK2 high or low	20			20			
t_{su}	Setup time	Data before CLK1↑							ns
		$\overline{GIN}$ before CLK1↑							
		$\overline{G1\text{-}2}$ before CLK2↑							
		$\overline{G2\text{-}1}$ before CLK1↑							
		$\overline{GSH}$ before CLK2↑							
		SCLR before CLK1↑ or CLK2↑							
t_h	Hold time after CLK1↑ or CLK2↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

'ALS964 recommended operating conditions

			SN54ALS964			SN74ALS964			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current	SEROUT			8			16	mA
		Q_A thru Q_H			12			24	
f_{clock}	Clock frequency (at 50% duty cycle)		0		25	0		25	MHz
t_w	Pulse duration	CLK high or low	20			20			ns
		ACLR low							
t_{su}	Setup time	Data before CLK↑							ns
		$\overline{GIN}$ before CLK↑							
		$\overline{G1\text{-}2}$ before CLK↑							
		$\overline{G2\text{-}1}$ before CLK↑							
		$\overline{GSH}$ before CLK↑							
		SCLR before CLK↑							
t_h	Hold time after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS963 SN54ALS964			SN74ALS963 SN74ALS964			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	SEROUT	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 16 mA					0.35	0.5	
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS963	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							
	'ALS964	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled							

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports (Q_A throuh Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS963 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS963			SN74ALS963			
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CLK1 or CLK2	Any Q	25	30		25	30		MHz
t_{PLH}	CLK1	Any Q			10			10	ns
t_{PHL}					14			14	
t_{PLH}	CLK2	SEROUT			10			10	ns
t_{PHL}					14			14	
t_{PHZ}	$\overline{OE}$	Any Q			15			15	ns
t_{PLZ}					18			18	
t_{PZH}	$\overline{OE}$	Any Q			12			12	ns
t_{PZL}					12			12	

'ALS964 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS964			SN74ALS964			
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CLK	Any Q	25	30		25	30		MHz
t_{PLH}	CLK	Any Q			10			10	ns
t_{PHL}					14			14	
t_{PLH}	CLK	SEROUT			10			10	ns
t_{PHL}					14			14	
t_{PHZ}	ACLR	Any Q or SEROUT			14			14	ns
t_{PHZ}	$\overline{OE}$	Any Q			15			15	ns
t_{PLZ}					18			18	
t_{PZH}	$\overline{OE}$	Any Q			12			12	ns
t_{PZL}					12			12	

NOTE: Load circuit and voltage waveforms are shown in Section 1.

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