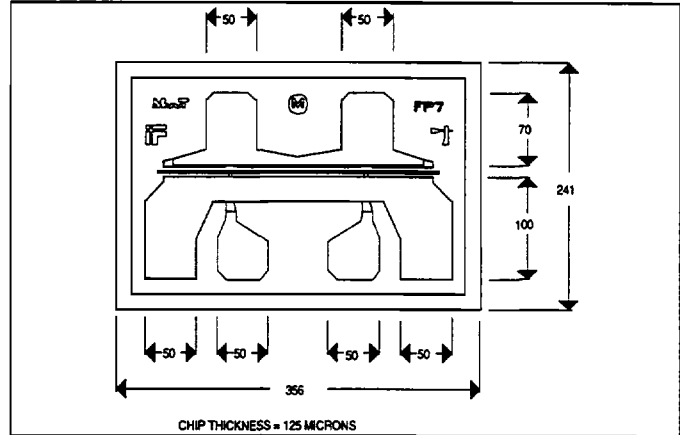


MwT-S7

18 GHz High Gain, Low Noise GaAs FET

- HIGH AVAILABLE GAIN WHEN BIASED FOR LOW-NOISE
- EXCELLENT FOR BROADBAND GAIN OR OSCILLATOR BUFFER APPLICATIONS
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- 250 MICRON GATE WIDTH
- CHOICE OF CHIP AND TWO PACKAGE TYPES

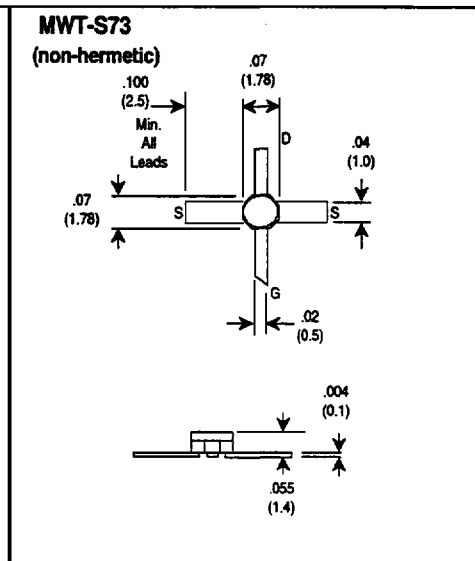
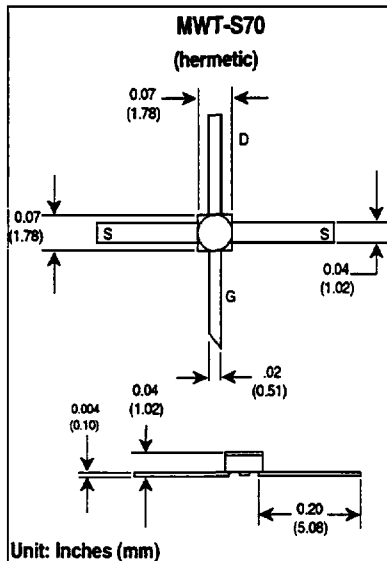


DESCRIPTION

The MwT-S7 is a GaAs MESFET device whose nominal quarter-micron gate length and 250 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 18 GHz frequency range while exhibiting low noise figure. The straight gate geometry of the MwT-S7 makes it equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. Processing which guarantees low phase noise makes the MwT-S7 particularly attractive for oscillator applications. The chip is produced using MwT's reliable metal system and all devices are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability. Designers can use MwT's unique BIN selection feature to choose devices from narrow I_{DSS} ranges, insuring consistent circuit operation.

RF SPECIFICATIONS AT $T_a = 25^\circ\text{C}$

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MwT-S7 LN MwT-S770 LN MwT-S773 LN		
				MIN	TYP	MAX
NF _{opt}	Optimum Noise Figure V _{DS} =3.0 V I _{DS} =10mA	12GHZ	dB		1.5	1.8
GA	Gain at Optimum Noise Figure V _{DS} =3.0 V I _{DS} =10mA	12GHZ	dB	7.0	8.0	
P1dB	Output Power at 1dB Compression V _{DS} =4.5 V I _{DS} =0.6 I _{DSS} = 30mA	12GHZ	dBm		16.0	
SSG	Small Signal Gain V _{DS} =4.5 V I _{DS} =0.6 I _{DSS} = 30mA	12GHZ	dB	10.0	11.0	
I _{DSS}	Recommended I _{DSS} Range for Optimum P1dB		mA		34-70	



DC SPECIFICATIONS AT Ta = 25 °C

* Overall Rth depends on case mounting

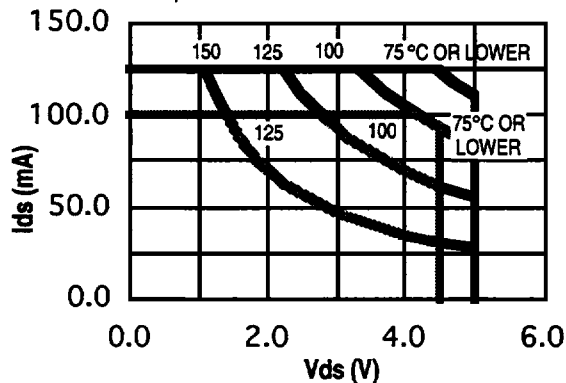
SYMBOL	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Idss	Saturated Drain Current Vds=3.0 V VGS=0.0 V	mA	26		98
Gm	Transconductance Vds=3.0 V VGS=0.0 V	mS	45	60	
Vp	Pinch-off Voltage Vds=3.0 V IDS=1.0 mA	V		-1.5	-4.5
BVGSO	Gate-to-Source Breakdown Voltage Igs=-0.4 mA, Igd=0	V	-4.0	-7.0	
BVGDO	Gate-to-Drain Breakdown Voltage Igd=-0.4 mA, Igs=0	V	-5.0	-7.0	
Rth	Thermal Resistance* MwT-S7 Chip MwT-S770,S773	°CW			180 380*

MAXIMUM RATINGS AT Ta = 25 °C

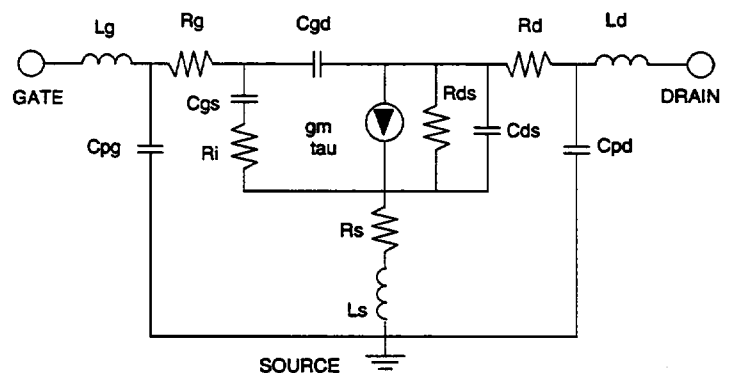
SYMBOL	PARAMETER	UNITS	CONT MAX ¹	ABSOLUTE MAX ²
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	50	75

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

SAFE OPERATING LIMITS vs. Case Temperature



DEVICE EQUIVALENT CIRCUIT MODEL



PARAMETER		VALUE	
Gate Bond Wire Inductance	Lg	0.13	nH
Gate Pad Capacitance	Cpg	0.05	pF
Gate Resistance	Rg	0.2	Ω
Gate-Source Capacitance	Cgs	0.314	pF
Channel Resistance	Ri	6.9	Ω
Gate-Drain Capacitance	Cgd	0.027	pF
Transconductance	gm	69.0	mS
Transit time	tau	2.0	psec

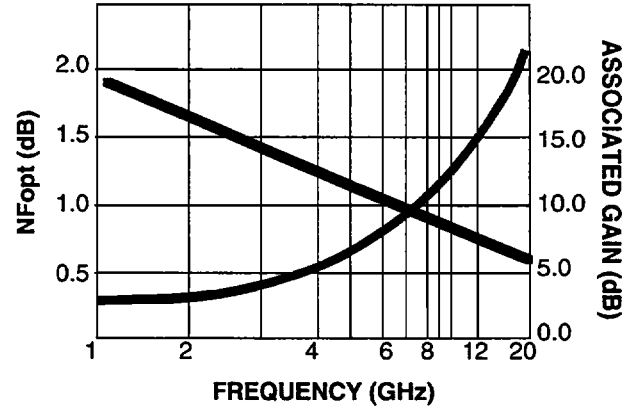
PARAMETER		VALUE	
Source Resistance	Rs	2.6	Ω
Source Inductance	Ls	0.025	nH
Drain-Source Resistance	Rds	173.0	Ω
Drain-Source Capacitance	Cds	0.07	pF
Drain Resistance	Rd	3.67	Ω
Drain Pad Capacitance	Cpd	0.027	pF
Drain Inductance	Ld	0.159	nH

TYPICAL NOISE PARAMETERS

MwT-S7LN Chip: VDS = 3 V, IDS = 12 mA

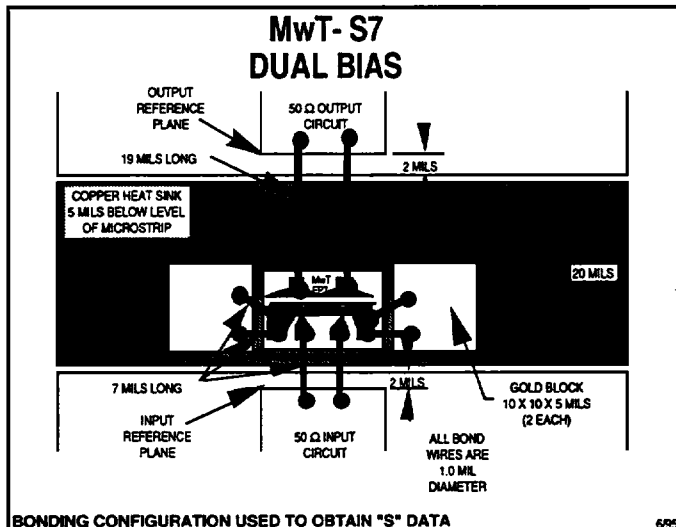
FREQUENCY GHz	NF MIN dB	GAMMA OPT		Rn/50
		MAG	ANGLE	
2.00	0.29	0.68	27.0	0.188
4.00	0.56	0.49	57.0	0.182
8.00	1.06	0.41	114.0	0.165
12.00	1.50	0.49	149.0	0.152
16.00	1.89	0.55	168.0	0.143
18.00	2.10	0.58	175.0	0.140

NOISE FIGURE AND ASSOCIATED GAIN VS. FREQUENCY



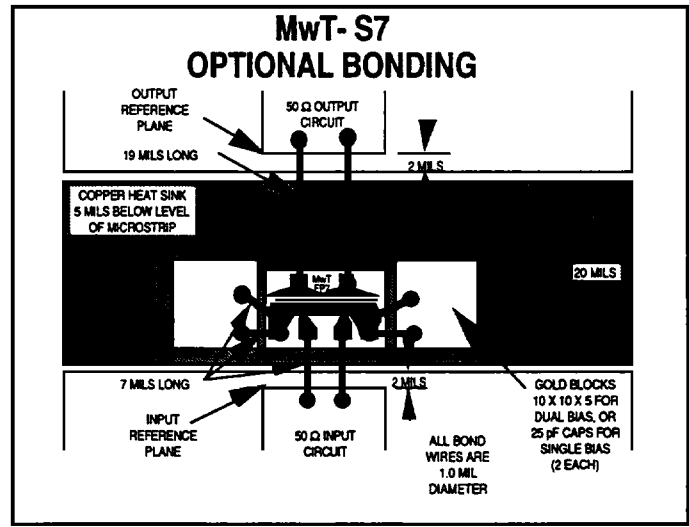
RECOMMENDED ASSEMBLY CONFIGURATION

Shown below is the assembly and bonding configuration used for S-Parameter measurements of the MwT-S7 chip. This configuration is recommended for optimum performance. For single-bias applications the gold blocks may be replaced by capacitors. An additional interconnecting bond would then be required. Contact MwT for additional applications information.



BONDING CONFIGURATION USED TO OBTAIN "S" DATA

Contact MwT for bonding configuration to be used when substituting the MwT-7 for the NEC 710. Ask for Application Note DEV101.



Contact MwT for bonding configuration to be used when substituting the MwT-7 for the NEC 710. Ask for Application Note DEV101.

BIN SELECTION

Every MwT-S7 wafer has been probed for Idss and the data stored on computer disk. Customers may select from Idss values in any of 18 current bins, as shown below, to insure consistent performance in their circuit. The shaded bins are typically available in smaller quantity and caution is advised before designing these bins into high production applications. MwT's "Smart Wafer Picker" reads the stored Idss Data from the disk and devices from customer selected bins are quickly and automatically picked from the wafer and loaded into shipping containers.

BIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
IDSS (mA)	26-30	30-34	34-38	38-42	42-46	46-50	50-54	54-58	58-62	62-66	66-70	70-74	74-78	78-82	82-86	86-90	90-94	94-98

BIN ACCURACY

Due to the effects of temperature, dc loading and probe tip varnishing, the IDSS from the "on wafer" probing of any MwT device may differ after it has been attached to a proper heat sink and tested in an RF or DC circuit.

Because of the aforementioned effects, the IDSS distribution may deviate as much as +/- 1 bin within the range identified on the label of each die shipping container, and +/- 2 bins within the selected range.

DEVICE HANDLING PROCEDURE

- 1) Open package in clean room environment only.
- 2) GaAs FETs are sensitive to electrostatic discharge. Precautions should be taken in handling, die attachment, and bonding to assure that Maximum Ratings are not exceeded as a result of electrical discharge.
- 3) Chips have been cleaned and are ready for die attachment. DO NOT attempt to re-clean.
- 4) Assembly should be performed with parts no hotter than 300° C. All circuit components (such as resistors and capacitors) should be assembled completely before the FET is die attached. Assembly should be performed as quickly as possible. In general, no chip should be left at 300°C for over 2 minutes.
- 5) Die attach with clean AuSn alloy under forming gas at 280 to 300° C. Scrub chip down with tweezers. Thermal resistance is critically dependent on this operation.
- 6) Thermasonic wedge bonding is recommended. A .0015 in. bond flat wedge at 125 to 150° C should be used with a heater stage temperature of 200 to 225° C. Apply 15 to 20 grams of bond force to .001 in. diameter gold wire with an elongation of 2 to 5%.
- 7) Store in a clean, dry, inert environment such as nitrogen at room temperature.
- 8) CAUTION: Handling of chips other than as specified above may cause permanent damage.