CHAPTER 1
PINOUTS

1.1. PINOUT DIAGRAMS

1.1.1. Pentium™ Processor Pinouts

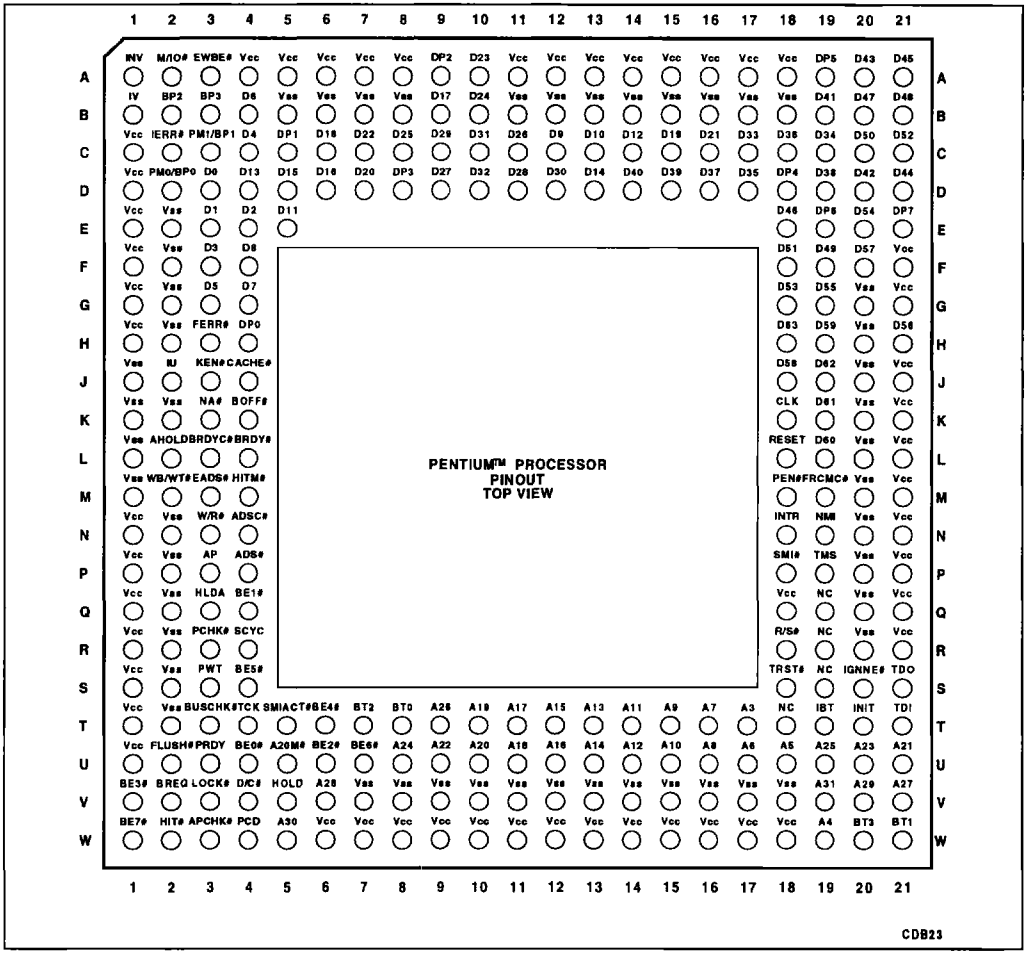

Figure 1-1. Pentium™ Processor Pinout (Top View)

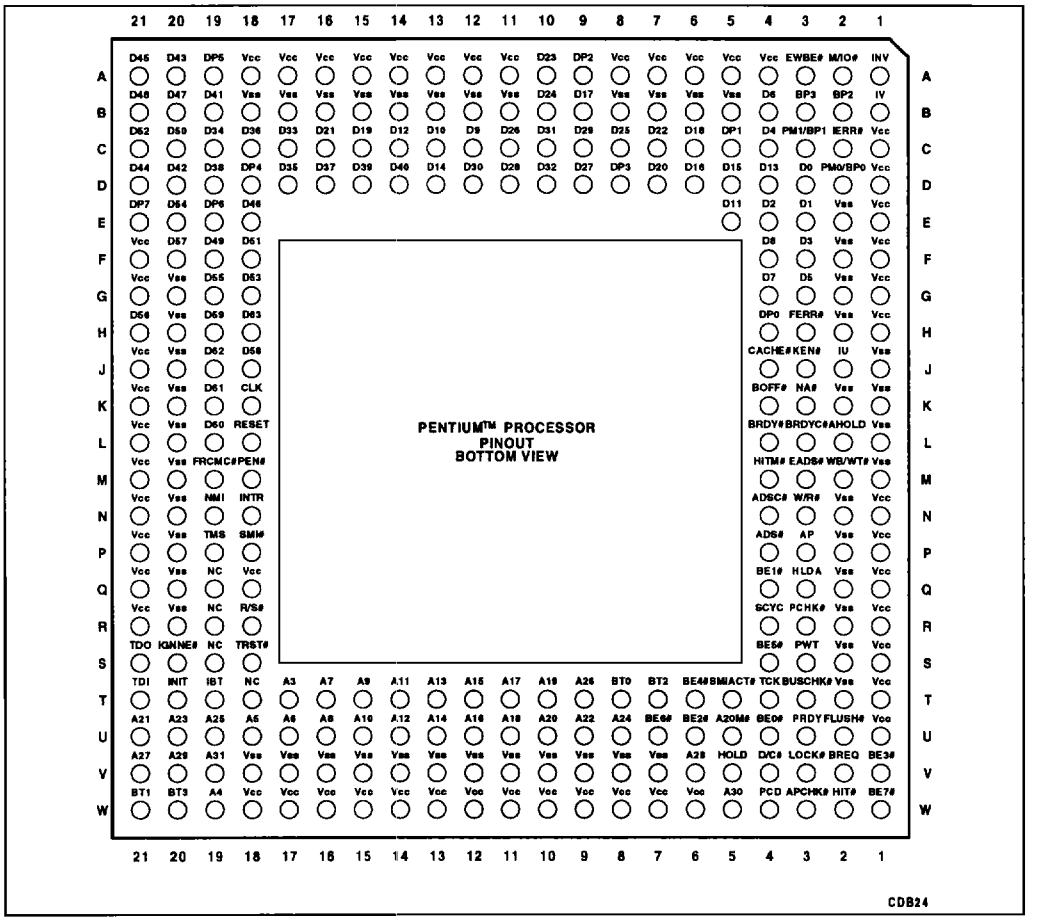

Figure 1-2. Pentium™ Processor Pinout (Bottom View)

1.1.2. 82496 Cache Controller Pinouts

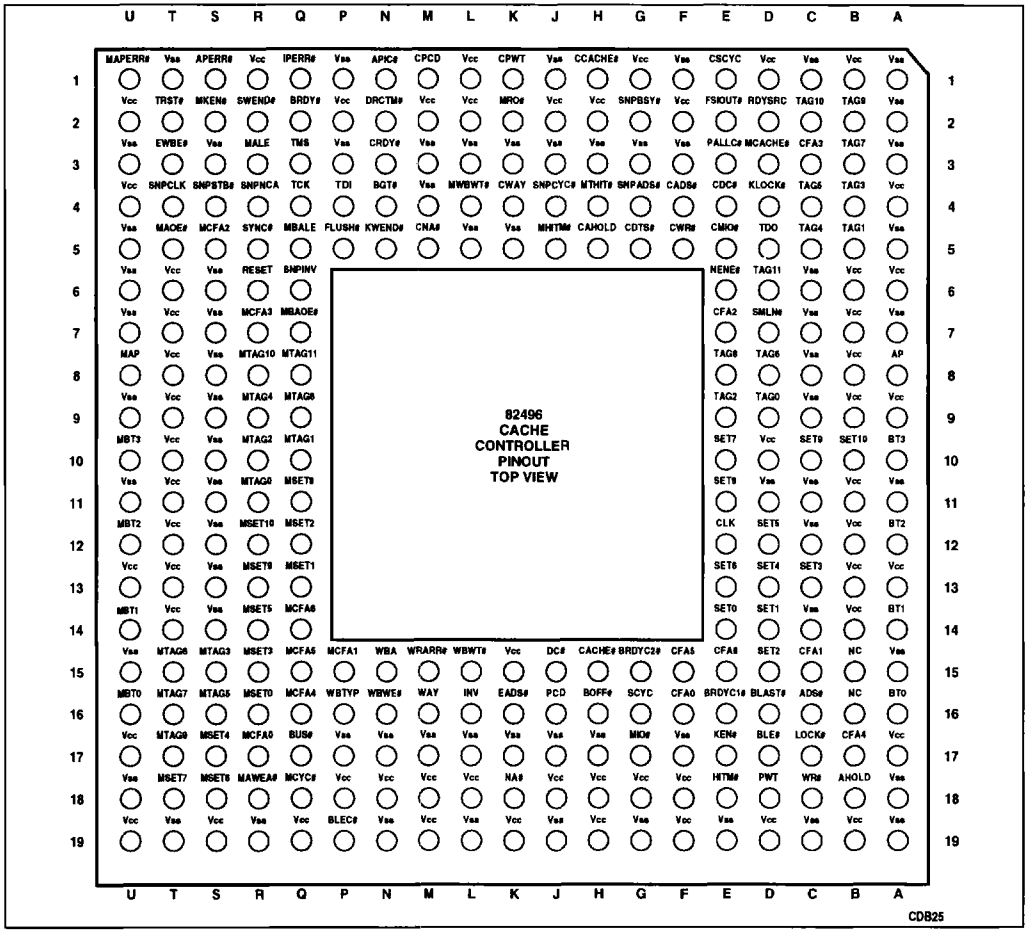

Figure 1-3. 82496 Cache Controller Pinout (Top View)

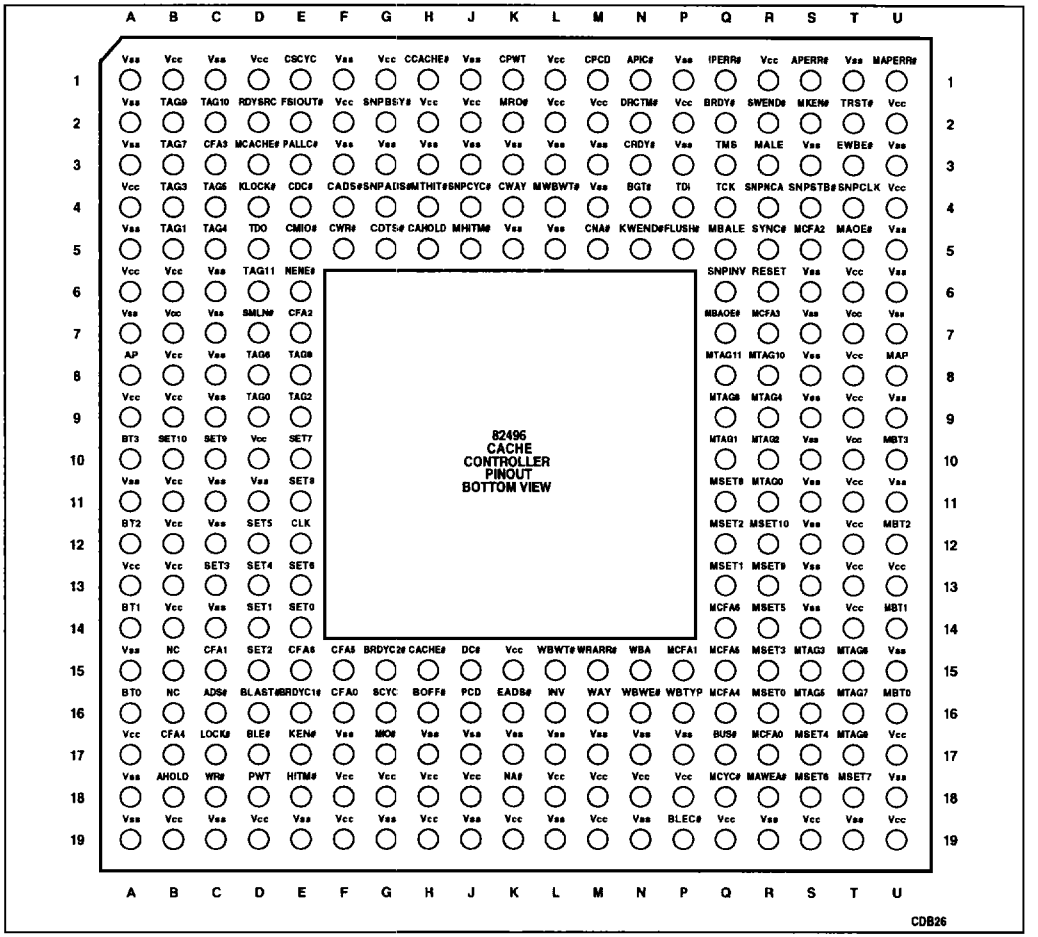

Figure 1-4. 82496 Cache Controller Pinout (Bottom View)

1.1.3. 82491 Cache SRAM Memory Pinouts

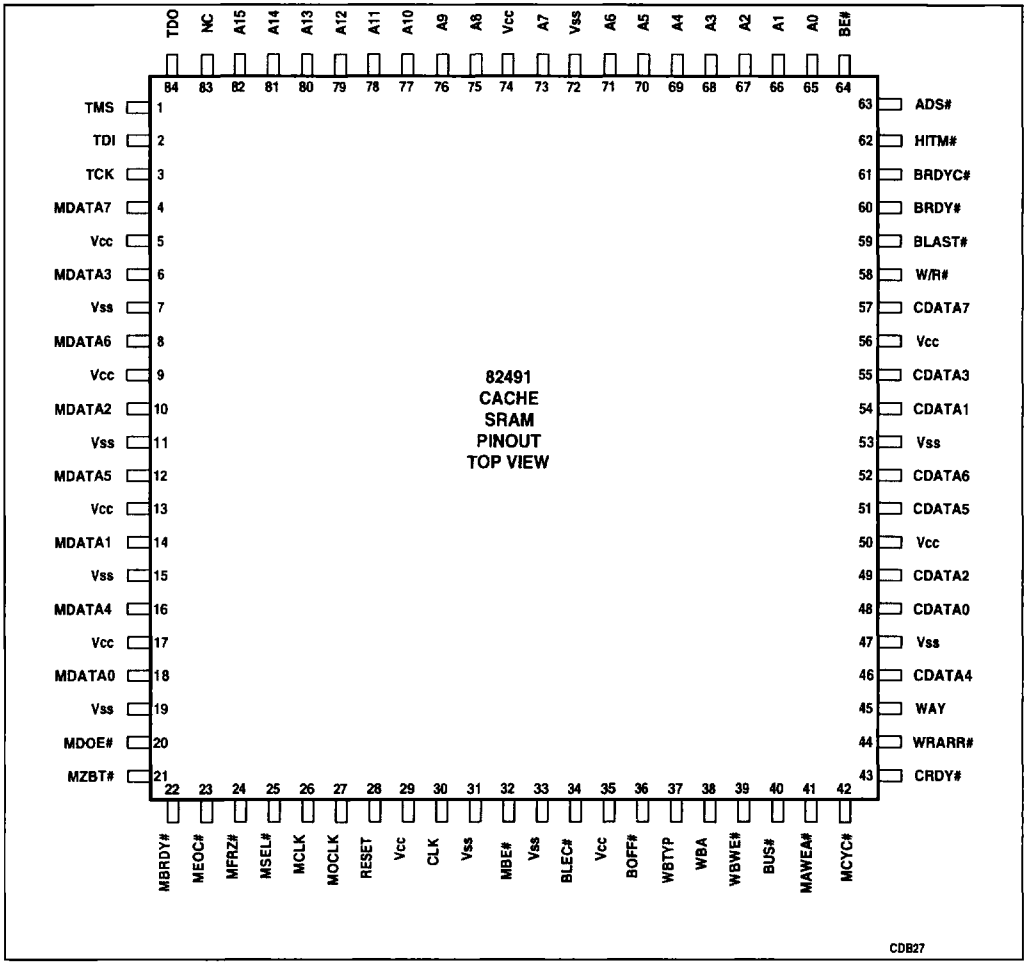

Figure 1-5. 82491 Cache SRAM Memory Pinout (Top View)

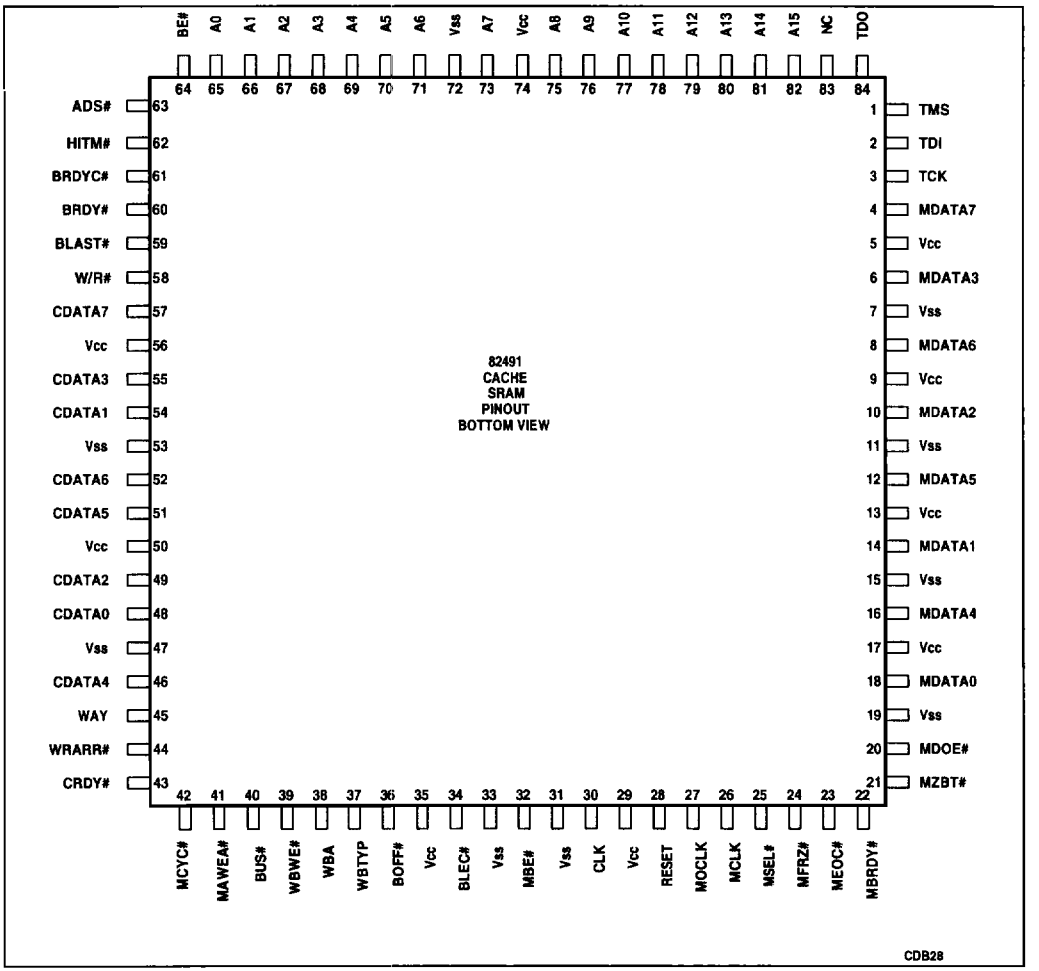

Figure 1-6. 82491 Cache SRAM Pinout (Bottom View)

1.2. PIN CROSS REFERENCE TABLES

1.2.1. Pentium Processor

Table 1-1. Pentium™ Processor Pin Cross Reference by Pin Name

Address		Data				Control			
A3	T17	D0	D03	D32	D10	A20M#	U05	FRCMC#	M19
A4	W19	D1	E03	D33	C17	ADS#	P04	HIT#	W02
A5	U18	D2	E04	D34	C19	ADSC#	N04	HITM#	M04
A6	U17	D3	F03	D35	D17	AHOLD	L02	HLDA	Q03
A7	T16	D4	C04	D36	C18	AP	P03	HOLD	V05
A8	U16	D5	G03	D37	D16	APCHK#	W03	IBT	T19
A9	T15	D6	B04	D38	D19	BE0#	U04	IERR#	C02
A10	U15	D7	G04	D39	D15	BE1#	Q04	IGNNE#	S20
A11	T14	D8	F04	D40	D14	BE2#	U06	INIT	T20
A12	U14	D9	C12	D41	B19	BE3#	V01	INTR	N18
A13	T13	D10	C13	D42	D20	BE4#	T06	INV	A01
A14	U13	D11	E05	D43	A20	BE5#	S04	IU	J02
A15	T12	D12	C14	D44	D21	BE6#	U07	IV	B01
A16	U12	D13	D04	D45	A21	BE7#	W01	KEN#	J03
A17	T11	D14	D13	D46	E18	BOFF#	K04	LOCK#	V03
A18	U11	D15	D05	D47	B20	BP2	B02	M/IO#	A02
A19	T10	D16	D06	D48	B21	BP3	B03	NA#	K03
A20	U10	D17	B09	D49	F19	BRDY#	L04	NMI	N19
A21	U21	D18	C06	D50	C20	BRDYC#	L03	PCD	W04
A22	U09	D19	C15	D51	F18	BREQ	V02	PCHK#	R03
A23	U20	D20	D07	D52	C21	BUSCHK#	T03	PEN#	M18
A24	U08	D21	C16	D53	G18	CACHE#	J04	PM0/BP0	D02
A25	U19	D22	C07	D54	E20	CLK	K18	PM1/BP1	C03
A26	T09	D23	A10	D55	G19	D/C#	V04	PRDY	U03

Table 1-1. Pentium™ Processor Pin Cross Reference by Pin Name (Contd.)

Address		Data				Control			
A27	V21	D24	B10	D56	H21	DP0	H04	PWT	S03
A28	V06	D25	C08	D57	F20	DP1	C05	R/S#	R18
A29	V20	D26	C11	D58	J18	DP2	A09	RESET	L18
A30	W05	D27	D09	D59	H19	DP3	D08	SCYC	R04
A31	V19	D28	D11	D60	L19	DP4	D18	SMI#	P18
		D29	C09	D61	K19	DP5	A19	SMIACT#	T05
BT0	T08	D30	D12	D62	J19	DP6	E19	TCK	T04
BT1	W21	D31	C10	D63	H18	DP7	E21	TDI	T21
BT2	T07					EADS#	M03	TDO	S21
BT3	W20					EWBE#	A03	TMS	P19
						FERR#	H03	TRST#	S18
						FLUSH#	U02	W/R#	N03
								WB/WT#	M02

V_{CC}				V_{SS}					
A04	C01	N21	W08	B05	B15	H02	L20	Q20	V10
A05	D01	P01	W09	B06	B16	H20	M01	R02	V11
A06	E01	P21	W10	B07	B17	J01	M20	R20	V12
A07	F01	Q01	W11	B08	B18	J20	N02	S02	V13
A08	F21	Q18	W12	B11	E02	K01	N20	T02	V14
A11	G01	Q21	W13	B12	F02	K02	P02	V07	V15
A12	G21	R01	W14	B13	G02	K20	P20	V08	V16
A13	H01	R21	W15	B14	G20	L01	Q02	V09	V17
A14	J21	S01	W16						V18
A15	K21	T01	W17						
A16	L21	U01	W18						
A17	M21	W06			**NC:**	Q19	S19	R19	T18
A18	N01	W07							

1.2.2. 82496 Cache Controller

Table 1-2. 82496 Cache Controller Pin Cross Reference by Pin Name

Cache Control							
ADS#	C16	CNA#	M05	MAOE#	T05	SNPADS#	G04
AHOLD	B18	CPCD	M01	MAP	U08	SNPBSY#	G02
AP	A08	CPWT	K01	MAPERR#	U01	SNPCLK	T04
APERR#	S01	CRDY#	N03	MAWEA#	R18	SNPCYC#	J04
APIC#	N01	CSCYC	E01	MBALE	Q05	SNPINV	Q06
BGT#	N04	CW/R#	F05	MBAOE#	Q07	SNPNCA	R04
BLAST#	D16	CWAY	K04	MCACHE#	D03	SNPSTB#	S04
BLE#	D17	D/C#	J15	MCYC#	Q18	SWEND#	R02
BLEC#	P19	DRCTM#	N02	MHITM#	J05	SYNC#	R05
BOFF#	H16	EADS#	K16	MKEN#	S02	TCK	Q04
BRDY#	Q02	EWBE#	T03	MRO#	K02	TDI	P04
BRDYC1#	E16	FLUSH#	P05	MTHIT#	H04	TDO	D05
BRDYC2#	G15	FSIOUT#	E02	MWB/WT#	L04	TMS	Q03
BUS#	Q17	HITM#	E18	NA#	K18	TRST#	T02
CACHE#	H15	INV	L16	NENE#	E06	W/R#	C18
CADS#	F04	IPERR#	Q01	PALLC#	E03	WAY	M16
CAHOLD	H05	KEN#	E17	PCD	J16	WB/WT#	L15
CCACHE#	H01	KLOCK#	D04	PWT	D18	WBA	N15
CD/C#	E04	KWEND#	N05	RDYSRC	D02	WBTYP	P16
CDTS#	G05	LOCK#	C17	RESET	R06	WBWE#	N16
CLK	E12	M/IO#	G17	SCYC	G16	WRARR#	M15
CM/IO#	E05	MALE	R03	SMLN#	D07		

Table 1-2. 82496 Cache Controller Pin Cross Reference by Pin Name (Contd.)

CPU Bus Address					
CFA0	F16	SET0	E14	TAG0	D09
CFA1	C15	SET1	D14	TAG1	B05
CFA2	E07	SET2	D15	TAG2	E09
CFA3	C03	SET3	C13	TAG3	B04
CFA4	B17	SET4	D13	TAG4	C05
CFA5	F15	SET5	D12	TAG5	C04
CFA6	E15	SET6	E13	TAG6	D08
		SET7	E10	TAG7	B03
BT0	A16	SET8	E11	TAG8	E08
BT1	A14	SET9	C10	TAG9	B02
BT2	A12	SET10	B10	TAG10	C02
BT3	A10			TAG11	D06
Memory Bus Address					
MCFA0	R17	MSET0	R16	MTAG0	R11
MCFA1	P15	MSET1	Q13	MTAG1	Q10
MCFA2	S05	MSET2	Q12	MTAG2	R10
MCFA3	R07	MSET3	R15	MTAG3	S15
MCFA4	Q16	MSET4	S17	MTAG4	R09
MCFA5	Q15	MSET5	R14	MTAG5	S16
MCFA6	Q14	MSET6	S18	MTAG6	T15
		MSET7	T18	MTAG7	T16
MBT0	U16	MSET8	Q11	MTAG8	Q09
MBT1	U14	MSET9	R13	MTAG9	T17
MBT2	U12	MSET10	R12	MTAG10	R08
MBT3	U10			MTAG11	Q08

Table 1-2. 82496 Cache Controller Pin Cross Reference by Pin Name (Contd.)

V_{SS}			V_{CC}		
A01	G03	R19	A04	F02	P02
A02	G19	S03	A06	F18	P18
A03	H03	S06	A09	F19	Q19
A05	H17	S07	A13	G01	R01
A07	J01	S08	A17	G18	S19
A11	J03	S09	B01	H02	T06
A15	J17	S10	B06	H18	T07
A18	J19	S11	B07	H19	T08
A19	K03	S12	B08	J02	T09
C01	K05	S13	B09	J18	T10
C06	K17	S14	B11	K15	T11
C07	L03	T01	B12	K19	T12
C08	L05	T19	B13	L01	T13
C09	L17	U03	B14	L02	T14
C11	L19	U05	B19	L18	U02
C12	M03	U06	D01	M02	U04
C14	M04	U07	D10	M18	U13
C19	M17	U09	D19	M19	U17
D11	N17	U11		N18	U19
E19	N19	U15			
F01	P01	U18			
F03	P03		**NC:**	B15	B16
F17	P17				

1.2.3. 82491 Cache SRAM

Table 1-3. 82491 Cache SRAM Pin Cross Reference by Pin Name

Address		CPU Bus Data		Control			
A0	65	CDATA0	48	ADS#	63	MEOC#	23
A1	66	CDATA1	54	BE#	64	MFRZ#	24
A2	67	CDATA2	49	BLAST#	59	MOCLK	27
A3	68	CDATA3	55	BLEC#	34	MSEL#	25
A4	69	CDATA4	46	BOFF#	36	MZBT#	21
A5	70	CDATA5	51	BRDY#	60	RESET	28
A6	71	CDATA6	52	BRDYC#	61	TCK	3
A7	73	CDATA7	57	BUS#	40	TDI	2
A8	75	Memory Bus Data		CLK	30	TDO	84
A9	76			CRDY#	43	TMS	1
A10	77	MDATA0	18	HITM#	62	W/R#	58
A11	78	MDATA1	14	MAWEA#	41	WAY	45
A12	79	MDATA2	10	MBE#	32	WBA	38
A13	80	MDATA3	6	MBRDY#	22	WBTYP	37
A14	81	MDATA4	16	MCLK	26	WBWE#	39
A15	82	MDATA5	12	MCYC#	42	WRARR#	44
		MDATA6	8	MDOE#	20		
		MDATA7	4				

NC	V_{CC}			V_{SS}		
83	5	17	50	7	19	47
	9	29	56	11	31	53
	13	35	74	15	33	72

1.3. BRIEF PIN DESCRIPTIONS

This section provides brief descriptions of all signals of the Pentium™ processor cache chip set.

The # symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level.

Tables 1-4 through 1-9 list the signals which comprise each interface — both external (i.e., to the memory bus controller) and internal (i.e. the Pentium processor cache chip set optimized interface).

Figure 1-7 illustrates signal partitioning.

Table 1-10 describes all Pentium processor signals to which the Memory Bus Controller has access, all 82496 Cache Controller signals, all 82491 Cache SRAM signals, and all Optimized interface signals.

Tables 1-11 to 1-13 list the Pentium processor cache chip set signals which have internal pull-up or pull-down resistors and are glitch free.

Table 1-14 lists the interconnects between the optimized interface signals.

Tables 1-15 to 1-18 list pin states at reset, Output pins, Input pins, and Input/Output pins.

The following abbreviations may be used in Tables 1-7 through 1-18: P (Pentium processor), CC (82496 Cache Controller), and CS (82491 Cache SRAM).

For detailed Pentium processor pin descriptions, refer to the *Pentium™ Processor Data Book*. For detailed 82496 Cache Controller and 82491 Cache SRAM pin descriptions refer to the Hardware Interface chapter. **Note that all input pins must meet their AC/DC specifications to guarantee proper functional behavior of the 82496 Cache Controller and 82491 Cache SRAM.**

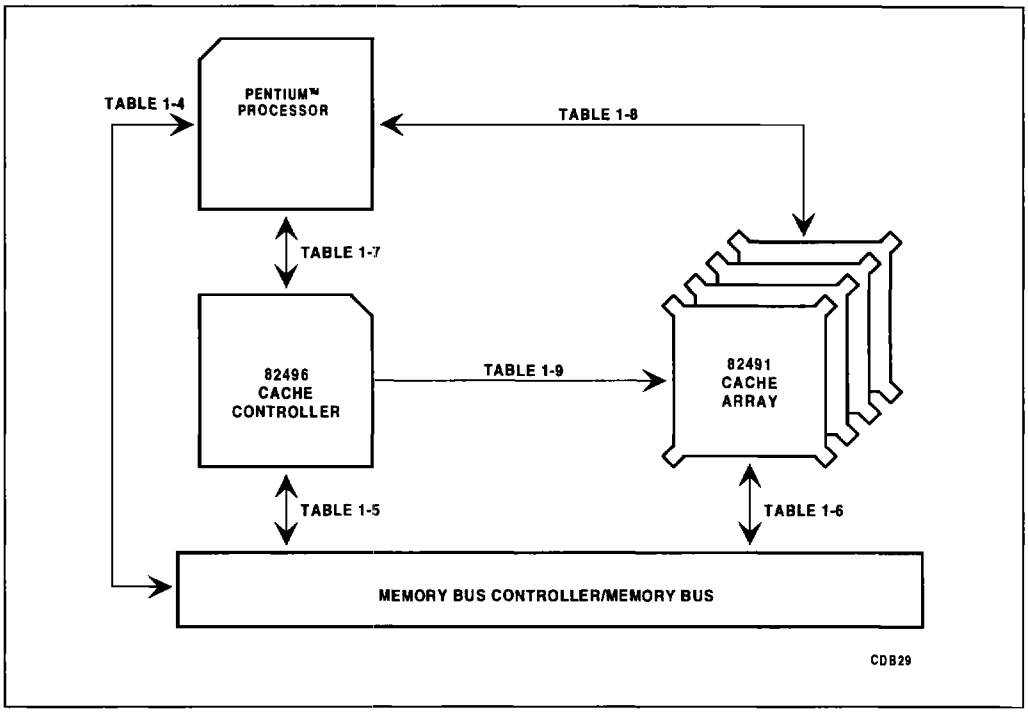

Figure 1-7. Brief Pin Description Table Cross Reference

In the following tables, a signal name in brackets "[ ]" represents a configuration input signal sampled at RESET, and a signal name in parenthesis "( )" represents a strobed mode signal.

Table 1-4. Pentium™ Processor/MBC Interface Signals

APCHK#	CLK	HOLD	INTR	PEN#	SMIACT#
BP[3:2],PM/BP[1:0]	FERR#	IBT	IU	PRDY	TCK
BRDY#	FLUSH#	IERR#	IV	R/S#	TDI
BREQ	HLDA	IGNNE#	NMI	RESET	TDO
BUSCHK#	HIT#	INIT	PCHK#	SMI#	TMS
					TRST#

Table 1-5. 82496 Cache Controller/MBC Interface Signals

APERR#	CM/IO#	KLOCK#	MRO#	SNPINV
APIC#	CNA# [CFG0]	KWEND# [CFG2]	MTHIT#	SNPNCA
BGT# [CLDRV]	CPCD	MALE [WWOR#]	MWB/WT#	SNPSTB#
BLE#	CPWT	MAOE#	NENE#	SWEND# [CFG1]
BRDY#	CRDY# [SLFTST#]	MAP	PALLC#	SYNC# [MALDRV]
CADS#	CSCYC	MAPERR#	RDYSRC	TCK
CAHOLD	CW/R#	MBALE [HIGHZ#]	RESET	TDI
CCACHE#	CWAY	MBAOE#	SMLN#	TDO
CD/C#	DRCTM#	MBT[3:0]	SNPADS#	TMS
CDTS#	FLUSH#	MCACHE#	SNPBSY#	TRST#
CFG[2:0]	FSIOUT#	MHITM#	SNPCLK [SNPMD]	
CLK	IPERR#	MKEN#	SNPCYC#	
MCFA[6:0], MSET[10:0], MTAG[11:0]				

Table 1-6. 82491 Cache SRAM/MBC Interface Signals

BRDY#	MBRDY# (MISTB)	MEOC#	MZBT# [MX4/8#]	TDO
CLK	MCLK [MSTBM]	MFRZ# [MDLDRV]	RESET	TMS
CRDY#	MDATA[7:0]	MOCLK (MOSTB)	TCK	
MBE# [PAR#]	MDOE#	MSEL# [MTR4/8#]	TDI	

Table 1-7. Pentium™ Processor/82496 Cache Controller Interface Signals

ADSC#/ADS#	BRDYC#/BRDYC1#	EADS#	KEN#	PCD
AHOLD	BT[3:0]	EWBE#	LOCK#	PWT
AP	CACHE#	HITM#	M/IO#	SCYC
BOFF#	D/C#	INV	NA#	W/R#
A[31:3]/CFA[6:0], SET[10:0], TAG[11:0]				WB/WT#

Table 1-8. Pentium™ Processor/82491 Cache SRAM Interface Signals

A[17:3]/A[15:1]	ADS#	BE[7:0]#/BE#	D[63:0]/CDATA[7:0]
HITM#	W/R#	BE[7:0]#/CDATA[7:4][1-1]	DP[3:0]/CDATA[3:0][1-1]

1-1 82491 Cache SRAMs configured as parity devices.

Table 1-9. 82496 Cache Controller/82491 Cache SRAM Interface Signals

BLAST#	BRDYC2#/BRDYC#	MCYC#	WBTYP [LR0]
BLEC#	BUS#	WAY	WBWE# [LR1]
BOFF#	MAWEA#	WBA [SEC2#]	WRARR#

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions

Symbol	Type	Part	Name and Function
A[15:0] A[31:3]	I I/O	P CC	Pentium™ processor **Address** pins. 82491 Cache SRAM **Address** inputs. As outputs, the CPU address lines, along with the byte enables, define the physical area of memory or I/O accessed. The 82496 Cache Controller drives the inquire address to the Pentium processor on A[31:5]. Note that 82491 Cache SRAM address pin A0 is always connected to VSS.
A20M#	I	P	When the **Address bit 20 Mask** pin is asserted, the Pentium processor emulates the address wraparound at one Mbyte which occurs on the 8086. When A20M# is asserted, the Pentium processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
ADS# 	I I O	CC CS P	**Address Strobe** signal from the Pentium processor to the 82491 Cache SRAMs. ADS# indicates the start of a new, valid CPU bus cycle and is functionally identical to ADSC#. The 82496 Cache Controller ADS# input is connected to the Pentium processor ADSC# output.
ADSC#	O	P	**Address Strobe** signal from the Pentium processor to the 82496 Cache Controller ADS# input. ADSC# indicates the start of a CPU cycle and is functionally identical to ADS#.
AHOLD	O I	CC P	In response to the assertion of **Address Hold**, the Pentium processor will stop driving the address lines (A[31:3]), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles. AHOLD is driven by the 82496 Cache Controller to the Pentium processor AHOLD input during back-invalidation cycles and inquire cycles.
AP	I/O I/O	CC P	**Address Parity** is driven by the Pentium processor with even parity information on all Pentium processor generated cycles in the same clock that the address is driven. Even parity is driven back to the Pentium processor during inquire cycles on this pin in the same clock as EADS# by the 82496 Cache Controller to ensure that the correct parity check status is indicated by the Pentium processor.
APCHK#	O	P	This is the **address parity check status** pin. APCHK# is asserted two clocks after EADS# is sampled active if the Pentium processor has detected a parity error on the address bus during 82496 Cache Controller inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
APERR#	O	CC	The **Address Parity Error** output indicates that the 82496 Cache Controller has detected a CPU bus address parity error.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
APIC#	O	CC	The **Advanced Programmable Interrupt Controller Address Decoding** output indicates, when active, that the current address is an APIC address (ie. 0 FE E0 00 00 to 0 FE E0 03 FF Hex).
BE# BE[7:0]#	I O	CS P	The **Byte Enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A[31:3]). One Pentium processor byte enable output, BE[7:0]#, is connected to either one or two (cache size dependent) 82491 Cache SRAM BE# input. When a 82491 Cache SRAM is configured to be a parity device, the CPU byte enables are connected to the 82491 Cache SRAM CDATA[7:4] pins (BE[7:4]# to one parity 82491 Cache SRAM, and BE[3:0]# to the other).
BGT#	I	CC	**Bus Guaranteed Transfer** is generated by the Memory Bus Controller (MBC) to indicate that it is committed to completing a given memory bus cycle. Until BGT# is active, the 82496 Cache Controller owns the cycle and may abort the cycle upon an intervening bus snoop. Once BGT# is asserted, the MBC owns the cycle, freeing the 82496 Cache Controller for other operations. BGT# shares a pin with the Configuration signal CLDRV.
BLAST#	O I	CC CS	The **Burst Last** signal indicates the end of a burst cycle when it comes together with BRDY# or BRDYC#.
BLE#	O	CC	The 82496 Cache Controller asserts **Byte Latch Enable** to latch PCD, PWT, BE0#-BE7#, CACHE# and SCYC from the CPU into an external 377-type latch. This signal is not necessary with the 82496 Cache Controller /82491 Cache SRAM secondary cache since those signals are latched into the 82496 Cache Controller and 82491 Cache SRAM devices.
BLEC#	O I	CC CS	The 82496 Cache Controller asserts **Byte Latch Enable** to the 82491 Cache SRAM to latch the Pentium processor byte enables (BE[7:0]#). If active (LOW), the 82491 Cache SRAM will latch new byte enable data upon the rising edge of CLK. If inactive (HIGH), the latch will be closed.
BOFF#	O I I	CC CS P	The **Back-Off** Pentium processor signal is driven by the 82496 Cache Controller to resolve In response to BOFF#, the Pentium processor and 82491 Cache SRAM (if driving CDATA lines to the Pentium processor) will float their buses on the next CLK. The CPU remains in bus hold until BOFF# is negated, at which time the Pentium processor restarts the aborted bus cycles.
BP[3:2] PM/BP[1:0]	O O	P P	The **Breakpoint** pins correspond to the debug registers DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **Performance Monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of reset configured for performance monitoring (for more information, see Appendix A).

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
BRDY#	I I I	CC CS P	The **Burst Ready** input indicates that the 82496 Cache Controller has presented valid data on the data pins in response to a read or that the 82496 Cache Controller has accepted the Pentium processor data in response to a write request. BRDY# is generated by the Memory Bus Controller (MBC).
BRDYC#	I I	CS P	**Burst Ready Cache** is an input to the Pentium processor from the cache used for unlocked cache hit cycles and posted writes. The Pentium processor BRDYC# input is connected to the 82496 Cache Controller BRDYC1# output. The 82491 Cache SRAM BRDYC# input is connected to the 82496 Cache Controller BRDYC2# output and is used for tracking these hit and posted write cycles.
BRDYC1#	O	CC	**Burst Ready Cache 1** is output by the 82496 Cache Controller to the Pentium processor BRDYC# input during cache hit and posted cycles.
BRDYC2#	O	CC	**Burst Ready Cache 2** is output by the 82496 Cache Controller to the 82491 Cache SRAM BRDYC# input during cache hit and posted cycles.
BREQ	O	P	The **Bus Request** output indicates to the external system that the Pentium processor has internally generated a bus request. This signal is always driven whether or not the Pentium processor is driving its bus.
BT[3:0]	I O	CC P	The **Branch Trace Outputs** provide bits 2:0 of the branch target linear address (BT[2:0]) and the default operand size (BT3) during a branch trace message special cycle.
BUS#	O I	CC CS	The **Bus/Array Select** output of the 82496 Cache Controller multiplexes either the memory bus path or array path to the CPU bus of the 82491 Cache SRAM.
BUSCHK#	I	P	The **Bus Check** input pin allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium processor will vector to the machine check exception. For proper Pentium processor /82496 Cache Controller /82491 Cache SRAM operation, BUSCHK# must be asserted as detailed in Chapter 4.
BUSCHK#	I	P	The **Bus Check** input pin allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium processor will vector to the machine check exception. For proper Pentium processor /82496 Cache Controller /82491 Cache SRAM operation, BUSCHK# must be asserted as detailed in Chapter 4.
CACHE#	I O	CC P	For Pentium processor-initiated cycles, the **Cache** signal indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
CADS#	O	CC	**Cache Address Strobe** is generated by the 82496 Cache Controller to request that the Memory Bus Controller execute a memory bus cycle. When active, CADS# indicates that the memory bus address (if MAOE#, MBAOE#, MALE, and MBALE are active), control, and attribute signals are valid.
CAHOLD	O	CC	82496 Cache Controller **CAHOLD** is generated by the 82496 Cache Controller to track the CPU AHOLD signal. This is useful to the MBC during warm reset (INIT), Locked sequences, and flush or writeback special cycles. CAHOLD also provides information relevant to 82496 Cache Controller built-in self-test (BIST).
CCACHE#	O	CC	82496 Cache Controller **Internal Caching Indication** is a latched version of the Pentium processor CACHE# attribute. CCACHE# indicates to the MBC how many BRDY#s it must return to the Pentium processor. If CCACHE# is inactive (HIGH), the MBC must return one BRDY#. If CCACHE# is active (LOW), the MBC must return four BRDY#s for cycles cacheable in the Pentium processor, and one for cycles not cacheable in the Pentium processor (depends upon the values of MKEN#, MRO#, and CD/C#). CCACHE# is valid with CADS# and SNPADS#.
CD/C#	O	CC	**Cache Data/Control** is driven by the 82496 Cache Controller to indicate whether a requested memory bus cycle needs data or code.
CDATA[7:0]	I/O	CS	**Cache Data** I/O pins are the 8 bits comprising the I/O data bus interface between each 82491 Cache SRAM and the Pentium processor data bus. When an 82491 Cache SRAM is configured to be a parity device, bits 3-0 are used for parity (connected to CPU DP[7:4] or DP[3:0]) and bits 7-4 are used for bit enables (connected to CPU BE[7:4]# or BE[3:0]#). For cache configurations which only require 4 CDATA pins, bits 3-0 are used.
CDTS#	O	CC	**Cache Data Strobe** indicates to the memory bus controller that the data path is ready. In read cycles, CDTS# indicates that the memory bus controller can generate the first BRDY# in the next CLK. For write cycles, CDTS# indicates that data is available on the memory bus in the next CLK. CDTS# permits independent address and data strobes for CADS# and SNPADS# cycles.
CFA[6:0] SET[10:0] TAG[11:0]	I/O I/O I/O	CC CC CC	**Configurable Address** pins of the 82496 Cache Controller are multiplexed to the Pentium processor address pins according to the 82496 Cache Controller configuration.
CFG[2:0]	I	CC	During the falling edge of RESET, **Configuration Pins 0,1, and 2** are used to configure the 82496 Cache Controller in any of five modes that determine 82496 Cache Controller /Pentium processor line ratio, cache tag size (4K-Tags or 8K-Tags) and lines per sector. CFG2 shares a pin with the 82496 Cache Controller input signal KWEND#. CFG1 shares a pin with the 82496 Cache Controller input signal SWEND#. CFG0 shares a pin with the 82496 Cache Controller input signal CNA#.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
CLDRV	I	CC	During RESET, the **Cache Low Drive Configuration** signal determines the driving strength of the connections between the 82496 Cache Controller and 82491 Cache SRAM components. CLDRV shares a pin with the 82496 Cache Controller input signal BGT#.
CLK	I I I	CC CS P	The **Clock** input provides the fundamental timing for the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM components. Its frequency is the internal operating frequency of the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, and TRST# are specified with respect to the rising edge of CLK. The clock inputs must be provided with minimal skew between devices.
CM/IO#	O	CC	**Cache Memory/IO** is driven by the 82496 Cache Controller to indicate whether a requested memory bus cycle is for memory or for I/O.
CNA#	I	CC	**Cache Next Address Enable** is driven by the memory bus controller to dynamically pipeline the 82496 Cache Controller cycles. If a cycle is pending and CNA# is given, a new CADS# is driven with the new cycle information. CNA# shares a pin with the Configuration signal CFG0.
CPCD	O	CC	82496 Cache Controller **Page Cache Disable** is a latched version of the Pentium processor PCD attribute to give the memory bus controller direct access. CPCD is valid with CADS# and SNPADS#.
CPWT	O	CC	82496 Cache Controller **Page Writethrough** is a latched version of the Pentium processor PWT attribute to give the memory bus controller direct access. CPWT is valid with CADS# and SNPADS#.
CRDY#	I I	CC CS	**Cache Memory Bus Ready** is generated by the memory bus controller to indicate to the 82496 Cache Controller and 82491 Cache SRAM that a memory bus cycle has completed and the devices should make resources available for the next cycle. The 82496 Cache Controller CRDY# input signal shares a pin with the Configuration signal SLFTST#.
CRDY#	I I	CC CS	**Cache Memory Bus Ready** is generated by the memory bus controller to indicate to the 82496 Cache Controller and 82491 Cache SRAM that a memory bus cycle has completed and the devices should make resources available for the next cycle. The 82496 Cache Controller CRDY# input signal shares a pin with the Configuration signal SLFTST#.
CCCYC	O	CC	82496 Cache Controller **Split Cycle Indication** is a latched version of the Pentium processor SCYC attribute to give the memory bus controller direct access. CSCYC is active only for locked cycles with SCYC active, and inactive for all others. CSCYC is valid with CADS# and SNPADS#.
CW/R#	O	CC	**Cache Write/Read** is driven by the 82496 Cache Controller to indicate a requested memory bus cycle requires a read or a write.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
CWAY	O	CC	**Cache Way** is driven by the 82496 Cache Controller to indicate to the memory bus controller in which cache "way" the line will be loaded during line fills or driven from during writebacks. CWAY is valid with CADS# and is used to facilitate external tracking tags.
D/C#	I O	CC P	The **Data/Code** signal is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D[63:0]	I/O	P	These are the 64 **Data Lines** for the processor. Lines D[7:0] define the least significant byte of the data bus; lines D[63:56] define the most significant byte of the data bus. During reads, the CPU samples the data bus when BRDY# is returned. The Pentium processor Data Bus pins are distributed to each 82491 Cache SRAM .
DP[7:0]	I/O	P	These are the **Data Parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor . DP7 applies to D[63:56], DP0 applies to D[7:0]. The Pentium processor Data Parity Bus pins are distributed to each 82491 Cache SRAM configured to be a parity device. The CPU data parity pins are connected to the 82491 Cache SRAM CDATA[3:0] pins.
DRCTM#	I	CC	Memory Bus **Direct to [M] State** allows the memory bus to inform the 82496 Cache Controller of a request to skip the [E] state and move a line directly to the [M] state. DRCTM# allows the chip set to support read-for-ownership and cache-to-cache transfers (without main memory update), and is sampled when SWEND# is asserted.
EADS#	O I	CC P	The **External Address Strobe** is driven by the 82496 Cache Controller during back-invalidations or inquire cycles to maintain inclusion and indicates that a valid external address has been driven onto the Pentium processor address pins to be used for an inquire cycle.
EWBE#	O I	CC P	The Pentium processor **External Writeback Buffer Empty** input is driven by the 82496 Cache Controller for use in Strong Write Ordering mode. EWBE#, when inactive (HIGH), indicates that a writethrough cycle is posted in the 82496 Cache Controller /82491 Cache SRAM cache. When the Pentium processor generates a write, and EWBE# is sampled inactive, the Pentium processor will hold off all subsequent writes to all E or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# going active when the posted write receives BGT# from the MBC. When the 82496 Cache Controller is configured in weak write ordering mode, EWBE# will always be driven active (low).
FERR#	O	P	The **Floating-Point Error** pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS type floating-point error reporting.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
FLUSH#	I I	CC P	When asserted to the Pentium processor, the **Cache Flush** signal forces the CPU to writeback all modified lines in the data cache and invalidate its internal caches. A flush acknowledge special cycle will be generated by the Pentium processor indicating completion of the invalidation and writeback. When asserted to the 82496 Cache Controller, **FLUSH#** causes the 82496 Cache Controller to execute a writeback to main memory of any modified cache lines and then invalidate all 82496 Cache Controller tag locations. FLUSH# also causes the 82496 Cache Controller to inquire the CPU and writeback all Pentium processor modified lines in the data cache and invalidate all cache lines. Note: For proper Pentium processor /82496 Cache Controller operation, FLUSH# must be HIGH at the falling edge of RESET.
FRCMC#	I	P	The **Functional Redundancy Checking Master/Checker** mode input is used to determine whether the Pentium processor is configured in master mode or checker mode. When using the 82496 Cache Controller /82491 Cache SRAM secondary cache, the Pentium processor must be configured as a Master Device (i.e., FRCMC#=1).
FSIOUT#	O	CC	**Flush/Sync/Initialization Output** indicates the start and end of Flush, Sync and Initialization operations.
HIGHZ#	I	CC	If active along with SLFTST#, the **High Impedance Output Configuration** signal causes the 82496 Cache Controller to float all output pins. HIGHZ# shares a pin with the 82496 Cache Controller input signal MBALE.
HIT#	O	P	The **Hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the Pentium processor data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted by the processor. If the inquire cycle misses Pentium processor cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles. This signal is not used by the 82496 Cache Controller cache controller, but may be accessed by the MBC.
HITM#	I I O	CC CS P	The **Hit to a Modified Line** signal is driven by the Pentium processor to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
HLDA	O	P	The **Bus Hold Acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the Pentium processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the Pentium processor will resume driving the bus. If the Pentium processor has a bus cycle pending, it will be driven in the same clock that HLDA is deasserted.
HOLD	I	P	In response to the **Bus Hold Request**, the Pentium processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium processor will maintain its bus in this state until HOLD is deasserted. HOLD is not recognized during LOCK cycles. The Pentium processor will recognize HOLD during reset.
IBT	O	P	The **Instruction Branch Taken** pin is driven active (high) for one clock to indicate that a branch was taken. This output is always driven by the Pentium processor.
IERR#	O	P	The Pentium processor **Internal Error** pin is used to indicate two types of errors, internal parity errors and functional redundancy errors. If a parity error occurs on a read from an internal array, the Pentium processor will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	P	This is the **Ignore Numeric Error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium processor will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, or FSTCW, the Pentium processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is zero, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1) and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, or FSTCW, the Pentium processor will stop execution and wait for an external interrupt.
INIT	I	P	The Pentium processor **Initialization** input pin forces the Pentium processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, model specific registers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power-up. If INIT is sampled high when RESET transitions from high to low the Pentium processor will perform built-in self test prior to the start of program execution.
INTR	I	P	An active **Maskable Interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
INV	O I	CC P	The Pentium processor **Invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
IPERR#	O	CC	**Internal Parity Error** is driven active for TAGRAM parity errors and for internal address path parity errors.
IU	O	P	The **U-Pipe Instruction Complete** signal is driven active (high) for 1 clock to indicate that an instruction in the u-pipeline has completed execution. This pin is always driven by the Pentium processor.
IV	O	P	The **V-Pipe Instruction Complete** signal is driven active (high) for one clock to indicate that an instruction in the v-pipeline has completed execution. This pin is always driven by the Pentium processor.
KEN#	O I	CC P	The **Cache Enable** pin is used to determine whether the current cycle is cacheable by the CPU or not and is, consequently, used to determine cycle length. When the Pentium processor generates a cycle that can be cached (CACHE# asserted) and KEN# is returned active by the 82496 Cache Controller, the cycle will be transformed into a burst line fill cycle.
KLOCK#	O	CC	82496 Cache Controller **Cache LOCK#** is driven by the 82496 Cache Controller and indicates to the memory bus controller that a request to execute atomic read-modify-write sequences is present. KLOCK# tracks the LOCK# signal of the Pentium processor.
KWEND#	I	CC	**Cacheability Window End** is generated by the MBC to indicate to the 82496 Cache Controller that the Cacheability Window (the period during which cacheability is determined) has expired. When KWEND# is asserted, the 82496 Cache Controller latches the memory cacheability signal (MKEN#) and the Memory Read-Only Signal (MRO#), and makes determinations based on the cacheability attributes (e.g., whether a line is cacheable, is read-only, requires a replacement, or requires an allocation). KWEND# shares a pin with the Configuration signal CFG2.
LOCK#	I O	CC P	The **Bus Lock** pin indicates that the current bus cycle is locked. The Pentium processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back to back locked cycles. The LOCK# pin is driven to the 82496 Cache Controller which, in turn, drives the memory bus KLOCK# output.
LR[1:0]	O I	CC CS	The **Line Ratio 1 and 0 Optimized Interface Configuration** signals are driven by the 82496 Cache Controller to the 82491 Cache SRAM at RESET to pass along line ratio information. LR1 shares pins with the 82496 Cache Controller and 82491 Cache SRAM WBWE# signals. LR0 shares pins with the 82496 Cache Controller and 82491 Cache SRAM WBTYP signals.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
M/IO#	I O	CC P	The **Memory/Input-Output** signal is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
MALDRV	I	CC	During the falling edge of RESET, the 82496 Cache Controller **Memory Address Bus Low Drive Configuration** input is sampled to determine the 82496 Cache Controller's memory address bus driving strength. MALDRV shares a pin with the 82496 Cache Controller input signal SYNC#.
MALE	I	CC	**Memory Bus, Address Latch Enable** is generated by the memory bus controller to control transparent address latches (resembling 373-series TTL logic) within the 82496 Cache Controller. CADS# generates a new address at the input of the internal address latch. If MALE and MAOE# are both active, the address flows to the memory bus. When MALE becomes inactive (low), the address is latched. MALE shares a pin with the Configuration signal WWOR#.
MAOE#	I	CC	**Memory Bus Address Output Enable** is generated by the memory bus controller to control the output buffers of the 82496 Cache Controller's memory bus address latches. If MAOE# is active (low), the 82496 Cache Controller drives the memory bus address lines. If MAOE# is inactive (high), the 82496 Cache Controller's address inputs are driven to the hi-z state. Snoops are enabled only while MAOE# is inactive.
MAP	I/O	CC	**Memory Address Parity** is an input when MAOE#=1 (Snoop cycle), and indicates the address parity of the line address bits. **MAP** is an Output when MAOE#=0 (82496 Cache Controller initiated cycle), and indicates the address parity of the line address bits.
MAPERR#	O	CC	**Memory Address Parity Error** is driven active during 82496 Cache Controller snoop cycles whenever there is a memory address bus parity error.
MAWEA#	O I	CC CS	The 82496 Cache Controller asserts **Memory Bus Array Write Enable or Allocation** signal to the 82491 Cache SRAM to indicate that the data in the memory buffers should be written to the array, or that an allocation should occur.
MBALE	I	CC	82496 Cache Controller **Memory Bus Sub-Line Address Latch Enable** functions as MALE but controls only the 82496 Cache Controller sub-line addresses. MBALE is generated by the memory bus controller to control transparent address latches (resembling 373-series TTL logic) within the 82496 Cache Controller. CADS# generates a new address at the internal address latch input. If MBALE and MBAOE# are both active, the sub-line address flows to the memory bus. If MBALE becomes inactive (LOW), the sub-line address is latched. A separate subline control input is provided because the 82496 Cache Controller only provides the starting sub-line address. MBALE shares a pin with the 82496 Cache Controller Configuration signal HIGHZ#.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
MBAOE#	I	CC	82496 Cache Controller **Memory Bus Sub-Line Address Output Enable** functions like MAOE# but only controls the 82496 Cache Controller sub-line addresses. If MBAOE# is active (low), the 82496 Cache Controller drives the sub-line portion of the address onto the memory bus. Otherwise, the 82496 Cache Controller's sub-line address is driven to the hi-z state. MBAOE# is also sampled during snoop cycles. If MBAOE# is sampled inactive in conjunction with SNPSTB#, snoop writeback cycles begin at the sub-line address provided. If MBAOE# is sampled active with SNPSTB#, snoop writeback cycles begin at sub-line address 0. A separate sub-line control input is provided because the 82496 Cache Controller only provides the starting sub-line address.
MBE#	O	CS	The 82491 Cache SRAM **Memory Byte Enable** output is a latched version of the Pentium processor byte enable outputs, BE[7:0]#. The memory cycle byte enables (MBE#) are always valid either with or one CLK after CADS#. MBE# shares a pin with the 82491 Cache SRAM Configuration pin PAR#.
MBRDY#	I	CS	In clocked memory bus mode, **Memory Bus Ready** is used to clock data into and out of the 82491 Cache SRAM . When active (LOW), MBRDY# indicates that the 82491 Cache SRAM will increment the burst counter and output or accept the next data upon the rising edge of MCLK (or MOCLK for writes, if applicable). MBRDY# is qualified by MSEL#. MBRDY# shares a pin with the 82491 Cache SRAM input signal MISTB.
MBT[3:0]	O	CC	The Memory **Branch Trace Address** signals echo the Pentium processor BT[3:0] bits which provide bits 2:0 of the branch target linear address (MBT[2:0]) and the default operand size (MBT3) during a branch trace message special cycle. MBT[3:0] must be pulled low with an external resistor for proper cache operation.
MCACHE#	O	CC	82496 Cache Controller **Internal Cacheability** is driven during read cycles to indicate whether the current cycle is potentially cacheable in the 82496 Cache Controller /82491 Cache SRAM. During write operations, MCACHE# is only active for writeback cycles. MCACHE# is inactive during I/O, special and locked cycles.
MCFA[6:0] MSET[10:0] MTAG[11:0]	I/O I/O I/O	CC CC CC	**Memory Bus Configurable address lines** **Memory bus SET number** **Memory bus TAG bits** The **Memory Address** lines are used along with the 8 MBE#s to define the areas of memory or I/O to be accessed. They are driven during normal memory bus cycles and are inputs during snoop operations.
MCLK	I	CS	**Memory Bus Clock** is the memory bus clock input to the 82491 Cache SRAM while in clocked memory bus mode. Here, memory bus signals and data are sampled on the rising edge of MCLK. During clocked memory bus writes, data is driven with respect to MCLK or MOCLK, depending on the configuration. MCLK inputs to each 82491 Cache SRAM must be within proper skew specifications. MCLK shares a pin with the Configuration signal MSTBM.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
MCYC#	O I	CC CS	The 82496 Cache Controller asserts **Memory Bus Cycle** to the 82491 Cache SRAM to indicate that the current cycle will use the memory buffers.
MDATA[7:0]	I/O	CS	The **Memory Data Pins** are each 82491 Cache SRAM's data I/O pins. Together with other 82491 Cache SRAM components, they form a 64- or 128-bit wide memory bus. In clocked memory bus mode, data is sampled or driven on MDATA[7:0] with the rising edge of MCLK when MBRDY# is active. MOCLK is used as a latch enable to hold write data on the MDATA[7:0] pins. In strobed memory bus mode, data is sampled or driven on MDATA[7:0] with MISTB, MOSTB, or MEOC# edges. For cache configurations which only require 4 MDATA pins, bits 3-0 are used.
MDLDRV	I	CS	During the falling edge of RESET, the **Memory Data Bus Low Drive Configuration** signal is sampled to indicate the memory data bus driver strength of the 82491 Cache SRAM, which offers normal (MDLDRV=HIGH) and high drive (MDLDRV=LOW) capability buffers. MDLDRV shares a pin with the 82491 Cache SRAM input signal MFRZ#.
MDOE#	I	CS	**Memory Data Output Enable** controls when the 82491 Cache SRAM drives the data onto the memory bus. When MDOE# is inactive (high), the MDATA pins are tri-stated. When MDOE# is active (low), the MDATA pins drive data. Because it is unrelated to CLK and MCLK, MDOE# functions the same during strobed and clocked memory bus operations.
MEOC#	I	CS	**Memory End of Cycle** ends the current cycle. Because it is synchronous to the memory bus clock and asynchronous to the CPU CLK, MEOC# can end a memory bus cycle and begin a new cycle without waiting for Pentium processor CLK synchronization. MEOC# also causes data to be latched or driven and resets the memory burst counter. In clocked memory bus mode, MEOC# is sampled on the rising edge of MCLK. In strobed mode, actions occur on MEOC# falling edge.
MFRZ#	I	CS	**Memory Freeze** is used during write cycles that could cause allocation cycles. When MFRZ# is sampled active (low) with MEOC#, write data is latched within the 82491 Cache SRAM. The subsequent allocation will not overwrite latched data, thereby avoiding the memory write on the memory bus. Because memory is not updated, the allocated line must be cached in the [M] state. MFRZ# shares a pin with the Configuration signal MDLDRV.
MHITM#	O	CC	**Memory Bus Hit to Modified Line** is driven during snoop cycles to indicate whether snooping addresses hit a modified cache line within the 82496 Cache Controller /82491 Cache SRAM. When snoop hits to [M] occur, the 82496 Cache Controller automatically schedules the writeback of modified lines. MHITM# is valid in the CLK following SNPCYC#. If active, MHITM# remains active until the CLK of CRDY# of the snoop writeback.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
MISTB	I	CS	In strobed memory bus mode, **Memory Input Strobe** is the 82491 Cache SRAM's input data strobe. On each edge of MISTB, the chip set latches data and increments the burst counter. MISTB is qualified by MSEL#. MISTB shares a pin with the 82491 Cache SRAM input signal MBRDY#.
MKEN#	I	CC	**Memory Bus Cacheability** is driven by the memory bus controller to indicate to the 82496 Cache Controller whether the current memory bus cycle is cacheable to the 82496 Cache Controller /82491 Cache SRAM cache. MKEN# is sampled when KWEND# is asserted.
MOCLK	I	CS	In clocked memory bus mode, **Memory Output Clock** controls a transparent latch at the 82491 Cache SRAM's data outputs. MDATA hold time may be increased through a clock input skewed from MCLK. MOCLK shares a pin with the 82491 Cache SRAM input signal MOSTB.
MOSTB	I	CS	In strobed memory bus mode, each edge of the **Memory Output Strobe** signal outputs new data onto the memory bus. MOSTB is qualified by MSEL#. MOSTB shares a pin with the 82491 Cache SRAM input signal MOCLK.
MRO#	I	CC	**Memory Bus Read-Only** indicates to the 82496 Cache Controller that an accessed line is READ-ONLY. For the Pentium processor, READ-ONLY code lines are cacheable in the first level cache; Read-Only data lines are not cacheable in the first level cache. READ-ONLY lines are cached in the 82496 Cache Controller in the [S] state if both MKEN# and MRO# are sampled active during KWEND#. MRO# is sampled with KWEND# assertion. Subsequent writes to Read-Only lines are not updated but instead posted to the memory system.
MSEL#	I	CS	**Memory Select** is a chip select input which provides three functions. (1) In clocked mode, MSEL# qualifies the MBRDY# 82491 Cache SRAM input. In strobed mode, MSEL# qualifies the MISTB and MOSTB inputs. (2) If MSEL# is active with MEOC#, MZBT# is sampled for the next cycle. (3) MSEL# going inactive causes the 82491 Cache SRAM 's memory burst counter to reset. Note that in clocked mode, MZBT# is sampled on every MCLK rising edge with MSEL# inactive. MSEL# shares a pin with the Configuration signal MTR4/8#.
MSET[10:0]	I/O	CC	See MCFA[6:0].
MSTBM	I	CS	The **Memory Bus Strobed Mode Configuration** signal determines whether the 82491 Cache SRAM will operate in the strobed memory bus mode or in clocked memory bus mode. If a clock is detected on this pin any time after reset, the 82491 Cache SRAM will operate in clocked mode. If this input remains stable at VSS or VCC, the 82491 Cache SRAM will operate in strobed mode. MSTBM shares a pin with the 82491 Cache SRAM input signal MCLK.
MTAG[11:0]	I/O	CC	See MCFA[6:0].

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
MTHIT#	O	CC	**Memory Bus Tag Hit** is driven by the 82496 Cache Controller during snoop cycles to indicate whether a snooping address hits an exclusive, shared, or modified cache line. MTHIT# is valid in the CLK following SNPCYC# and remains valid until the CLK of the next SNPCYC#.
MTR4/8#	I	CS	The **Memory Transfer Configuration** signal is sampled at the falling edge of RESET and determines the number of transfers needed on the memory bus for each cache line. If MTR4/8# is high, there are four transfers for each cache line; If MTR4/8# is low, there are eight transfers. MTR4/8# shares a pin with the 82491 Cache SRAM input signal MSEL#.
MWB/WT#	I	CC	**Memory Bus Write Policy** allows the memory bus to dynamically indicate to the 82496 Cache Controller whether the write policy is writethrough or writeback. MWB/WT# is sampled when SWEND# becomes active. If MWB/WT# is sampled low, the tag state changes to shared (used, for example, when the line is detected in another cache). If MWB/WT# is sampled high, the tag state can change to an exclusive state.
MX4/8#	I	CS	On the falling edge of RESET, the **Memory I/O Bits Configuration** signal is sampled to determine the number of I/O pins to be used for the memory bus. If MX4/8# is HIGH, four I/O pins are used. If MX4/8# is LOW, eight I/O pins are used. MX4/8# shares a pin with the 82491 Cache SRAM input signal MZBT#.
MZBT#	I	CS	When sampled active with MSEL# inactive or MEOC# active, **Memory Zero Based Transfer** indicates that burst location zero of the memory bus cycle should be the starting sub-line address independent of the sub-line address requested by the Pentium processor. MZBT# shares a pin with the Configuration signal MX4/8#.
NA#	O I	CC P	An active **Next Address** signal indicates that the 82496 Cache Controller is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium processor will drive out a pending cycle two clocks after NA# is asserted. The Pentium processor supports up to 2 outstanding bus cycles.
NENE#	O	CC	**Next Near** allows the memory bus controller (MBC) to take advantage of paged or static column DRAMs by indicating whether a requested memory address is "near" the previously generated address (i.e., within the same 2K-Byte DRAM page). NENE# is valid with CADS# and undefined during SNPADS#.
NMI	I	P	The **Non-Maskable Interrupt** request signal indicates that an external non-maskable interrupt has been generated.
PALLC#	O	CC	**Potential Allocate** indicates to the memory bus controller that the current write cycle could potentially allocate a cache line. PALLC# is active for write miss cycles in which LOCK#, PCD and PWT are inactive.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
PAR#	I	CS	The **Parity Configuration** signal, when sampled active during RESET, causes the 82491 Cache SRAM to be configured solely as a parity device. For 82491 Cache SRAM s configured as parity devices, PAR# remains tri-stated following Reset. PAR# shares a pin with the 82491 Cache SRAM output signal MBE#.
PCD	I O	CC P	The **Page Cache Disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	P	The **Parity Check** signal indicates the result of a parity check on a data read. It is driven by the Pentium processor with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	P	The **Parity Enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the Pentium processor will vector to the machine check exception before the beginning of the next instruction.
PRDY	O	P	The PRDY output pin indicates that the processor has stopped normal execution in response to the R/S# pin going inactive or Probe Mode being entered (see Appendix A for more information regarding Probe Mode). This pin is provided for use with the Intel debug port described in the *Pentium™ Processor Data Book*.
PWT	I O	CC P	The **Page Writethrough** pin reflects the state of the PWT bit in CR3, the Page Directory Entry, or the Page Table Entry. The PWT pin is used to provide an external writeback indication on a page by page basis. PWT active causes the 82496 Cache Controller to put the line in 'S' state in cases of linefill regardless of the value of MWB/WT#. PWT is ignored by the 82496 Cache Controller if the line is in the cache in 'E' or 'M' state.
R/S#	I	P	The R/S# input is an asynchronous, edge sensitive input used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary. This pin is provided for use with the Intel debug port described in the *Pentium™ Processor Data Book*.
RDYSRC	O	CC	**Ready Source** indicates whether the MBC or the 82496 Cache Controller provides BRDY# to the Pentium processor . If RDYSRC is high, the memory bus controller must generate BRDY#. If RDYSRC is low, the 82496 Cache Controller generates BRDY#.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
RESET	I I I	CC CS P	**Reset** forces the Pentium processor to begin execution at a known state. All the Pentium processor internal caches will be invalidated upon the reset. Modified lines in the data cache are not written back. When asserted to the 82496 Cache Controller and 82491 Cache SRAM, the reset signal initiates cache execution at a known state. RESET going inactive causes the state of the configuration input pins to be sampled. **The following 82496 Cache Controller pins are sampled during the falling edge of RESET:** CNA#[CFG0]: CFG0 line of 82496 Cache Controller configuration inputs. SWEND#[CFG1]: CFG1 line of 82496 Cache Controller configuration inputs. KWEND#[CFG2]: CFG2 line of 82496 Cache Controller configuration inputs. BGT#[CLDRV]: Indicates the driving strength of the 82496 Cache Controller /82491 Cache SRAM interface. SYNC#[MALDRV]: Indicates the 82496 Cache Controller's memory address bus driving strength. SNPCLK[SNPMD]: Indicates whether the snoop mode is synchronous, clocked, or strobed. MALE[WWOR#]: Enforces strong or weak write-ordering consistency. CRDY#[SLFTST#]: Invokes 82496 Cache Controller self-test if HIGHZ# high. MBALE[HIGHZ#]: Tristates 82496 Cache Controller outputs if active with SLFTST#. Note: For proper Pentium processor/82496 Cache Controller operation, 82496 Cache Controller FLUSH# must be HIGH at the falling edge of RESET. **The following 82491 Cache SRAM pins are sampled during the falling edge of RESET:** MZBT#[MX4/8#]: Determines whether each 82491 Cache SRAM uses four or eight I/O pins on the memory bus. MSEL#[MTR4/8#]: Determines the number of memory bus transfers needed to fill each cache line — four transfers if HIGH, eight if LOW. MCLK[MSTBM]: Indicates the memory bus configuration — strobed if stable (high or low), clocked if toggling. MFRZ#[MDLDRV]: Indicates the 82491 Cache SRAM 's memory data bus driving strength. MBE# [PAR#]: Configures the 82491 Cache SRAM as a parity storage device. WBA[SEC2#]: Configures the 82491 Cache SRAM to be 2 Lines per Sector. WBTYP[LR0]: Line Ratio information, bit 0. WBWE#[LR1]: Line Ration information, bit 1.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
			The following Pentium processor pins are sampled during the falling edge of RESET: BUSCHK#, BRDYC#, CLRDRV: used to configure I/O buffers. FLUSH#, FRCMC# and INIT: sampled when RESET transitions from high to low to determine if tristate test mode or checker mode will be entered, or if BIST will be run.
SCYC	I O	CC P	The **Split Cycle** signal is asserted during misaligned LOCK transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SEC2#	O I	CC CS	The 82496 Cache Controller drives the **2 lines per sector Optimized Interface Configuration** signal during RESET to the 82491 Cache SRAM to pass along lines/sector information. If active, SEC2# indicates 2 lines per sector. SEC2# shares pins with the 82496 Cache Controller and 82491 Cache SRAM WBA signals.
SET[10:0]	I/O	CC	See CFA[6:0].
SLFTST#	I	CC	If the **82496 Cache Controller Self Test Configuration** signal is sampled LOW (active) during the falling edge of RESET while MBALE is HIGH (active), 82496 Cache Controller self-test is invoked. SLFTST# shares a pin with the 82496 Cache Controller input signal CRDY#.
SMI#	I	P	The **System Management Interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	P	An active **System Management Interrupt Active** signal indicates that the processor is operating in System Management Mode (SMM).
SMLN#	O	CC	**Same Cache Line** indicates to the memory bus controller that the current cycle accesses the same 82496 Cache Controller line as the previous memory (not I/O) cycle. SMLN# is valid together with CADS# and can be used to selectively activate SNPSTB# for other caches. For example, SMLN# can prevent consecutive snoops to the same line.
SNPADS#	O	CC	**Cache Snoop Address Strobe** functions exactly like CADS# but is generated only on snoop writeback cycles. Because snoop writeback cycles must be immediately serviced on the memory bus, the separate address strobe eases memory bus controller (MBC) implementation. When SNPADS# is active, the MBC aborts all pending cycles (ie. those for which BGT# has not been issued; after BGT#, snoop lookups are delayed). The 82496 Cache Controller may re-issue cycles following snoop completion.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
SNPBSY#	O	CC	When active (LOW), **Snoop Busy** indicates that the 82496 Cache Controller will latch the snoop address and attributes, but will delay the snoop lookup. SNPBSY# is activated when a snoop hits a modified line or when back-invalidation is needed for a snoop in progress. The 82496 Cache Controller does not perform snoop lookups until SNPBSY# is deactivated.
SNPCLK	I	CC	**Snoop Clock** provides the 82496 Cache Controller with a snoop clock so the MBC can snoop at its own rate. During clocked mode, SNPSTB#, SNPINV, SNPNCA, MBAOE#, MAOE#, MAP, and all Address lines are sampled by SNPCLK. SNPCLK shares a pin with the Configuration signal SNPMD.
SNPCYC#	O	CC	**Snoop Cycle** indicates when a snoop lookup is occurring within the 82496 Cache Controller TAGRAM. MHITM# and MTHIT# are valid from the clock following SNPCYC#.
SNPINV	I	CC	**Snoop Invalidation** is sampled with SNPSTB# and indicates the state of a cache line following snoop hit cycle. If active, SNPINV forces the line to become invalid.
SNPMD	I	CC	When HIGH during RESET, the **Snoop Mode Configuration** signal indicates strobed snooping mode. If LOW during reset, SNPMD indicates synchronous snooping mode. In clocked snooping mode, SNPMD is connected to the snoop clock source. SNPMD shares a pin with the 82496 Cache Controller input signal SNPCLK.
SNPNCA	I	CC	**Snoop Non Caching Device Access** is sampled with SNPSTB# and indicates to the 82496 Cache Controller whether a bus master is a non caching device (e.g., a DMA controller). SNPNCA helps prevent the 82496 Cache Controller from unnecessarily changing cache line states from exclusive or modified to shared.
SNPSTB#	I	CC	**Snoop Strobe** causes snoop address and parameters to be latched and initiates a snoop. The 82496 Cache Controller supports three latching modes: Clocked, Strobed, and Synchronous latching modes. In clocked mode, address and attribute signals are latched when SNPSTB# becomes active with the rising edge of SNPCLK. In strobed mode, addresses and attributes are latched at the falling edge of SNPSTB#. In synchronous mode, address and attribute signals are latched when SNPSTB# becomes active with the rising edge of CLK.
SWEND#	I	CC	**Snoop Window End** is generated by the memory bus controller to indicate that the Snoop Window has expired. When SWEND# is asserted, the 82496 Cache Controller latches the Write Policy (MWB/WT#) and Direct to Memory Transfer (DRCTM#) attributes. By the end of the window, all devices have snooped the bus master address and generated the snoop results. Once a cycle has received BGT#, the 82496 Cache Controller prevents snooping until it receives SWEND#. The 82496 Cache Controller can then update its tag RAM. SWEND# shares a pin with the Configuration signal CFG1.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
SYNC#	I	CC	The **Synchronize Pentium processor CPU Cache Chip Set** signal synchronizes the 82496 Cache Controller /82491 Cache SRAM tag array with main memory. All modified cache lines in the 82496 Cache Controller /82491 Cache SRAM are written back to main memory. SYNC# differs from FLUSH# in that it doesn't invalidate the 82496 Cache Controller or Pentium processor tag array. All E,I, and S state lines remain in the E,I, and S states. All modified cache lines (M state) cause the 82496 Cache Controller to inquire the CPU (the Pentium processor will writeback 'M' state data to the 82496 Cache Controller /82491 Cache SRAM) and become non-modified (E state) by writing modified data to the memory bus. SYNC# shares a pin with the Configuration signal MALDRV.
TAG[11:0]	I/O	CC	See CFA[6:0].
TCK	I I I	CC CS P	The **Testability Clock** input provides the clocking function for the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM boundary scan in accordance with the JTAG/Boundary Scan interface (IEEE Std 1149.1). It is used to clock state information and data into and out of the Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM during boundary scan.
TDI	I I I	CC CS P	The **Test Data Input** is a serial input pin for the test logic. TAP instructions and data are shifted into the Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM components on the TDI input pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O O O	CC CS P	The **Test Data Output** is a serial output of the test logic. TAP instructions and data are shifted out of the Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM on the TDO pin on the falling edge of TCK when the TAP controller is in the appropriate state.
TMS	I I I	CC CS P	The value of the **Test Mode Select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes for the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM components.
TRST#	I I	CC P	The **Test Reset** pin. When asserted, it allows the TAP controller to be asynchronously initialized.
W/R#	I I O	CC CS P	**Write/Read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WAY	O I	CC CS	The 82496 Cache Controller **Way** indication is used by the 82491 Cache SRAM to properly load and store buffers as well as update the MRU bit.
WB/WT#	O I	CC P	The **WriteBack/WriteThrough** signal allows a Pentium processor data cache line to be defined as writeback or writethrough on a line by line basis. As a result, it determines whether a cache line is initially in the S or E state in the CPU data cache. This signal provides the L1/L2 cache consistency protocol. NOTE: the 82496 Cache Controller forces the Pentium processor into a write-once mode in order to maintain Modified data inclusion and assure cache consistency.

Table 1-10. Pentium™ Processor Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
WBA	O I	CC CS	The **Writeback Buffer Address** pin is driven by the 82496 Cache Controller to indicate which line is loaded into the writeback buffer by the 82491 Cache SRAM for replacement writebacks. For snoop writebacks, WBA indicates a snoop hit to the writeback buffer. WBA shares a pin with the Optimized Interface Configuration signal SEC2#
WBTYP	O I	CC CS	The 82496 Cache Controller **Writeback Cycle Type** pin is driven to the 82491 Cache SRAM to indicate a replacement writeback or snoop writeback cycle. WBTYP shares a pin with the Optimized Interface Configuration signal LR0.
WBWE#	0 I	CC CS	The 82496 Cache Controller **Writeback Buffer Write Enable** pin is used in conjunction with the WBA and WBTYP pins to load the writeback buffers of the 82491 Cache SRAM. WBWE# shares a pin with the Optimized Interface Configuration signal LR1.
WRARR#	O I	CC CS	The 82496 Cache Controller **Write to 82491 Cache SRAM Array** signal controls the writing of data into the 82491 Cache SRAM array and updating of the MRU bit.
WWOR#	I	CC	The **Weak Write Ordering Configuration** signal configures the 82496 Cache Controller into strong or weak write ordering modes. In strong ordering mode, the chip set writes data to memory in the order in which it was received from the Pentium processor. WWOR# shares a pin with the 82496 Cache Controller input signal MALE.

Table 1-11. Pentium™ Processor Cache Chip Set Internal Pull-Up Resistors

Pentium™ Processor	82496 Cache Controller	82491 Cache SRAM
BUSCHK#	ADS#	ADS#
R/S#	BGT#	BOFF#
SMI#	CNA#	HITM#
TCK	DRCTM#	MBE#
TDI	FLUSH#	MCLK
TMS	KWEND#	MFRZ#
TRST#	MRO#	MOCLK
	NA#	MZBT#
	SNPCLK	TCK
	SNPSTB#	TDI
	SWEND#	TMS
	SYNC#	
	TCK	
	TDI	
	TMS	
	TRST#	

NOTE: Internal pull-up resistor values are approximately 25K to 100K ohms.

Table 1-12. Pentium™ Processor Cache Chip Set Internal Pull-Down Resistors

Pentium™ Processor	82496 Cache Controller	82491 Cache SRAM
None	None	BLEC#

Table 1-13. Pentium™ Processor Cache Chip Set Glitch Free Pins

Pentium™ Processor	82496 Cache Controller	82491 Cache SRAM
APCHK#	APERR#	MISTB#[2]
FERR#	CADS#	MOSTB#[2]
HLDA	CDTS#	MEOC#[2]
IERR#	IPERR#	MSEL#[2]
LOCK#	KLOCK#	MZBT#[2]
PCHK#	MAPERR#	
	SNPADS#	
	SNPCYC#	

NOTES:

1. Glitch Free pins are always at a valid logic level following RESET.
2. These signals must be glitch free when the C8C is configured in strobed memory bus mode.

Table 1-14. Signal Interconnects on Optimized Interface

Pentium™ Processor	82496 Cache Controller			82491 Cache SRAM		
(I/O)	**256KB:**	(I/O)	**512KB:**	**256KB:**	(I/O)	**512KB:**
VSS	—		—	A0		—
VSS	CFA5		CFA4	A1		A0
A[4:3]	CFA[1:0]		CFA[1:0]	A[3:2]		A[2:1]
A5	CFA6		CFA5	A4		A3
A6	SET0		CFA6	A5		A4
A[16:7]	SET[10:1]		SET[9:0]	A[15:6]		A[14:5]
A17	TAG0		SET10			A15
A[28:18]	TAG[11:1]		TAG[10:0]			
A29	CFA2		TAG 11			
A30	CFA3		CFA2			
A31	CFA4		CFA3			
ADS# (O)				ADS# (I)		
ADSC# (O)	ADS# (I)					
AHOLD (I)	AHOLD (O)					
AP (I/O)	AP (I/O)					
BE[7:0]# (O)				BE# (I), CDATA[7:4] (I) *		
	BLAST# (O)			BLAST# (I)		
	BLEC# (O)			BLEC# (I)		
BOFF# (I)	BOFF# (O)			BOFF# (I)		
BRDYC# (I)	BRDYC1# (O)					
	BRDYC2# (O)			BRDYC# (I)		
BT[3:0] (I/O)	BT[3:0] (I/O)					
	BUS# (O)			BUS# (I)		
CACHE# (O)	CACHE# (I)					
D[63:0] (I/O)				CDATA[7:0] (I/O)		
D/C# (O)	D/C# (I)					
DP[7:0] (I/O)				CDATA[3:0] (I/O) *		
EADS# (I)	EADS# (O)					
EWBE# (I)	EWBE# (O)					

Table 1-14. Signal Interconnects on Optimized Interface (Contd.)

Pentium™ Processor	82496 Cache Controller	82491 Cache SRAM
HITM# (O)	HITM# (I)	HITM# (I)
INV (I)	INV (O)	
KEN# (I)	KEN# (O)	
LOCK# (O)	LOCK# (I)	
M/IO# (O)	M/IO# (I)	
	MAWEA# (O)	MAWEA# (I)
	MCYC# (O)	MCYC# (I)
NA# (I)	NA# (O)	
PCD (O)	PCD (I)	
PWT (O)	PWT (I)	
SCYC (O)	SCYC (I)	
W/R# (O)	W/R# (I)	W/R# (I)
	WAY (O)	WAY (I)
WB/WT# (I)	WB/WT# (O)	
	WBA [SEC2#] (O)	WBA [SEC2#] (I)
	WBTYP [LR0] (O)	WBTYP [LR0] (I)
	WBWE# [LR1] (O)	WBWE# [LR1] (I)
	WRARR# (O)	WRARR# (I)

* The Pentium processor Byte Enable outputs are connected to 82491 Cache SRAM CDATA[7:4] pins for 82491 Cache SRAMs configured to be data parity devices. The Pentium processor Data Parity signals are connected to 82491 Cache SRAM CDATA[3:0] pins for 82491 Cache SRAMs configured to be parity devices.

Table 1-15. Pin States during RESET

Pin Name	Part	State During RESET
APCHK#	Pentium™ processor	High
APERR#	82496 Cache Controller	High
APIC#	82496 Cache Controller	Undefined
BLE#	82496 Cache Controller	Low
BP[3:2],	Pentium processor	Low
BP/PM[1:0]		
BREQ	Pentium processor	Low
BT[3:0]	Pentium processor	Low
CADS#	82496 Cache Controller	High
CAHOLD	82496 Cache Controller	Note 1
CCACHE#	82496 Cache Controller	Undefined
CD/C#	82496 Cache Controller	Undefined
CDTS#	82496 Cache Controller	High
CM/IO#	82496 Cache Controller	Undefined
CPCD	82496 Cache Controller	Undefined
CPWT	82496 Cache Controller	Undefined
CSCYC	82496 Cache Controller	Undefined
CW/R#	82496 Cache Controller	Undefined
CWAY	82496 Cache Controller	Undefined
FERR#	Pentium processor	High
FSIOUT#	82496 Cache Controller	Low
HIT#	Pentium processor	High
HLDA	Pentium processor	Low
IBT	Pentium processor	Low
IERR#	Pentium processor	High
IPERR#	82496 Cache Controller	High

Pin Name	Part	State During RESET
IU	Pentium processor	Low
IV	Pentium processor	Low
KLOCK#	82496 Cache Controller	High
MAP	82496 Cache Controller	Undefined
MAPERR#	82496 Cache Controller	High
MBT[3:0]	82496 Cache Controller	Low
MCACHE#	82496 Cache Controller	Undefined
MCFA[6:0]	82496 Cache Controller	Undefined
MDATA[7:0]	82491 Cache SRAM	High-Z
MHITM#	82496 Cache Controller	High
MSET[10:0]	82496 Cache Controller	Undefined
MTAG[11:0]	82496 Cache Controller	Undefined
MTHIT#	82496 Cache Controller	High
NENE#	82496 Cache Controller	Undefined
PALLC#	82496 Cache Controller	Undefined
PCHK#	Pentium processor	High
PRDY	Pentium processor	Low
RDYSRC	82496 Cache Controller	Undefined
SMIACT#	Pentium processor	High
SMLN#	82496 Cache Controller	Undefined
SNPADS#	82496 Cache Controller	High
SNPBSY#	82496 Cache Controller	Low
SNPCYC#	82496 Cache Controller	High
TDO	Pentium processor	Note 2
	82496 Cache Controller	
	82491 Cache SRAM	

NOTES:

1. The state of CAHOLD depends upon whether self-test is selected.
2. The state of TDO is determined by boundary scan which is independent of all other signals including RESET.

Note that "Undefined" does not mean that the signal is floating. It means that the value being driven during RESET will vary.

Table 1-16. Pentium™ Processor Cache Chip Set Output Pins

Pin Name	Component	Active Level	Synchronous / Asynchronous	When Floated
ADS#	Pentium™ processor	Low	Synchronous to CLK	Bus Hold, BOFF#
ADSC#	Pentium processor	Low	Synchronous to CLK	Bus Hold, BOFF#
AHOLD	82496 Cache Controller	High	Synchronous to CLK	—
APCHK#	Pentium processor	Low	Synchronous to CLK	—
APERR#	82496 Cache Controller	Low	Synchronous to CLK	—
APIC#	82496 Cache Controller	Low	Synchronous to CLK	—
BE[7:0]#	Pentium processor	Low	Synchronous to CLK	Bus Hold, BOFF#
BLAST#	82496 Cache Controller	Low	Synchronous to CLK	—
BLE#	82496 Cache Controller	—	Synchronous to CLK	—
BLEC#	82496 Cache Controller	—	Synchronous to CLK	—
BOFF#	82496 Cache Controller	Low	Synchronous to CLK	—
BP[3:2], PM/BP[1:0]	Pentium processor		Synchronous to CLK	—
BRDYC1#	82496 Cache Controller	Low	Synchronous to CLK	—
BRDYC2#	82496 Cache Controller	Low	Synchronous to CLK	—
BREQ	Pentium processor	High	Synchronous to CLK	—
BT[3:0]	Pentium processor	—	Synchronous to CLK	Address Hold, Bus Hold, BOFF#
BUS#	82496 Cache Controller	Low	Synchronous to CLK	—
CACHE#	Pentium processor	Low	Synchronous to CLK	Bus Hold, BOFF#
CADS#	82496 Cache Controller	Low	Synchronous to CLK	—
CAHOLD	82496 Cache Controller	High	Synchronous to CLK	—
CCACHE#	82496 Cache Controller	Low	Synchronous to CLK	—
CD/C#	82496 Cache Controller	—	Synchronous to CLK	—
CDTS#	82496 Cache Controller	Low	Synchronous to CLK	—
CM/IO#	82496 Cache Controller	—	Synchronous to CLK	—
CPCD	82496 Cache Controller	High	Synchronous to CLK	—
CPWT	82496 Cache Controller	High	Synchronous to CLK	—
CSCYC	82496 Cache Controller	High	Synchronous to CLK	—

Table 1-16. Pentium™ Processor Cache Chip Set Output Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous	When Floated
CW/R#	82496 Cache Controller	—	Synchronous to CLK	—
CWAY	82496 Cache Controller	—	Synchronous to CLK	—
D/C#	Pentium processor	—	Synchronous to CLK	Bus Hold, BOFF#
EADS#	82496 Cache Controller	Low	Synchronous to CLK	—
EWBE#	82496 Cache Controller	Low	Synchronous to CLK	—
FERR#	Pentium processor	Low	Synchronous to CLK	—
FSIOUT#	82496 Cache Controller	Low	Synchronous to CLK	—
HIT#	Pentium processor	Low	Synchronous to CLK	—
HITM#	Pentium processor	Low	Synchronous to CLK	—
HLDA	Pentium processor	High	Synchronous to CLK	—
IBT	Pentium processor	High	Asynchronous	—
IERR#	Pentium processor	Low	Synchronous to CLK	—
INV	82496 Cache Controller	High	Synchronous to CLK	—
IPR#	82496 Cache Controller	Low	Synchronous to CLK	—
IU	Pentium processor	High	Synchronous to CLK	—
IV	Pentium processor	High	Synchronous to CLK	—
KEN#	82496 Cache Controller	Low	Synchronous to CLK	—
KLOCK#	82496 Cache Controller	Low	Synchronous to CLK	—
LOCK#	Pentium processor	Low	Synchronous to CLK	Bus Hold, BOFF#
M/IO#	Pentium processor	—	Synchronous to CLK	Bus Hold, BOFF#
MAPERR#	82496 Cache Controller	Low	Synchronous to CLK	—
MAWEA#	82496 Cache Controller	Low	Synchronous to CLK	—
MBE#	82491 Cache SRAM	Low	Synchronous to CLK	Reset to first CADS#
MBT[3:0]	82496 Cache Controller	—	Synchronous to CLK	MAOE# inactive
MCACHE#	82496 Cache Controller	Low	Synchronous to CLK	—
MCYC#	82496 Cache Controller	Low	Synchronous to CLK	—
MHITM#	82496 Cache Controller	Low	Synchronous to CLK	—
MTHIT#	82496 Cache Controller	Low	Synchronous to CLK	—

Table 1-16. Pentium™ Processor Cache Chip Set Output Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous	When Floated
NA#	82496 Cache Controller	Low	Synchronous to CLK	—
NENE#	82496 Cache Controller	Low	Synchronous to CLK	—
PALLC#	82496 Cache Controller	Low	Synchronous to CLK	—
PCD	Pentium processor	High	Synchronous to CLK	Bus Hold, BOFF#
PCHK#	Pentium processor	Low	Synchronous to CLK	—
PRDY	Pentium processor	High	Synchronous to CLK	—
PWT	Pentium processor	High	Synchronous to CLK	Bus Hold, BOFF#
RDYSRC	82496 Cache Controller	—	Synchronous to CLK	
SCYC	Pentium processor	High	Synchronous to CLK	Bus Hold, BOFF#
SMIACT#	Pentium processor	Low	Asynchronous	—
SMLN#	82496 Cache Controller	Low	Synchronous to CLK	—
SNPADS#	82496 Cache Controller	Low	Synchronous to CLK	—
SNPBSY#	82496 Cache Controller	Low	Synchronous to CLK	—
SNPCYC#	82496 Cache Controller	Low	Synchronous to CLK	—
TDO	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	—	Synchronous to TCK	All states except Shift-DR and Shift IR
W/R#	Pentium processor	—	Synchronous to CLK	Bus Hold, BOFF#
WAY	82496 Cache Controller	—	Synchronous to CLK	—
WB/WT#	82496 Cache Controller	—	Synchronous to CLK	—
WBA [SEC2#]	82496 Cache Controller	—	Synchronous to CLK	—
WBTYP [LR0]	82496 Cache Controller	—	Synchronous to CLK	—
WBWE# [LR1]	82496 Cache Controller	Low	Synchronous to CLK	—
WRARR#	82496 Cache Controller	Low	Synchronous to CLK	—

Table 1-17. Pentium™ Processor Cache Chip Set Input Pins

Pin Name	Component	Active Level	Synchronous / Asynchronous
A[15:0]	82491 Cache SRAM	—	Synchronous to CLK
A20M#	Pentium™ processor	Low	Asynchronous
ADS#	82491 Cache SRAM	Low	Synchronous to CLK
ADSC#	82496 Cache Controller	Low	Synchronous to CLK
AHOLD	Pentium processor	High	Synchronous to CLK
BE#	82491 Cache SRAM	Low	Synchronous to CLK
BGT# [CLDRV]	82496 Cache Controller	Low [—]	Synchronous to CLK
BLAST#	82491 Cache SRAM	Low	Synchronous to CLK
BLEC#	82491 Cache SRAM	Low	Synchronous to CLK
BOFF#	Pentium processor, 82491 Cache SRAM	Low	Synchronous to CLK
BRDY#	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	Low	Synchronous to CLK
BRDYC#	Pentium processor, 82491 Cache SRAM	Low	Synchronous to CLK
BT[3:0]	82496 Cache Controller	—	Synchronous to CLK
BUS#	82491 Cache SRAM	Low	Synchronous to CLK
BUSCHK#	Pentium processor	Low	Synchronous to CLK
CACHE#	82496 Cache Controller	Low	Synchronous to CLK
CLK	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	—	n/a
CNA# [CFG0]	82496 Cache Controller	Low [—]	Synchronous to CLK
CRDY# [SLFTST#]	82496 Cache Controller, 82491 Cache SRAM [CC]	Low [Low]	Synchronous to CLK
D/C#	82496 Cache Controller	—	Synchronous to CLK
DRCTM#	82496 Cache Controller	Low	Synchronous to CLK (Note 1)
EADS#	Pentium processor	Low	Synchronous to CLK
EWBE#	Pentium processor	Low	Synchronous to CLK
FLUSH#	Pentium processor, 82496 Cache Controller	Low	Asynchronous
FRCMC#	Pentium processor	Low	Asynchronous

Table 1-17. Pentium™ Processor Cache Chip Set Input Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous
HITM#	82496 Cache Controller, 82491 Cache SRAM	Low	Synchronous to CLK
HOLD	Pentium processor	High	Synchronous to CLK
IGNNE#	Pentium processor	Low	Asynchronous
INIT	Pentium processor	High	Asynchronous
INTR	Pentium processor	High	Asynchronous
INV	Pentium processor	High	Synchronous to CLK
KEN#	Pentium processor	Low	Synchronous to CLK
KWEND# [CFG2]	82496 Cache Controller	Low [—]	Synchronous to CLK
LOCK#	82496 Cache Controller	Low	Synchronous to CLK
M/IO#	82496 Cache Controller	—	Synchronous to CLK
MALE [WWOR#]	82496 Cache Controller	High [Low]	Asynchronous [Synchronous to CLK]
MAOE#	82496 Cache Controller	Low	Asynchronous (Note 2)
MAWEA#	82491 Cache SRAM	Low	Synchronous to CLK
MBALE [HIGHZ#]	82496 Cache Controller	High [Low]	Asynchronous [Synchronous to CLK]
MBAOE#	82496 Cache Controller	Low	Asynchronous (Note 2)
MBRDY#	82491 Cache SRAM	Low	Synchronous to MCLK
MCLK [MSTBM]	82491 Cache SRAM	— [—]	n/a [Synchronous to CLK]
MCYC#	82491 Cache SRAM	Low	Synchronous to CLK
MDOE#	82491 Cache SRAM	Low	Asynchronous
MEOC#	82491 Cache SRAM	Low	Synchronous to MCLK or Asynchronous
MFRZ# [MDLDRV]	82491 Cache SRAM	Low [—]	Synchronous to MCLK or Asynchronous [Synchronous to CLK]
MISTB	82491 Cache SRAM	Transition	Asynchronous
MKEN#	82496 Cache Controller	Low	Synchronous to CLK (Note 1)
MOCLK	82491 Cache SRAM	—	n/a
MOSTB	82491 Cache SRAM	Transition	Asynchronous
MRO#	82496 Cache Controller	Low	Synchronous to CLK (Note 1)
MSEL# [MTR4/8#]	82491 Cache SRAM	Low [—]	Synchronous to MCLK or Asynchronous [Synchronous to CLK]

Table 1-17. Pentium™ Processor Cache Chip Set Input Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous
MWB/WT#	82496 Cache Controller	—	Synchronous to CLK (Note 1)
MZBT# [MX4/8#]	82491 Cache SRAM	Low [—]	Synchronous to MCLK or Asynchronous [Synchronous to CLK]
NA#	Pentium processor	Low	Synchronous to CLK
NMI	Pentium processor	High	Asynchronous
PAR# (Note 3)	82491 Cache SRAM	Low	Synchronous to CLK
PCD	82496 Cache Controller	High	Synchronous to CLK
PWT	82496 Cache Controller	High	Synchronous to CLK
PEN#	Pentium processor	Low	Synchronous to CLK
R/S#	Pentium processor	—	Asynchronous
RESET	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	High	Asynchronous
SCYC	82496 Cache Controller	High	Synchronous to CLK
SMI#	Pentium processor	Low	Asynchronous
SNPCLK [SNPMD]	82496 Cache Controller	— [—]	n/a [Synchronous to CLK]
SNPINV	82496 Cache Controller	High	Note 2
SNPNCA	82496 Cache Controller	High	Note 2
SNPSTB#	82496 Cache Controller	Low	Note 2
SWEND# [CFG1]	82496 Cache Controller	Low [—]	Synchronous to CLK
SYNC# [MALDRV]	82496 Cache Controller	Low [—]	Asynchronous [Synchronous to CLK]
TCK	Pentium processor, 82496 Cache Controller 82491 Cache SRAM	—	n/a
TDI	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	—	Synchronous to TCK
TMS	Pentium processor, 82496 Cache Controller 82491 Cache SRAM	—	Synchronous to TCK

Table 1-17. Pentium™ Processor Cache Chip Set Input Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous
TRST#	Pentium processor, 82496 Cache Controller	Low	Asynchronous
W/R#	82496 Cache Controller, 82491 Cache SRAM	—	Synchronous to CLK
WAY	82491 Cache SRAM	—	Synchronous to CLK
WB/WT#	Pentium processor	—	Synchronous to CLK
WBA [SEC2#]	82491 Cache SRAM	—[—]	Synchronous to CLK
WBTYP [LR0]	82491 Cache SRAM	— [—]	Synchronous to CLK
WBWE# [LR1]	82491 Cache SRAM	Low [—]	Synchronous to CLK
WRARR#	82491 Cache SRAM	Low	Synchronous to CLK

NOTES:

1. DRCTM# and MWB/WT# must be synchronous to CLK while SWEND# is active. MKEN# and MRO# must be synchronous to CLK when KWEND# is active.
2. SNPSTB# is Synchronous to CLK in Synchronous snoop mode, Synchronous to SNPCLK in Clocked snoop mode, and Asynchronous in Strobed snoop mode. MAOE#, MBAOE#, SNPINV, and SNPNCA are sampled with SNPSTB#.
3. PAR# is a configuration input which shares a pin with the MBE# output signal.

Table 1-18. Pentium™ Processor Cache Chip Set Input/Output Pins

Pin Name	Component	Synchronous / Asynchronous	When Floated
A[31:3]	Pentium™ processor	Synchronous to CLK	Address Hold, Bus Hold, BOFF#, Note 3
AP	Pentium processor, 82496 Cache Controller	Synchronous to CLK	Address Hold, Bus Hold, BOFF#, Note 3
CDATA[7:0]	82491 Cache SRAM	Synchronous to CLK	RESET, BOFF#, see conditions 1,2 below (Note #5)
CFA[6:0], SET[10:0], TAG[11:0]	82496 Cache Controller	Synchronous to CLK	—
D[63:0]	Pentium processor	Synchronous to CLK	Bus Hold, BOFF#
DP[7:0]	Pentium processor	Synchronous to CLK	Bus Hold, BOFF#
MAP	82496 Cache Controller	Note 1	MAOE# inactive
MCFA[6:0], MSET[10:0], MTAG[11:0]	82496 Cache Controller	Note 1	MAOE# or MBAOE# inactive, Note 4
MDATA[7:0]	82491 Cache SRAM	Note 2	RESET, BOFF#, MDOE# inactive

NOTES:

1. When inputs: Synchronous to CLK, SNPCLK or SNPSTB#. When outputs: Synchronous to CLK, MAOE# active and MALE high.
2. Synchronous to CLK, MCLK, MOCLK or Asynchronous (MISTB/MOSTB).
3. The 82496 Cache Controller always asserts AHOLD to the Pentium processor (to float the CPU address signals) prior to BOFF# assertion (to float the 82491 Cache SRAM data signals). Technically, therefore, the BOFF# signal does not cause the Address lines to float since they have already been floated with AHOLD.
4. The specific 82496 Cache Controller address signals floated with MAOE# or MBAOE# are configuration dependent (refer to section 4.2.7).
5. The following conditions also cause the Cache SRAM CDATA[7:0] outputs to be tristated:
   (a) A write cycle on the memory bus
   (b) After the last BLAST#/BRDY# of a read cycle

Note that the appropriate signals on the CPU bus are floated in the CLK after either BOFF# or AHOLD is asserted.