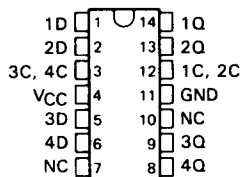


# SN54HC77, SN74HC77 4-BIT BISTABLE LATCHES

D2684, DECEMBER 1982 — REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC77 . . . J PACKAGE  
SN74HC77 . . . D OR N PACKAGE  
(TOP VIEW)



NC—No internal connection

Not available in chip carrier package with JEDEC-Standard pinout. For chip carrier information, contact the factory.

## description

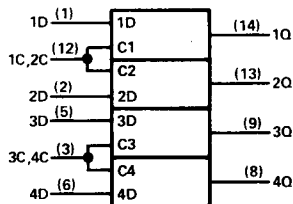
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information, which was present at the data input at the time the transition occurred, is retained at the Q output until the enable is permitted to go high.

The SN54HC77 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC77 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(Each Latch)

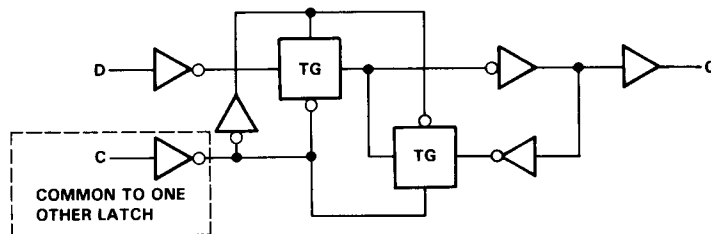
INPUTS		OUTPUT
D	C	Q
L	H	L
H	H	H
X	L	$Q_0$

## logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram, each latch (positive logic)



2

HCMOS Devices

# SN54HC77, SN74HC77 4-BIT BISTABLE LATCHES

2

HCMOS Devices

## absolute maximum ratings over operating free-air temperature range†

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}(V_I < 0 \text{ or } V_I > V_{CC})$ .....	$\pm 20$ mA
Output clamp current, $I_{OK}(V_O < 0 \text{ or } V_O > V_{CC})$ .....	$\pm 20$ mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$ .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND pins .....	$\pm 50$ mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: J package .....	300 °C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package .....	260 °C
Storage temperature range .....	-65 °C to 150 °C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

			SN54HC77			SN74HC77			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage		2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 6$ V	4.2			4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0	0.3		0	0.3		V
		$V_{CC} = 4.5$ V	0	0.9		0	0.9		
		$V_{CC} = 6$ V	0	1.2		0	1.2		
$V_I$	Input voltage		0	$V_{CC}$		0	$V_{CC}$		V
$V_O$	Output voltage		0	$V_{CC}$		0	$V_{CC}$		V
$t_t$	Input transition (rise and fall) times	$V_{CC} = 2$ V	0	1000		0	1000		ns
		$V_{CC} = 4.5$ V	0	500		0	500		
		$V_{CC} = 6$ V	0	400		0	400		
$T_A$	Operating free-air temperature		-55	125		-40	85		°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC77		SN74HC77		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL}, I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH} \text{ or } V_{IL}, I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH} \text{ or } V_{IL}, I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.80		5.2		5.34		
$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}, I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH} \text{ or } V_{IL}, I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH} \text{ or } V_{IL}, I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
$I_I$	$V_I = V_{CC} \text{ or } 0$	6 V		$\pm 0.1$	$\pm 100$		$\pm 1000$		$\pm 1000$	nA
$I_{CC}$	$V_I = V_{CC} \text{ or } 0, I_O = 0$	6 V			4		80		40	$\mu\text{A}$
$C_i$		2 to 6 V		3	10		10		10	pF

**SN54HC77, SN74HC77  
4-BIT BISTABLE LATCHES**

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

	V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC77		SN74HC77		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub> Pulse duration, C high	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t <sub>su</sub> Setup time, data before Cl	2 V	100		150		125		ns
	4.5 V	20		30		25		
	6 V	17		26		21		
t <sub>h</sub> Hold time, data after Cl	2 V	5		5		5		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C<sub>L</sub> = 50 pF (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC77		SN74HC77		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	2 V	40	120		180		150		ns
			4.5 V	12	24		36		30		
			6 V	10	20		31		26		
t <sub>pd</sub>	C	Q	2 V	45	130		195		165		ns
			4.5 V	14	26		39		33		
			6 V	11	22		33		28		
t <sub>t</sub>		Any	2 V	28	75		110		95		ns
			4.5 V	8	15		22		19		
			6 V	6	13		19		16		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

C <sub>pd</sub>	Power dissipation capacitance per latch	No load, T <sub>A</sub> = 25°C	16 pF typ
-----------------	---	--------------------------------	-----------

**2**

**HCMOS Devices**