Advance Information

LANCAM® WL Family

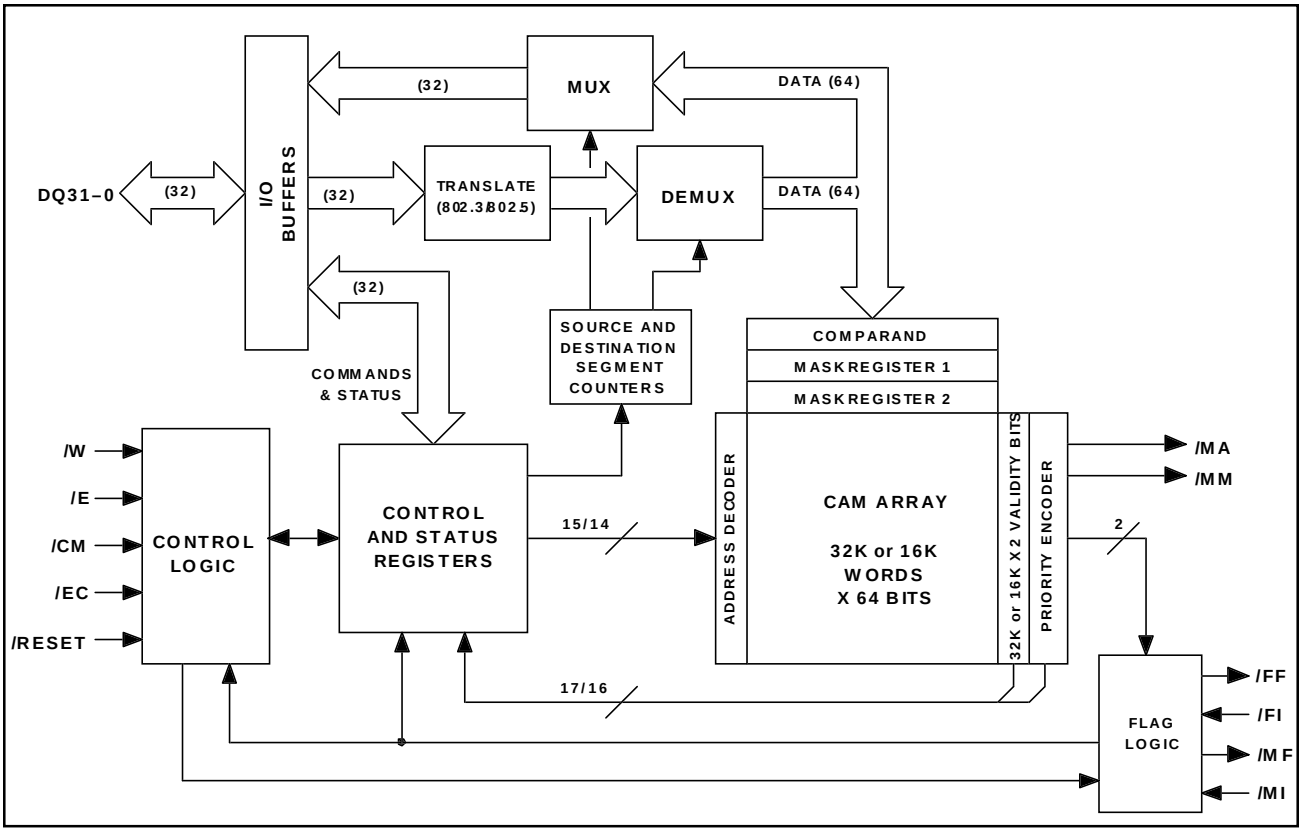
APPLICATION BENEFITS

Enhances Ethernet and Token-Ring LAN bridges and switches:

- **64-bit width stores 48-bit MAC address plus associated data (Port ID, time stamp, "permanent" flag)**
- **32-bit I/O supports ports of fast (100 Mb) Ethernet or Gigabit Ethernet**
- **Station list depth flexibility with choice of pin-compatible device densities and glue-free cascading**
- **3.3 Volt supply for low power operation**
- **Industrial temperature grades for harsh environments**

DISTINCTIVE CHARACTERISTICS

- **32,768 (MU9C7485) and 16,384 (MU9C6485) word CMOS content-addressable memories (CAMs)**
- **64-bit word width**
- **32-bit I/O**
- **Fast 50 ns compare speed**
- **Dual configuration register set for rapid context switching**
- **Increased flexibility of MUSIC's patented CAM/RAM partitioning**
- **160-Pin in PQFP package**
- **3.3 Volt operation**
- **IEEE 1149.1 (JTAG) compliant**



Block Diagram

GENERAL DESCRIPTION

The MU9C7485 and MU9C6485 LANCAM WLs are 64-bit wide content-addressable memories (CAMs), featuring a 32-bit wide interface. This interface doubles the available I/O bandwidth in many applications while maintaining the same powerful enhanced architecture and instruction set as the MU9C2480A/L.

Content-addressable memories, also known as associative memories, operate in the converse way to random access memories (RAM). In a RAM, the input to the device is an address and the output is the data stored at that address. In a CAM, the input is a data sample and the output is a flag to indicate a match and the address of the matching data. As a result, a CAM searches large databases for matching data in a short, constant time period, no matter how many entries are in the database. The ability to search data words up to 64 bits wide allows large address spaces to be searched rapidly and efficiently. A patented architecture links each CAM entry to associated data and makes this data available for use after a successful compare operation.

While the LANCAM WLs are optimized for LAN network address filtering, they are also well suited for applications that require high-speed data searching, such as virtual memories and cache management, data compression and encryption, database accelerators, and image processing.

OPERATIONAL OVERVIEW

To use the LANCAM WL, the user loads the data into the Comparand register, which is automatically compared to all valid CAM locations. The device then indicates whether or not one or more of the valid CAM locations contains data that match the target data. The status of each CAM location is determined by two validity bits at each memory location. The two bits are encoded to render four validity conditions: Valid, Empty, Skip, and RAM, as shown in Table 1. The memory can be partitioned into CAM and associated RAM segments on 16-bit boundaries, but by using one of the two available mask registers, the CAM/RAM partitioning can be set at any arbitrary size between zero and 64 bits.

The LANCAM WL's internal data path is 64 bits wide for rapid internal comparison and data movement. A data translation facility converts between IEEE 802.3 (CSMA/CD "Ethernet") and 802.5 (Token Ring) address formats. Vertical cascading of additional LANCAM WLs in a daisy chain fashion extends the CAM memory depth for large databases. Cascading requires no external logic. Loading data to the Control, Comparand, and mask registers automatically triggers a compare. Compares may also be initiated by a command to the device. Associated RAM data is available immediately after a successful compare operation. The Status register reports the results of compares including all flags and addresses. Two mask registers are available and can be used in two different ways: to mask comparisons or to mask data writes. The random access validity type allows additional masks to be stored in the CAM array where they may be retrieved rapidly.

A simple four-wire control interface and commands loaded into the Instruction decoder control the device. A powerful instruction set increases the control flexibility and minimizes software overhead. Additionally, dedicated pins for match and multiple-match flags enhance performance when the device is controlled by a state machine. These and other features make the LANCAM WL a powerful associative memory that drastically reduces search delays.

Skip Bit	Empty Bit	Entry Type
0	0	Valid
0	1	Empty
1	0	Skip
1	1	RAM

Table 1: Entry Types vs. Validity Bits

/W	/CM	Cycle Type
LOW	LOW	Command Write Cycle
LOW	HIGH	Data Write Cycle
HIGH	LOW	Command Read Cycle
HIGH	HIGH	Data Read Cycle

Table 2: I/O Cycles

PIN DESCRIPTIONS

All signals are implemented in CMOS technology with TTL levels. Signal names that start with a slash ("/") are active LOW. Inputs should never be left floating. The CAM architecture draws large currents during compare operations, mandating the use of good layout and bypassing techniques. Refer to the Electrical Characteristics section for more information.

/E (Chip Enable, Input, TTL)

The /E input enables the device while LOW. The falling edge registers the control signals /W, /CM, /EC. The rising edge locks the daisy chain, turns off the DQ pins, and clocks the Destination and Source Segment counters. The four cycle types enabled by /E are shown in Table 2.

/W (Write Enable, Input, TTL)

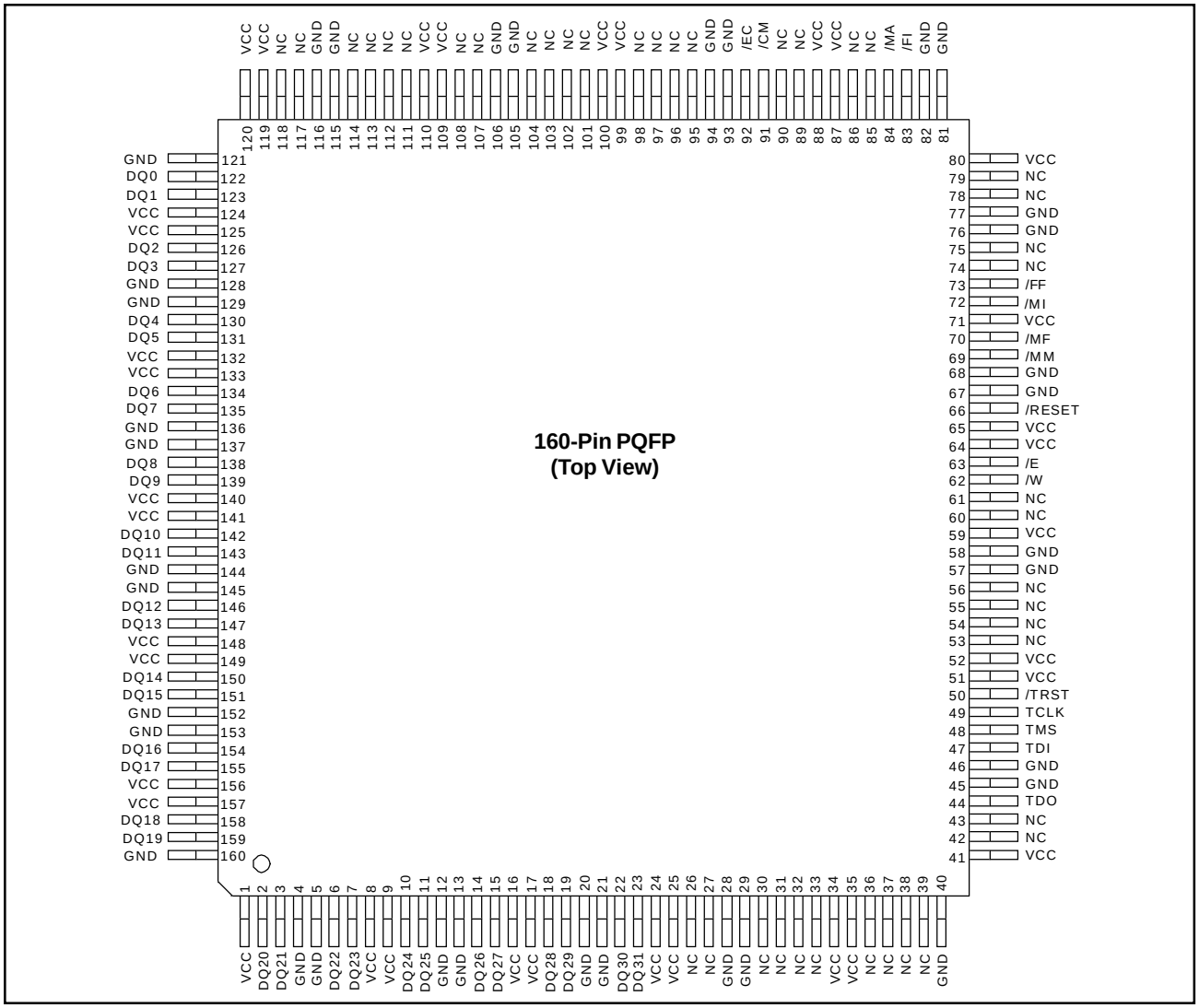
The /W input selects the direction of data flow during a device cycle. /W LOW selects a Write cycle and /W HIGH selects a Read cycle.

/CM (Data/Command Select, Input, TTL)

The /CM input selects whether the input signals on DQ31–0 are data or commands. /CM LOW selects Command cycles and /CM HIGH selects Data cycles.

/EC (Enable Daisy Chain, Input, TTL)

The /EC signal performs two functions. The /EC input enables the /MF output to show the results of a comparison, as shown in Figure 6 on page 15. If /EC is LOW at the falling edge of /E in a given cycle, the /MF output is enabled. Otherwise, the /MF output is held HIGH. The /EC signal



Pinout Diagram

PIN DESCRIPTIONS *Continued*

also enables the /MF–/MI daisy chain, which serves to select the device with the highest-priority match in a string of LANCAMs. Tables 6a and 6b on page 12 explain the effect of the /EC signal on a device with or without a match in both Standard and Enhanced modes. /EC must be HIGH during initialization.

DQ31–0 (Data Bus, I/O, TTL)
The DQ31–0 lines convey data, commands, and status to and from the LANCAM WL, as shown in Table 3. /W and /CM control the direction and nature of the information that flows to or from the device. When /E is HIGH, DQ31–0 go to HIGH-Z.

/MF (Match Flag, Output, TTL)
The /MF output goes LOW when one or more valid matches occur during a compare cycle. /MF becomes valid after /E goes HIGH on the cycle that enables the daisy chain (on the first cycle that /EC is registered LOW by the previous falling edge of /E; see Figure 6 on page 15). In a daisy chain, valid match(es) in higher priority devices are passed from the /MI input to /MF. If the daisy chain is enabled but the match flag is disabled in the Control register, the /MF output only depends on the /MI input of the device (/MF=/MI). /MF is HIGH if there is no match or when the daisy chain is disabled (/E goes HIGH when /EC was HIGH on the previous falling edge of /E). The System Match flag is the /MF pin of the last device in the daisy chain. /MF will be reset when the active configuration register set is changed.

/MI (Match Input, Input, TTL)
The /MI input prioritizes devices in vertically cascaded systems. It is connected to the /MF output of the previous device in the daisy chain. The /MI pin on the first device in the chain must be tied HIGH.

/MA (Device Match Flag, Output, TTL)
The /MA output is LOW when one or more valid matches occur during the current or the last previous compare cycle. The /MA output is not qualified by /EC or /MI, and reflects the match flag from that specific device's Status register. /MA will be reset when the active register set is changed.

/MM (Device Multiple Match Flag, Output, TTL)
The /MM output is LOW when more than one valid match occurs during the current or the last previous compare cycle. The /MM output is not qualified by /EC or /MI, and reflects the multiple match flag from that specific device's Status register. /MM will be reset when the active register set is changed.

/FF (Full Flag, Output, TTL)
If enabled in the Control register, the /FF output goes LOW when no empty memory locations exist within the device (and in the daisy chain above the device as indicated by the /FI pin). The System Full flag is the /FF pin of the last device in the daisy chain, and the Next Free address resides in the device with /FI LOW and /FF HIGH. If disabled in the Control register, the /FF output only depends on the /FI input (/FF = /FI).

/FI (Full Input, Input, TTL)
The /FI input generates a CAM-Memory-System-Full indication in vertically cascaded systems. It is connected to the /FF output of the previous device in the daisy chain. The /FI pin on the first device in a chain must be tied LOW.

/RESET (Reset, Input, TTL)
/RESET must be driven LOW to place the device in a known state before operation, which will reset the device to the conditions shown in Table 5 on page 10. The /RESET pin should be driven by TTL levels, not directly by an RC timeout. /E must be kept HIGH during /RESET.

/TRST (JTAG Reset, Input, TTL)
The /TRST input is the Test Reset input. It is internally pulled HIGH with a 25K resistor (minimum). This input must be tied to /RESET if in use or tied LOW when not in use.

/TCLK (JTAG Test Clock, Input, TTL)
The /TCLK input is the Test Clock input. It must be connected to a valid logic level when not in use.

TMS (JTAG Test mode Select, Input, TTL)
The TMS input is the Test Mode Select input. It is internally pulled HIGH with a 25K resistor (minimum).

TDI (JTAG Test Data Input, Input, TTL)
The TDI input is the Test Data input. It is internally pulled HIGH with a 25K resistor (minimum).

TDO (JTAG Test Data Output, Ouput, TTL)
The TDO output is the Test Data output.

VCC, GND (Positive Power Supply, Ground)
These pins are the power supply connections to the LANCAM WL. VCC must meet the voltage supply requirements in the Operating Conditions section relative to the GND pins, which are at 0 Volts (system reference potential), for correct operation of the device. All the ground and power pins must be connected to their respective planes with adequate bulk and high frequency bypassing capacitors in close proximity to the device.

FUNCTIONAL DESCRIPTION

The LANCAM WL is a content-addressable memory (CAM) with 32-bit I/O for network address filtering, virtual memory, data compression, caching, and table lookup applications. The memory consists of static CAM, organized in 64-bit data fields. Each data field can be partitioned into a CAM and a RAM subfield on 16-bit boundaries. The contents of the memory can be randomly accessed or associatively accessed by the use of a compare. During automatic comparison cycles, data in the Comparand register is automatically compared with the "Valid" entries in the memory array. The Device ID can be read using a TCO PS instruction (see Table 14 on page 24).

The data inputs and outputs of the LANCAM WL are multiplexed for data and instructions over a 32-bit I/O bus. Internally, data is handled on a 64-bit basis, since the Comparand register, the mask registers, and each memory entry are 64 bits wide. Memory entries are globally configurable into CAM and RAM segments on 16-bit boundaries, as described in US Patent 5,383,146 assigned to MUSIC Semiconductors. Seven different CAM/RAM splits are possible, with the CAM width going from one to four segments, and the remaining RAM width going from three to zero segments. Finer resolution on compare width is possible by invoking a mask register during a compare, which does global masking on a bit basis. The CAM subfield contains the associative data, which enters into compares, while the RAM subfield contains the associated data, which is not compared. In LAN bridges, the RAM subfield can hold, for example, port-address and aging information related to the destination or source address information held in the CAM subfield of a given location. In a translation application, the CAM field can hold the dictionary entries, while the RAM field holds the translations, with almost instantaneous response.

Each entry has two validity bits (known as Skip bit and Empty bit) associated with it to define its particular type: Empty, Valid, Skip, or RAM. When data is written to the active Comparand register, and the active Segment Control register reaches its terminal count, the contents of the Comparand register are automatically compared with the CAM portion of all the valid entries in the memory array. For added versatility, the Comparand register can be barrel-shifted right or left one bit at a time. A Compare instruction can then be used to force another compare between the Comparand register and the CAM portion of memory entries of any one of the four validity types. After a Read or Move from Memory operation, the validity bits of the location read or moved will be copied into the Status register, where they can be read from the Status register using Command Read cycles.

Data can be moved from one of the data registers (CR, MR1, or MR2) to a memory location that is based on the results of the last comparison (Highest-Priority Match or Next Free), or to an absolute address, or to the location pointed to by the active Address register. Data can also be written directly to the memory from the DQ bus using any of the above addressing modes. The Address register may be directly loaded and may be set to increment or decrement, allowing DMA-type reading or writing from memory.

Two sets of configuration registers (Control, Segment Control, Address, Mask Register 1, and Persistent Source and Destination) are provided to permit rapid context

/W	/CM	Cycle Type	"f" Bit	DQ31–16	DQ15–0
LOW	LOW	Command write	0	Non-TCO Instruction	XXXX
			1	Non-TCO Instruction	Absolute Address
			0	TCO Instruction (Read register)*	XXXX
			1	TCO Instruction (Write register)	Value to Register
HIGH	LOW	Command read	X	Status Register bits 31–16	Status Register bits 15–0
		TCO 2nd cycle	X	Status Register bits 31–16†	Register contents*
LOW	HIGH	Data write	X	Data to CR, MRX, Mem.	Data to CR, MRX, Mem.
HIGH	HIGH	Data read	X	Data from CR, MRX, Mem.	Data from CR, MRX, Mem.

Notes: * A CW of a TCO Instruction with the "f" bit set to 0 sets up a Register read in the following cycle. The following cycle must be a Command Read cycle, otherwise the register read will be cancelled.

† Upper 16 bits will be Status Register bits 31–16, except for a read of the Page Address register, in which case they will be all zeros.

Table 3: DQ Bus Multiplexing

FUNCTIONAL DESCRIPTION *Continued*

switching between foreground and background activities. Writes, reads, moves, and compares are controlled by the currently active set of configuration registers. The foreground set would typically be pre-loaded with values useful for comparing input data, often called filtering, while the background set would be pre-loaded with values useful for housekeeping activities such as purging old entries. Moving from the foreground task of filtering to the background task of purging can be done by issuing a single instruction to change the current set of configuration registers. The match condition of the device is reset whenever the active register set is changed.

The active Control register determines the operating conditions within the device. Conditions set by this register's contents are reset, enable or disable Match flag, enable or disable Full flag, default data translation, CAM/RAM partitioning, disable or select masking conditions, disable or select auto-incrementing or auto-decrementing the Address register, and select Standard (compatible with the MU9C1485) or Enhanced mode. The active Segment Control register contains separate counters to control the writing of 32-bit data segments to the selected persistent destination, and to control the reading of 32-bit data segments from the selected persistent source.

There are two active mask registers at any one time, which can be selected to mask comparisons or data writes. Mask Register 1 has both a foreground and background mode to support rapid context switching. Mask Register 2 does not have this mode, but can be shifted left or right one bit at a time. For masking comparisons, data stored in the active selected mask register determines which bits of the comparand are compared against the valid contents of the memory. If a bit is set HIGH in the mask register, the same bit position in the Comparand register becomes a "don't care" for the purpose of the comparison with all the memory locations. During a Data Write cycle or a MOV instruction, data in the specified active mask register can also determine which bits in the destination will be updated. If a bit is HIGH in the mask register, the corresponding bit of the destination is unchanged.

The match line associated with each memory address is fed into a priority encoder where multiple responses are resolved, and the address of the highest-priority responder (the lowest numerical match address) is generated. In the LAN bridge application, a multiple response might indicate an error. In other applications the existence of multiple responders may be valid.

Four input control signals and commands loaded into an instruction decoder control the LANCAM WL. Two of the four input control signals determine the cycle type. The control signals tell the device whether the data on the I/O bus represents data or a command, and is input or output. Commands are decoded by instruction logic and control moves, forced compares, validity bit manipulations, and the data path within the device. Registers (Control, Segment Control, Address, Next Free Address, etc.) are accessed using Temporary Command Override instructions. The data path from the DQ bus to/from data resources (comparand, masks, and memory) within the device are set until changed by Select Persistent Source and Destination instructions.

After a Compare cycle (caused by either a data write to the Comparand or mask registers, a write to the Control register, or a forced compare), the Status register contains the address of the Highest-Priority Matching location in that device, concatenated with its page address, along with flags indicating internal match, multiple match, and full. When the Status register is read with a Command Read cycle, the device with the Highest-priority match will respond, outputting the System Match address to the DQ bus. The internal Match (/MA) and Multiple match (/MM) flags are also output on pins. Another set of flags (/MF and /FF) that are qualified by the match and full flags of previous devices in the system are also available directly on output pins, and are independently daisy-chained to provide System Match and Full flags in vertically cascaded LANCAM arrays. In such arrays, if no match occurs during a comparison, read access to the memory and all the registers except the Next Free register is denied to prevent device contention. In a daisy chain, all devices will respond to Command and Data Write cycles, depending on the conditions shown in Tables 6a and 6b on page 12, unless the operation involves the Highest-Priority Match address or the Next Free address; in which case, only the specific device having the Highest-Priority match or the Next Free address will respond.

A Page Address register in each device simplifies vertical expansion in systems using more than one LANCAM. This register is loaded with a specific device address during system initialization, which then serves as the higher-order address bits. A Device Select register allows the user to target a specific device within a vertically cascaded system

FUNCTIONAL DESCRIPTION *Continued*

by setting it equal to the Page Address Register value, or to address all the devices in a string at the same time by setting the Device Select value to FFFFH.

Figure 1a shows expansion using a daisy chain. Note that system flags are generated without the need for external logic. The Page Address register allows each device in the vertically cascaded chain to supply its own address in the event of a match, eliminating the need for an external priority encoder to calculate the complete Match address at the expense of the ripple-through time to resolve the highest-priority match. The Full flag daisy-chaining allows Associative writes using a Move to Next Free Address instruction, which does not need a supplied address.

Figure 1b shows an external PLD implementation of a simple priority encoder that eliminates the daisy chain ripple-through delays for systems requiring maximum performance from many CAMS.

OPERATIONAL CHARACTERISTICS

Throughout the following, "aaaH" represents a three-digit hexadecimal number "aaa," while "bbB" represents a two-digit binary number "bb." All memory locations are written to or read from in 32-bit segments. Segment 0 corresponds to the lowest order bits (bits 31–0) and Segment 1 corresponds to the highest order bits (bits 63–32).

THE CONTROL BUS

Refer to the Block Diagram on page 1 for the following discussion. The inputs Chip Enable (/E), Write Enable (/W), Command Enable (/CM), and Enable Daisy Chain (/EC) are the primary control mechanism for the LANCAM WL. The /EC input of the Control bus enables the /MF Match flag output when LOW and controls the daisy chain operation. Instructions are the secondary control mechanism. Logical combinations of the Control Bus inputs, coupled with the execution of Select Persistent Source (SPS), Select Persistent Destination (SPD), and Temporary Command Override (TCO) instructions allow the I/O operations to and from the DQ31–0 lines to the internal resources, as shown in Table 4 on page 9.

The Comparand register is the default source and destination for Data Read and Write cycles. This default state can be

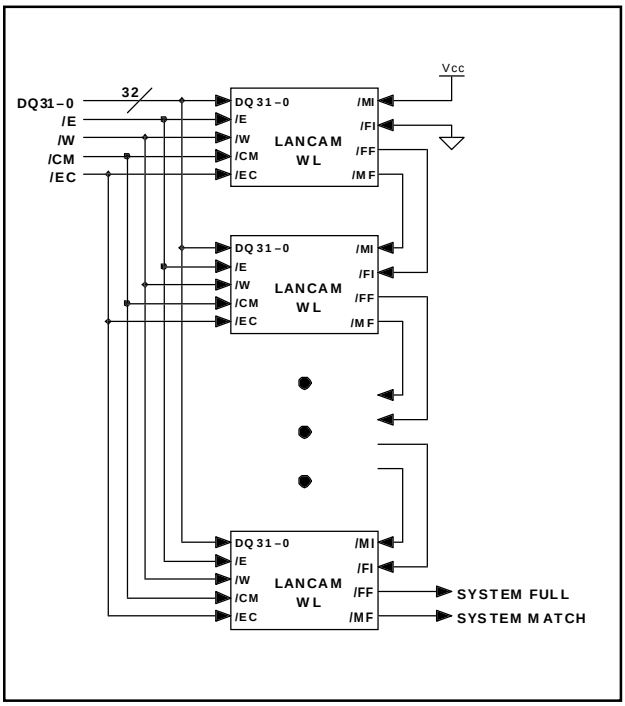


Figure 1a: Vertical Cascading

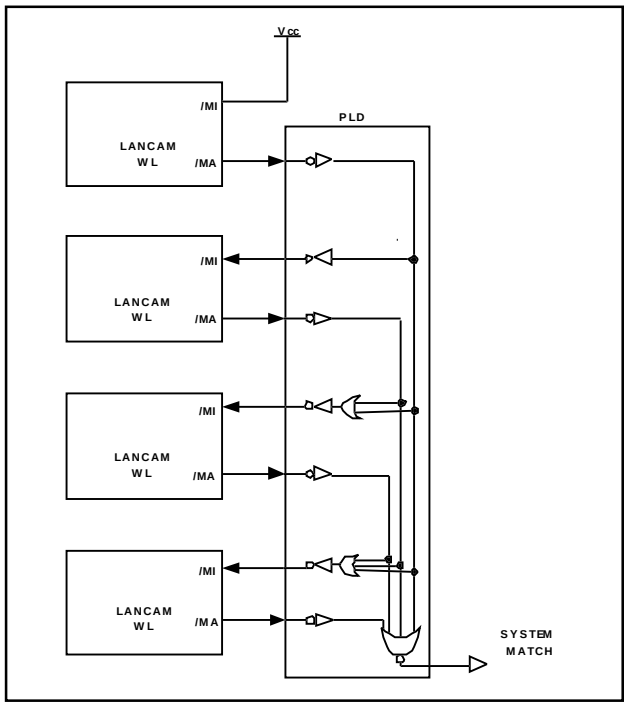


Figure 1b: External Prioritizing

OPERATIONAL CHARACTERISTICS *Continued*

overridden independently by executing a Select Persistent Source or Select Persistent Destination instruction, selecting a different source or destination for data. Subsequent Data Read or Data Write cycles will access that source or destination until another SPS or SPD instruction is executed. The currently selected persistent source or destination can be read back through a TCO PS or PD instruction. The sources and destinations available for persistent access are those resources on the 64-bit bus: Comparand register, Mask Register 1, Mask Register 2, and the Memory array.

The default destination for Command Write cycles is the Instruction decoder, while the default source for Command Read cycles is the Status register. The entire 32-bit Status register is read in a single cycle.

Temporary Command Override (TCO) instructions provide access to the Control register, the Page Address register, the Segment Control register, the Address register, the Next Free Address register, and Device Select register. These instructions are only active for one Command Write cycle to write a value into a register, or one Command Write cycle followed by a Command Read cycle to read a register's contents. Each of these 16-bit registers is read out on the DQ15–0 pins, with the upper 16 bits of the Status register output on the DQ31–16 pins (except in the case of a Page Address register read where 0s will be read on DQ31–16 instead), as shown in Table 3 on page 5.

The data and control interfaces to the LANCAM WL are synchronous. During a Write cycle, the Control and Data inputs are registered by the falling edge of /E. When writing to the persistently selected data destination, the Destination Segment counter is clocked by the rising edge of /E. During a Read cycle, the Control inputs are registered by the falling edge of /E, and the Data outputs are enabled while /E is LOW. When reading from the persistently selected data source, the Source Segment counter is clocked by the rising edge of /E.

THE REGISTER SET

The Control, Segment Control, Address, Mask Register 1, and the Persistent Source and Destination registers are duplicated, with one set termed the Foreground set and the other the Background set. The active set is chosen by issuing Select Foreground Registers or Select Background Registers instructions. By default, the Foreground set is active after a reset. Having two alternate sets of registers that determine the device configuration allows for a rapid return to a foreground network filtering task from a background housekeeping task.

Writing a value to the Control register or writing data to the last segment of the Comparand or either mask register will cause an automatic comparison to occur between the contents of the Comparand register and the words in the CAM segments of the memory marked valid, masked by MR1 or MR2 if selected in the Control register.

Instruction Decoder

The Instruction decoder is the write-only decode logic for instructions and is the default destination for Command Write cycles using the DQ31–16 lines. If the instruction requires an absolute address or register value, the "f" Address Field flag (bit 11) of the instruction is set to a 1, and the data on the DQ15–0 lines are written to the proper register in that same cycle. If the instruction written is a TCO, and the "f" bit is not set, the contents of the register specified by the TCO may be read back by a successive Command Read cycle to the DQ15–0 signal lines.

If the Address Field flag is set in a memory access instruction, the absolute address supplied on the DQ15–0 lines is loaded into the Address register, and the instruction completes at the new address. If the Address Field flag is not set, the memory access occurs at the address currently contained in the Address register. After the execution of the instruction, the Address register will increment, decrement, or stay the same value depending on the setting of Control Register bits CT3 and CT2.

Control Register (CT)

The Control register is composed of a number of switches that configure the LANCAM WL, as shown in Table 10 on page 23. It is written or read through DQ15–0 using a TCO CT instruction on DQ31–16. On read cycles, DQ31–16 will be the upper 16 bits of the Status register. If bit 15 of the value written during a TCO CT is a 0, the device is reset (and all other bits are ignored). See Table 5 for the Reset states. Bit 15 always reads back as a 0. A write to the Control register causes an automatic compare to occur (except in the case of a reset). Either the Foreground or Background Control register will be active, depending on which register set has been selected, and only the active Control register will be written to or read from.

If the Match flag is disabled through bits 14 and 13, the internal match condition, /MA(int), used to determine a

OPERATIONAL CHARACTERISTICS *Continued*

Cycle Type	/E	/CM	/W	I/O Status	SPS	SPD	TCO	Operation	Notes
Cmd Write	L	L	L	IN				Load Instruction decoder	1
				IN			✓	Load Address register	2
				IN			✓	Load Control register	2
				IN			✓	Load Page Address register	2
				IN			✓	Load Segment Control register	2
				IN			✓	Load Device Select register	2
				IN				Deselected	9
Cmd Read	L	L	H	OUT			✓	Read Next Free Address register	3
				OUT			✓	Read Address register	3
				OUT				Read Status Register bits 31–0	4
				OUT			✓	Read Control register	3
				OUT			✓	Read Page Address register	3
				OUT			✓	Read Segment Control register	3
				OUT			✓	Read Device Select register	3
				OUT			✓	Read Current Persistent Source or Destination	3, 10
				HIGH-Z				Deselected	9
Data Write	L	H	L	IN		✓		Load Comparand register	5, 8
				IN		✓		Load Mask Register 1	6, 8
				IN		✓		Load Mask Register 2	6, 8
				IN		✓		Write Memory Array at address	6, 8
				IN		✓		Write Memory Array at Next Free address	6, 8
				IN		✓		Write Memory Array at Highest-Priority match	6, 8
				IN				Deselected	9
Data Read	L	H	H	OUT	✓			Read Comparand register	5, 8
				OUT	✓			Read Mask Register 1	7, 8
				OUT	✓			Read Mask Register 2	7, 8
				OUT	✓			Read Memory Array at address	7, 8
				OUT	✓			Read Memory Array at Highest-Priority match	7, 8
				HIGH-Z				Deselected	9
	H	X	X	HIGH-Z				Deselected	

Notes:

1. Default Command Write cycle destination (does not require a TCO instruction).
2. To load a value into a register using a TCO instruction takes one Command Write cycle with the “f” bit equal to 1, and the value to be loaded into the selected register placed in DQ15–0.
3. Reading the contents of a register using a TCO instruction takes two cycles. The first cycle is a Command Write of a TCO instruction with the “f” bit equal to 0. If the next cycle is a Command Read, the value stored in the selected register will be read out on the DQ15–0 lines. Additionally, bits 31–16 of the Status register will be read out on the DQ31–16 lines, except in the case of a Page Address read where 0s will be read on DQ31–16 instead.
4. Default Command Read cycle source (does not require a TCO instruction).
5. Default persistent source and destination after Reset. If other resources were sources or destinations, SPD CR or SPS CR restores the Comparand register as the destination or source.
6. Selected by executing a Select Persistent Destination instruction.
7. Selected by executing a Select Persistent Source instruction.
8. Access is performed in one or two 32-bit Read or Write cycles. The Segment Control register is used to control the selection of the desired 32-bit segment(s) by establishing the Segment counters’ limits and start values.
9. Device is deselected if Device Select register setting does not equal Page Address register setting, unless the Device Select register is set to FFFFH which allows only write access to the device, except in the case of a match. (Writes to the Device Select register are always active.) Device may also be deselected under locked daisy chain conditions as shown in Tables 6a and 6b on page 12.
10. A Command Read cycle after a TCO PS or TCO PD reads back the Instruction decoder bits that were last set to select a persistent source or destination. The TCO PS instruction will also read back the Device ID.

Table 4: Input/Output Operations

OPERATIONAL CHARACTERISTICS *Continued*

CAM Status	/RESET Condition
Validity bits at all memory locations	Skip = 0, Empty = 1 (empty)
Match and Full flag outputs	Enabled
IEEE 802.3-802.5 Input Translation	Not Translated
CAM/RAM Partitioning	64 bits CAM, 0 bits RAM
Comparison Masking	Disabled
Address register auto-increment or auto-decrement	Disabled
Source and Destination Segment counters count ranges	0B to 1B; loaded with 0B
Address register and Next Free Address register	Contain all 0s
Page Address and Device Select registers	Contain all 0s (no change on Software reset)
Control register after reset (including CT15)	Contains 0008H
Persistent Destination for Command writes	Instruction decoder
Persistent Source for Command reads	Status register
Persistent Source and Destination for Data reads and writes	Comparand register
Operating Mode	Standard
Configuration Register set	Foreground

Table 5: Device Control State After Reset

daisy-chained device's response is forced HIGH as shown in Tables 6a and 6b on page 12, so that Case 6 is not possible, effectively removing the device from the daisy chain. With the Match flag disabled, /MF=/MI and operations directed to Highest-priority Match locations are ignored. Normal operation of the device is with the /MF enabled. The Match Flag Enable field has no effect on the /MA or /MM output pins or Status Register bits. These bits always reflect the true state of the device.

If the Full Flag is disabled through bits 12 and 11, the device behaves as if it were full and ignores instructions to Next Free address. Additionally, writes to the Page Address register will be disabled. All other instructions operate normally. Additionally, with the /FF disabled, /FF=/FI. Normal operation of the device is with the /FF enabled. The Full Flag Enable field has no effect on the /FL Status Register bit. This bit always reflects the true state of the device.

The IEEE Translation control at bits 10 and 9 can be used to enable the translation hardware for writes to 64-bit resources in the device. When translation is enabled, the bits are reordered as shown in Figure 2.

Control Register bits 8–6 control the CAM/RAM partitioning. The CAM portion of each word may be sized from a full 64 bits down to 16 bits in 16-bit increments. The RAM portion can be at either end of the 64-bit word.

Compare masks may be selected by bits 5 and 4. Mask Register 1, Mask Register 2, or neither may be selected to mask compare operations. The address register behavior is controlled by bits 3 and 2, and may be set to increment, decrement, or neither after a memory access. Bits 1 and 0 set the operating mode: Standard (compatible with the MU9C1485) as shown in Table 6a, or Enhanced as shown in Table 6b on page 12. The device will reset to Standard mode and follow the operating responses in Table 6a. When operating in Enhanced mode, it is not necessary to unlock the daisy chain with a NOP instruction before command or data writes after a non-matching compare, as required in Standard mode.

Segment Control Register (SC)

The Segment Control register, as shown in Table 11 on page 23, is accessed using a TCO SC instruction with the register contents placed on DQ15–0. On read cycles, DQ31–16 will be the upper 16 bits of the Status register, and D15, D10, D5, and D2 always read back as 0s. Reserved locations D14, D12, D9, D7, D4, and D1 should always be set to 0 and as such will also read back as 0s. Either the Foreground or Background Segment Control register will be active, depending on which register set has been selected, and only the active Segment Control register will be written to or read from.

The Segment Control register contains dual independent incrementing counters with limits, one for data reads and one for data writes. These counters control which 32-bit segment of the 64-bit internal resource is accessed during a particular data cycle on the 32-bit data bus. The actual

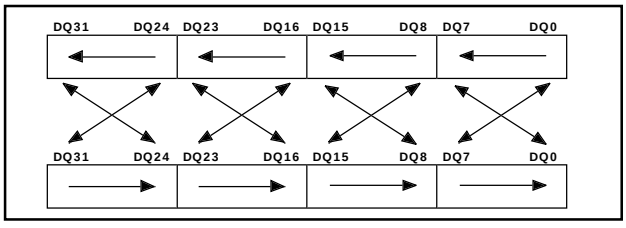


Figure 2: IEEE 802.3/802.5 Format Mapping

destination for data writes and source for data reads (called the persistent destination and source) are set independently with SPD and SPS instructions, respectively.

Each of the two counters consists of a start limit, an end limit, and the current segment pointer, each a single bit representing either the lower segment (0) or the upper segment (1). The current segment pointer can be set to either 0 or 1 even if that value is outside the range set by the start and end segments. The counters count up from the current segment pointer to the end limit and then roll over back to the start limit.

If a sequence of data writes or reads is interrupted, the Segment Control register can be reset to its initial start limit values with the RSC instruction. After a reset, both Source and Destination counters are set to count from Segment 0 to Segment 1 with an initial value of 0.

Page Address Register (PA)

The Page Address register is loaded using a TCO PA instruction on DQ31–16 with a user selected 16-bit value (not FFFFH) on DQ15–0. During reads of the PA register, DQ31–16 will all be 0. The entry in the PA register is used to give a unique address to the different devices in a daisy chain. In a daisy chain, the PA value of each device is loaded using the SFF instruction to advance to the next device, as shown in the "Setting Page Address Register Values" section on page 18. A software reset (using the Control register) does not affect the Page Address register.

Device Select Register (DS)

The Device Select register is used to select a specific (target) device using the TCO DS instruction in DQ31–16 and setting the 16-bit DS value in DQ15–0 equal to the target's PA value. The DS register can be read through DQ15–0 with DQ31–16 returning the upper 16 bits of the Status register. In a daisy chain, setting DS = FFFFH will select all devices. However, in this case, the ability to read information out of the device is restricted as shown in Tables 6a and 6b. A software reset (using the Control register) does not affect the Device Select register.

Address Register (AR)

The Address register points to the CAM memory location to be operated upon when a M@[AR] or M@aaaH is part of the instruction. It can be loaded directly by using a TCO AR instruction or indirectly by using an instruction requiring an absolute address, such as MOV aaaH, CR,V. The AR register can be read through DQ15–0 with DQ31–16 returning the upper 16 bits of the Status register. After being loaded, the Address register value will then be used for the next memory access referencing the Address register. A reset sets the Address register to zero.

Control Register bits CT3 and CT2 set the address to automatically increment or decrement (or not change) during sequences of Command or Data cycles. The Address register will change after executing an introduction that includes M@[AR] or M@aaaH, or after a data access to the end limit segment (as set in the Segment Control register) when the persistent source of destination is M@[AR] or M@aaaH.

Either the Foreground or Background Address register will be active, depending on which register set has been selected, and only the active Address register will be written to or read from.

Next Free Address Register (NF)

The LANCAM WL automatically stores the address of the first empty memory location in the Next Free Address register, which is then used as a memory address pointer for M@NF operations. The Next Free Address register, shown in Table 12 on page 24, can be read through DQ15–0 using a TCO NF instruction. DQ31–16 will return the upper 16 bits of the Status register. By taking /EC LOW during the TCO NF instruction cycle, only the device with /FI LOW and /FF HIGH will output the contents of its Next Free Address register, which gives the Next Free address in a system of daisy-chained devices. The Next Free address may be read from a specific device in the chain by setting the Device Select register to the value of the desired device's Page address and leaving /EC HIGH.

The Full Flag daisy chain causes only the device whose /FI input is LOW and /FF output HIGH to respond to an instruction using the Next Free address. After a reset, the Next Free Address register is set to zero.

Status Register

The 32-bit Status register, shown in Table 13 on page 24, is the default source for Command Read cycles. Bit 31 is the internal Match flag, which will go LOW if a match was found in this particular device. Bit 30 is the internal Multiple Match flag, which will go LOW if a Multiple match was detected. Bit 29 is the internal Full flag, which will go LOW if the particular device has no empty memory locations. Bits 28 and 27 are the Skip and Empty Validity bits, which reflect the validity of the last memory location read. After a reset, the Skip and Empty bits will read 11 until a read or move from memory has occurred. The rest of the Status register contains the Page address of

OPERATIONAL CHARACTERISTICS *Continued*

Case	Internal /EC(int)	Internal /MA (int)	External /MI	Device Select Reg.	Command Write[1]	Data Write	Command Read	Data Read
1	1	X	X	DS=FFFFH	YES[3]	YES[4]	NO	NO
2	1	X	X	DS=PA	YES[3]	YES[4]	YES	YES
3	1	X	X	DS≠FFFFH and DS≠PA	NO	NO	NO	NO
4	0	X	0	X	NO	NO	NO[5]	NO
5	0	1	1	X	NO	NO	NO[5]	NO
6[2]	0	0	1	X	YES[3]	YES[4]	YES[5]	YES

Table 6a: Standard Mode Device Select Response

Case	Internal /EC(int)	Internal /MA (int)	External /MI	Device Select Reg.	Command Write[1]	Data Write	Command Read	Data Read
1	1	X	X	DS = FFFFH	YES[3]	YES[4]	NO	NO
2	1	X	X	DS = PA	YES[3]	YES[4]	YES	YES
3	1	X	X	DS ≠ FFFFH and DS ≠ PA	NO	NO	NO	NO
4	0	0	0	X	YES[3,6]	YES[4,7]	NO[5]	NO
5	0	1	X	X	YES[3,6]	YES[4,7]	NO[5]	NO
6[2]	0	0	1	X	YES[3]	YES[4]	YES[5]	YES

Table 6b: Enhanced Mode Device Select Response

NOTES:

1. Exceptions are:
   A) A write to the Device Select register is always active in all devices;
   B) A write to the Page Address register is active in the device with /FI LOW and /FF HIGH; and
   C) The Set Full Flag (SFF) instruction is active in the device with /FI LOW and /FF HIGH.
2. If /MF is disabled in the Control register, /MA (Int) is forced HIGH preventing a Case 6 response.
3. This is NO for a MOV instruction involving Memory at Next Free address if /FI is HIGH or the device is full.
4. This is NO if the Persistent Destination is Memory at Next Free address and /FI is HIGH or the device is full.
5. For a Command read following a TCO NF instruction, this is YES if the device contains the first empty location in a daisy chain (i.e., /FI LOW and /FF HIGH) and NO if it does not.
6. This is NO for a MOV or VBC instruction involving Memory at Highest-Priority match.
7. This is NO if the Persistent Destination is Memory at Highest-Priority match.

the device and the address of the Highest-Priority match. After a reset or a no-match condition, the match address bits will be all 1s.

Comparand Register (CR)

The 64-bit Comparand register is the default destination for data writes and reads, using the Segment Control register to select which of the two 32-bit segments of the Comparand register is to be loaded or read out. The persistent source and destination for data writes and reads can be changed to the mask registers or memory by SPS and SPD instructions. During an automatic or forced compare, the Comparand register is simultaneously compared against the CAM portion of all memory locations with the correct validity condition. Automatic compares always compare against valid memory locations, while forced compares, using CMP instructions, can compare against memory locations tagged with any specific validity condition.

The Comparand register may be shifted one bit at a time to the right or left by issuing a Shift Right or Shift Left instruction, with the right and left limits for the wraparound determined by the CAM/RAM partitioning set in the Control register. During shift rights, bits shifted off the LSB of the CAM partition will reappear at the MSB of the CAM partition. Likewise, bits shifted off the MSB of the CAM partition will reappear at the LSB during shift lefts.

OPERATIONAL CHARACTERISTICS *Continued*

Mask Registers (MR1, MR2)

The Mask registers can be used in two different ways: either to mask compares or to mask data writes and moves. Either mask register can be selected in the Control register to mask every compare, or selected by instructions to participate in data writes or moves to and from Memory. If a bit in the selected mask register is set to a 0, the corresponding bit in the Comparand register will enter into a masked compare operation. If a Mask bit is a 1, the corresponding bit in the Comparand register will not enter into a masked compare operation. Bits set to 0 in the mask register cause corresponding bits in the destination register or memory location to be updated when masking data writes or moves, while a bit set to 1 will prevent that bit in the destination from being changed.

Either the Foreground or Background MR1 can be set active, but after a reset, the Foreground MR1 is active by default. MR2 incorporates a sliding mask, where the data can be replicated one bit at a time to the right or left with no wraparound by issuing a Shift Right or Shift Left instruction. The right and left limits are determined by the CAM/RAM partitioning set in the Control register. For a Shift Right the upper limit bit is replicated to the next lower bit, while for a Shift Left the lower limit bit is replicated to the next higher bit.

THE MEMORY ARRAY

Memory Organization

The Memory array is organized into 64-bit words with each word having an additional two validity bits (Skip and Empty). By default, all words are configured to be 64 CAM cells. However, bits 8–6 of the Control register can divide each word into a CAM field and a RAM field. The RAM field can be assigned to the least-significant or most-significant portion of each entry. The CAM/RAM partitioning is allowed on 16-bit boundaries, permitting selection of the configurations shown in Table 10 on page 23, bits 8–6 (e.g., “001” sets the 48 MSBs to CAM and the 16 LSBs to RAM). Memory Array bits designated as RAM can be used to store and retrieve data associated with the CAM content at the same memory location.

Memory Access

There are two general ways to get data into and out of the Memory array: directly or by moving the data by means of the Comparand or mask registers.

The first way, through direct reads or writes, is set up by issuing a Set Persistent Destination (SPD) or Set Persistent Source (SPS) command. The addresses for the direct access can be directly supplied, supplied from the Address register, supplied from the Next Free Address register, or supplied as the Highest-Priority Match address. Additionally, all the direct writes can be masked by either mask register.

The second way is to move data by means of the Comparand or mask registers. This is accomplished by issuing Data Move commands (MOV). Moves using the Comparand register can also be masked by either of the mask registers.

I/O CYCLES

The LANCAM WL supports four basic I/O cycles: Data Read, Data Write, Command Read, and Command Write. The states of the /W and /CM control inputs determine the cycle type. These signals are registered at the beginning of a cycle by the falling edge of /E. Table 3 on page 5 shows how the /W and /CM lines select the cycle type and how the data bus is utilized for each.

During Read cycles, the DQ31–0 outputs are enabled after /E goes LOW. During Write cycles, the data or command to be written is captured from DQ31–0 at the beginning of the cycle by the falling edge of /E. Figures 3 and 4 show Read and Write cycles respectively. Figure 5 shows typical cycle-to-cycle timing with the Match flag valid at the end of the Comparand Write cycle, assuming /EC is LOW at the start of this cycle. Data writes and reads to the comparand, mask registers, or memory occur in one or two 32-bit cycles, depending on the settings in the Segment Control register. The Compare operation automatically occurs during Data writes to the Comparand or mask registers when the destination segment counter reaches the end count set in the Segment Control register. If there was a match, the second cycle reads status or associated data, depending on the state of /CM. For cascaded devices, /EC needs to be LOW at the start of the cycle prior to any cycle that requires a locked daisy chain, such as a Status register or associated data read after a match. If there is no match in Standard mode, the output buffers stay HIGH-Z, and the daisy chain must be unlocked by taking /EC HIGH during a NOP or other non-functioning cycle, as indicated in Table 6. Figure 6 on page 15 shows how the internal /EC timing holds the daisy chain locking effect over into the next cycle. In the Enhanced mode, this NOP is not needed before data or command writes following a non-matching compare, as

OPERATIONAL CHARACTERISTICS *Continued*

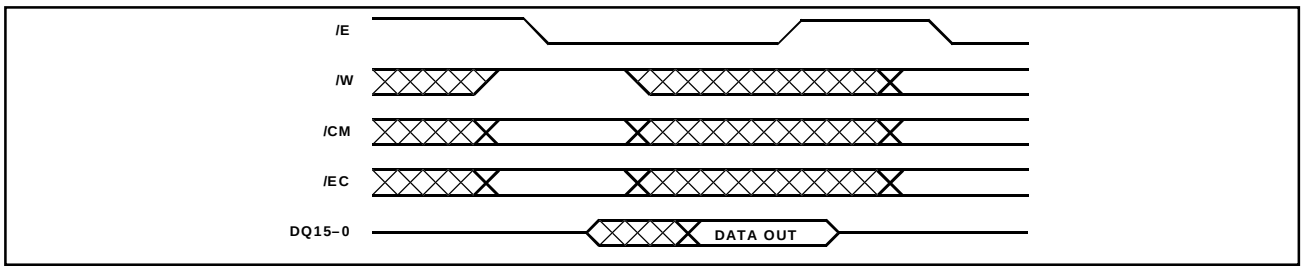


Figure 3: Read Cycle

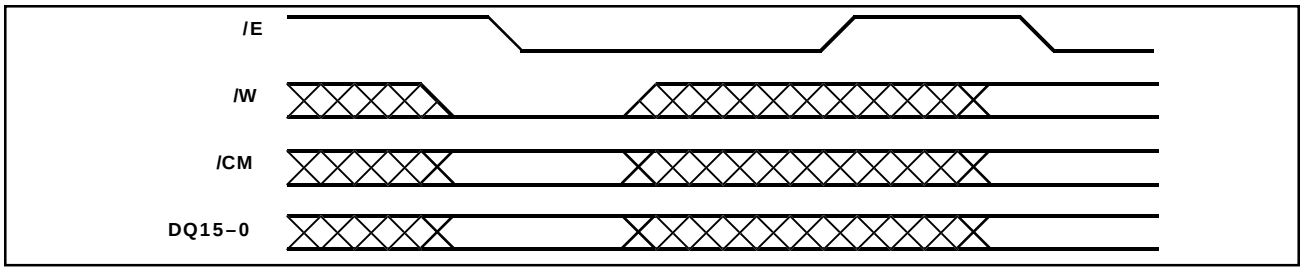


Figure 4: Write Cycle

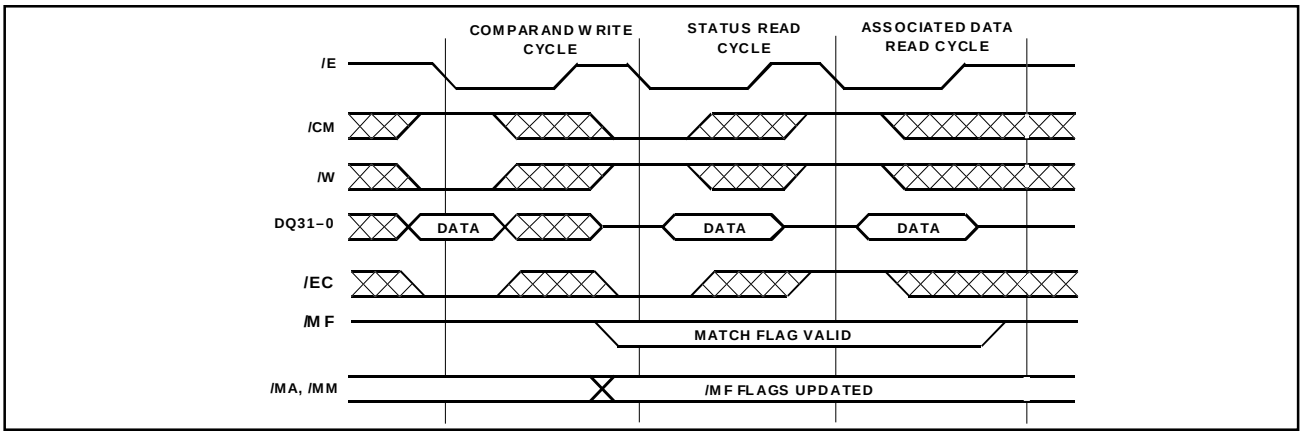


Figure 5: Cycle to Cycle Timing Example

indicated by Table 6b on page 12. A single-chip system does not require daisy-chained match flag operation, hence /EC could be tied HIGH and the /MA pin or flag in the Status register used instead of /MF, allowing access to the device regardless of the match condition.

The minimum timings for the /E control signal are given in the Switching Characteristics section on page 27. Note that at minimum timings the /E signal is non-symmetrical and that different cycle types have different timing requirements, as given in Table 9 on page 22.

COMPARE OPERATIONS

During a Compare operation, the data in the Comparand register is compared to all locations in the Memory array simultaneously. Any mask register used during compares must be selected beforehand in the Control register. There are two ways compares are initiated: Automatic compare and Forced compare.

Automatic compares perform a compare of the contents of the Comparand register against Memory locations that are tagged as "Valid," and occur whenever the following happens:

- The Destination Segment counter in the Segment Control register reaches its end limit during writes to the Comparand or mask registers.

OPERATIONAL CHARACTERISTICS *Continued*

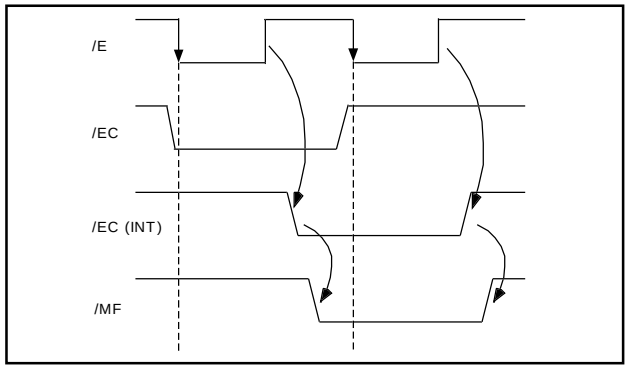


Figure 6: /EC(Int) Timing Diagram

- After a command write of a TCO CT is executed (except for a software reset), so that a compare is executed with the new settings of the Control register.

Forced compares are initiated by CMP instructions using one of the four validity conditions, V, R, S, and E. The forced compare against "Empty" locations automatically masks all 64 bits of data to find all locations with the validity bits set to "Empty", while the other forced compares are only masked as selected in the Control register.

VERTICAL CASCADING

LANCAM WLs can be vertically cascaded to increase system depth. Through the use of flag daisy-chaining, multiple devices will respond as an integrated system. The flag daisy chain allows all commands to be issued globally, with a response only in the device containing the Highest-Priority Matching or Next Free location. When connected in a daisy chain, the last device's Full flag and Match flag accurately report the condition for the whole string. A system in which LANCAM WLs are vertically cascaded using daisy-chaining of the flags is shown in Figure 1a on page 7.

To operate the daisy chain, the Device Select registers are set to FFFFH to enable all devices to execute Command Write and Data Write cycles. In normal operation, read cycles are enabled from the device with the highest-priority match by locking the daisy chain (see "Locked Daisy Chain" section). An individual device in the chain may be targeted for a read or write operation by temporarily setting the Device Select registers to the page address of the target device. Setting the Device Select registers back to FFFFH restores the operation of the entire daisy chain.

Match Flag Cascading

The Match Flag daisy chain cascading is used for three purposes: first, to allow operations on Highest-priority Match addresses to be issued globally over the whole string; second, to provide a system wide match flag; third, to lock out all devices except the one with the Highest-Priority match for instructions such as Status reads after a match. The Match flag logic causes only the highest-priority device to operate on its Highest-priority Match location while devices with lower-priority matches ignore Highest-priority Match operations. The lockout feature is enabled by the match flag cascading and the use of the /EC control signal, as shown in Tables 6a and 6b on page 12.

The ripple delay of the flags when connected in a daisy chain may require the extension of the /E HIGH time until the logic in all devices has settled out. In a string of "n" devices, the /E HIGH time should be greater than:

$$tEHMFV + (n-2) \cdot tMIVMFV$$

If the last device's Match flag is required by external logic or a state machine before the start of the next CAM cycle, one additional tMIVMFV should be added to the /E HIGH time along any required setup time and delays for the external logic.

Locked Daisy Chain

In a locked daisy chain, the highest-priority device is the one with /MI HIGH and /MF LOW. In Standard mode, only this device will respond to command and data reads and writes, until the daisy chain has been unlocked by taking /EC HIGH. This allows reading the associated data field from only the Highest-Priority Match location anywhere in a string of devices, or the Match address from the Status register of the device with the match. It also permits updating the entry stored at the Highest-Priority Match location. In Enhanced mode, devices are enabled to respond to some command and data writes, as noted in Tables 6a and 6b on page 12, but not command and data reads.

Table 6a (Standard mode) and Table 6b (Enhanced mode) on page 12 show when a device will respond to reads or writes and when it will not, based on the state of /EC(int), the internal match condition, and other control inputs. /EC is latched by the falling edge of /E. /EC(int) is registered from the latched /EC signal off the rising edge of /E, so it controls what happens in the next cycle, as shown in Figure 6. When /EC is first taken LOW in a string of LANCAM devices (and assuming the Device Select registers are set to FFFFH), all devices will respond to that command write or data write.

From then on the daisy chain will remain locked in each subsequent cycle as long as /EC is held LOW on the falling edge of /E in the current cycle. When the daisy chain is locked in Standard mode, only the Highest-Priority Match device will respond (See Case 6 of Table 6a on page 12). If, for example, all of the CAM memory locations were empty, there would be no match, and /MF would stay HIGH. Since none of the devices could then be the Highest-Priority Match device, none will respond to reads or writes until the daisy chain is unlocked by taking /EC HIGH and asserting /E for a cycle.

If there is a match between the data in the Comparand register and one or more locations in memory, then only the Highest-Priority Match device will respond to any cycle, such as an associated data or Status Register read. If there is not a match, then a NOP with /EC HIGH needs to be inserted before issuing any new instructions, such as Write to Next Free Address instruction to learn the data. Since Next Free operations are controlled by the /FI–/FF daisy chain, only the device with the first empty location will respond. If an instruction is used to unlock the daisy chain it will work only on the Highest-Priority Match device, if one exists. If none exists, the instruction will have no effect except to unlock the daisy chain. To read the Status registers of specific devices when there is no match requires the use of the TCO DS command to set DS=PA of each device. Single chip systems can tie /EC HIGH and read the Status register or the /MA and /MM pins to monitor match conditions, as the daisy chain lockout feature is not needed in this configuration. This removes the need to insert a NOP in the case of a no-match.

When the Control register is set to Enhanced mode, you can continue to write data to the Comparand register or issue a Move to Next Free Address instruction without first having to issue a NOP with /EC HIGH to unlock the daisy chain after a Compare cycle with no match, as indicated in cases 4 and 5 of Table 6b on page 12. In Enhanced mode, data write cycles as well as command write cycles are enabled in all devices even when /EC is LOW. Exceptions are data writes, moves, or VBC instructions involving HM, which occur only in the device with the highest match; and data writes or move instructions involving NF, which occur only in the device with /FI LOW and /FF HIGH. Enhanced mode speeds up system performance by eliminating the need to unlock the daisy chain before Command or Data Write cycles.

Full Flag Cascading

The Full Flag daisy chain cascading is used for three purposes: first, to allow instructions that address Next Free locations to operate globally; second, to provide a system wide Full flag; third, to allow the loading of the Page Address registers during initialization using the SFF instruction. The full flag logic causes only the device containing the first empty location to respond to Next Free instructions such as "MOV NF,CR,V", which will move the contents of the Comparand register to the first empty location in a string of devices and set that location Valid, so it will be available for the next automatic compare. With devices connected as in Figure 1a on page 7, the /FF output of the last device in a string provides a full indication for the entire string.

IEEE 802.3/802.5 Format Mapping

To support the symmetrical mapping between the address formats of IEEE 802.3 and IEEE 802.5, the LANCAM WL provides a bit translation facility. Formally expressed, the nth input bit, D(n), maps to the xth output bit, Q(x), through the following expressions:

$$D(n) = Q(7-n) \text{ for } 0 \le n \le 7,$$
$$D(n) = Q(23-n) \text{ for } 8 \le n \le 15$$
$$D(n) = Q(39-n) \text{ for } 16 \le n \le 23$$
$$D(n) = Q(55-n) \text{ for } 24 \le n \le 31$$

Control Register bits CT10 and CT9 select whether to persistently translate, or persistently not to translate, the data written onto the 64-bit internal bus. The default condition after a Reset command is not to translate the incoming data. Figure 2 on page 10 shows the bit mapping between the two formats.

IEEE 1149.1 Standard JTAG Test Access Port

The LANCAM WL has an IEEE 1149.1 Standard JTAG Test Access port with full boundary-scan architecture. Please refer to the IEEE Standard for information on using the JTAG functions. The JTAG Device identification for each device is shown in Table 7a and 7b and the functions that are possible are shown in Table 7c.

INITIALIZING THE LANCAM WL

Initialization of the LANCAM WL is required to configure the various registers on the device. Since a Control register reset establishes the operating conditions shown in Table 5 on page 10, restoration of operating conditions better suited for the application may be required after a reset, whether using the Control Register reset, or the /RESET pin. When the device powers up, the memory and registers are in an unknown state, so the /RESET pin must be asserted to place the device in a known state.

OPERATIONAL CHARACTERISTICS *Continued*

Binary	0001	0111	0100	0011	0010	0001	0011	0011
HEX	1	7	4	3	2	1	3	3
Description	Version	MU9C7485		32K		MANUFACTURER ID		

Table 7a: MU9C7485 Identification Code

Binary	0001	0110	0100	0001	0110	0001	0011	0011
HEX	1	6	4	1	6	1	3	3
Description	Version	MU9C6485		16K		MANUFACTURER ID		

Table 7b: MU9C6485 Identification Code

EXE TEST	0000
BYPASS	1111
SAMPLE	0001
ID CODE	0010
CLAMP	0100
HIGH-Z	0011
INTEST	0101

Table 7c: JTAG Codes

Cycle Type	Op-Code	Data Bus		Comments	Notes
		DQ31–16	DQ15–0		
Command Write	TCO DS	0A28H	FFFFH	Target Device Select register and disable local device selection	
Command Write	TCO CT	0A00H	0000H	Target Control register and reset	1
Command Write	TCO PA	0A08H	nnnnH	Target Page Address register and set page for cascaded operation	2
Command Write	SFF • •	0700H	X	Set Full flag; allows access to next device (repeat previous cycle plus this one for each device in chain)	2
Command Write	TCO CT	0A00H	0000H	Target Control register and reset Full flags, but not Page address	
Command Write	TCO CT	0A00H	8080H	Target Control register and give initial values	3
Command Write	TCO SC	0A10H	2808H	Target Segment counter and set destination to only use upper segment and source to only use lower segment	
Command Write	SPS M@HM	0005H	X	Set Persistent source to Memory at the Highest-Priority match	4

Notes:

1. Toggling the /RESET pin generates the same effect as this reset of the Control register, but good programming practice dictates a software reset for initialization to account for all possible prior conditions.
2. This instruction may be omitted for a single LANCAM WL application. The last SFF will cause the /FF pin in the last chip in a daisy chain to go LOW. In a daisy chain, DS needs to be set equal to PA to read out a particular chip prior to a match condition.
3. Typical LANCAM WL control environment: Enable match flag; Enable full flag; 32 CAM bits/32 RAM bits; Disable comparison masking; and Enable address increment. This example translates to 8080H. See Table 10 on page 23 for Control Register bit assignments.
4. Setting the persistent source to the Memory at Highest-Priority match allows a compare operation to be followed by a read of the associated data when a match is found. Note that the persistent destination is set to the Comparand register by the reset.

Table 8: Example Initialization Routine

OPERATIONAL CHARACTERISTICS *Continued*

Setting Page Address Register Values

In a vertically cascaded system, the user must set the individual Page Address registers to unique values by using the Page Address initialization mechanism. Each Page Address register must contain a unique value to prevent bus contention. This process allows individual device selection. The Page Address register initialization works as follows: Writes to Page Address registers are only active for devices with /FI LOW and /FF HIGH. At initialization, all devices are empty, thus the top device in the string will respond to a TCO PA instruction, and load its PA register. To advance to the next device in the string, a Set Full Flag (SFF) instruction is used, which is also only active for the device with /FI LOW and /FF HIGH. The SFF instruction changes the first device's /FF to LOW, although the device really is empty, which allows the next device in the string to respond to the TCO PA instruction and load its PA register. The initialization proceeds through the chain in a similar manner filling all the PA registers in turn. Each device must have a unique Page Address value stored in its PA register, or contention will result. After all the PA registers are filled, the entire string is reset through the Control register, which does not change the values stored in the individual PA registers. After the reset, the Device Select registers are usually set to FFFFH to enable operation, in Case 1 of Table 6a on page 12. The Control registers and the Segment Control registers are then set to their normal operating values for the application.

Vertically Cascaded System Initialization

Table 8 shows an example of code that initializes a daisy-chained string of LANCAM WL devices. The initialization example shows how to set the Page Address registers of each of the devices in the chain through the use of the Set Full Flag instruction, and how the Control registers and Segment counters of all the LANCAM WL devices are set for a typical application. Each Page Address register must contain a unique value (not FFFFH) to prevent bus contention.

For typical daisy chain operation, data is loaded into the Comparand registers of all the devices in a string simultaneously by setting DS=FFFFH. Since reading is prohibited when DS=FFFFH except for the device with a match, for a diagnostic operation you need to select a specific device by setting DS=PA for the desired device to be able to read from it. Refer to Tables 6a and 6b on page 12 for preconditions for reading and writing.

Initialization for a single LANCAM WL is similar. The Device Select register in this case is usually set to equal the Page Address register for normal operations. Also, the dedicated /MA flag output can be used instead of /MF, allowing /EC to be tied HIGH.

INSTRUCTION SET DESCRIPTIONS§

Instruction: Select Persistent Source (SPS)
Binary Op-Code: 0000 f000 0000 0sss*

f	**Address Field flag†**
sss	**Selected source**

This instruction selects a persistent source for data reads, until another SPS instruction changes it or a reset occurs. The default source after reset for Data Read cycles is the Comparand register. Setting the persistent source to M@aaaH loads the Address register with "aaaH," and the first access to that persistent source will be at aaaH, after which the AR value increments or decrements as set in the Control register. The SPS M@[AR] instruction does the same except the current Address Register value is used.

Instruction: Select Persistent Destination (SPD)
Binary Op-Code: 0000 f001 mmdd dvvv*

f	**Address Field flag†**
mm	**Mask Register select**
ddd	**Selected destination**
vvv	**Validity setting for Memory Location destinations**

This instruction selects a persistent destination for data writes, which remains until another SPD instruction changes it or a reset occurs. The default destination for Data Write cycles is the Comparand register after a reset. When the destination is the Comparand register or the memory array, the data written may be masked by either Mask Register 1 or Mask Register 2, so that only destination bits corresponding to bits in the mask register

INSTRUCTION SET DESCRIPTIONS§ *Continued*

set to 0 will be modified. An automatic compare will occur after writing the last segment of the Comparand or mask registers, but not after writing to memory. Setting the persistent destination to M@aaaH loads the Address register with "aaaH," and the first access to that persistent destination will be at aaaH, after which the AR value increments or decrements as set in the Control register. The SPD M@[AR] instruction does the same except the current Address Register value is used.

Instruction: Temporary Command Override (TCO)
Binary Op-Code: 0000 f010 00dd d000*

f	**Address Field flag†**
ddd	**Register selected as source or destination for only the next Command Read or Write cycle**

The TCO instruction temporarily redirects the DQ bus for register access. If f=1, a register write will be performed with the data on DQ15–0. If f=0, a subsequent Command Read cycle reads the register contents through DQ15–0. During register reads, DQ31–16 will contain the upper 16-bits of the Status register, except in the case of a Page Address register read where these bits are 0s. After the access, subsequent Command Read or Write cycles revert to reading the Status register and writing to the Instruction decoder. All registers except the Status, NF, PS, and PD are available for write access. All registers are available for read access. The complete Status register is only available through a non-TCO Command Read access. Reading the PS register also outputs the Device ID on bits 15–4, as shown in Table 14 on page 24.

Instruction: Data Move (MOV)
Binary Op-Code: 0000 f011 mmdd dsss or 0000 f011 mmdd dvss*

f	**Address Field flag†**
mm	**Mask Register select**
ddd	**Destination of data**
sss	**Source of data**
v	**Validity setting if destination is a Memory location**

The MOV instruction performs a 64-bit move of the data in the selected source to the selected destination. If the source or destination is aaaH, the Address register is set to "aaaH." For MOV instructions to or from aaaH or [AR], the Address register will increment or decrement from that value after the move completes, as set in the Control register. Data transfers between the Memory array and the Comparand register may be masked by either Mask Register 1 or Mask Register 2, in which case, only those bits in the destination which correspond to bits in the selected mask register set to 0 will be changed. A Memory location used as a destination for a MOV instruction may be set to Valid or left unchanged. If the source and destination are the same register, no net change occurs (a NOP).

Instruction: Validity Bit Control (VBC)
Binary Op-Code: 0000 f100 00dd dvvv*

f	**Address Field flag†**
ddd	**Destination of data**
vvv	**Validity setting for Memory location**

The VBC instruction sets the Validity bits at the selected memory locations to the selected state. This feature can be used to find all valid entries by using a repetitive sequence of CMP V through a mask of all 1s followed by a VBC HM, S. If the VBC target is aaaH, the Address register is set to "aaaH." For VBC instructions to or from aaaH or [AR], the Address register will increment or decrement from that value after the operation completes, as set in the Control register.

Instruction: Compare (CMP)
Binary Op-Code: 0000 0101 0000 0vvv*

vvv	**Validity condition**

A CMP V, S, or R instruction forces a Comparison of Valid, Skipped, or Random entries against the Comparand register through a mask register, if one is selected. During a CMP E instruction, the compare is only done on the Validity bits and all data bits are automatically masked.

Instruction: Special Instructions
Binary Op-Code: 0000 0110 00dd drrr*

ddd	**Target resource**
rrr	**Operation**

These instructions are a special set for the LANCAM WLs to accommodate the added features over the MU9C1485. Two alternate sets of configuration registers can be selected by using the Select Foreground and Select Background Registers instructions. These registers are the Control, Segment Control, Address, Mask Register 1, and the PS and PD registers. An RSC instruction resets the Segment Control register count values for both the Destination and Source counters to the original Start limits. The Shift instructions shift the designated register one bit right or left. The right and left limits for shifting are determined by the CAM/RAM partitioning set in the Control register. The Comparand register is a barrel-shifter, and for the example of a device set to 64 bits of CAM executing a Shift Comparand Right instruction, bit 0 is moved to bit 63, bit 1 is moved to bit 0, and bit 63 is moved to bit 62. For a Shift Comparand Left instruction, bit 63 is moved to bit 0, bit 0 is moved to

INSTRUCTION SET DESCRIPTIONS§ *Continued*

bit 1, and bit 62 is moved to bit 63. MR2 acts as a sliding mask, where for a Shift Right instruction bit 1 is moved to bit 0, while bit 0 "falls off the end," and bit 63 is replicated to bit 62. For a Shift Mask Left instruction, bit 0 is replicated to bit 1, bit 62 is moved to bit 63, and bit 63 "falls off the end." With shorter width CAM fields, the bit limits on the right or left move to match the width of CAM field.

Instruction: Set Full Flag (SFF)
Binary Op-Code: 0000 0111 0000 0000*
The SFF instruction is a special instruction used to force the Full flag LOW to permit setting the Page Address register in vertically cascaded systems.

Instruction: No Operation (NOP)
Binary Op-Code: 0000 0011 0000 0000
The NOP (No-OP) belongs to the MOV instructions, where a register is moved to itself. No change occurs within the device. This instruction is useful in unlocking the daisy chain in Standard mode.

Notes:
§ Instruction cycle lengths given in Table 9 on page 22.
* Instruction Op-Codes are loaded on the DQ31–16 lines.
† If f=1, the instruction requires an absolute address (or register contents for TCOs) to be supplied onthe DQ15–0 lines. Supplied addresses will update the Address register to the "aaaH" value supplied. After an operation involving M@[AR] or M@aaaH, the Address register will be incremented or decremented depending on the setting in the Control register.

INSTRUCTION SET SUMMARY

MNEMONIC FORMAT
INS dst,src[msk],val

INS: Instruction mnemonic
dst: Destination of the data
src: Source of the data
msk: Mask register used
val: Validity condition set at the location written

Instruction: Select Persistent Source

Operation	Mnemonic	Op-Code
Comparand Register	SPS CR	0000H
Mask Register 1	SPS MR1	0001H
Mask Register 2	SPS MR2	0002H
Memory Array at Addr. Reg.	SPS M@[AR]	0004H
Memory Array at Address	SPS M@aaaH	0804H
Mem. at Highest-Prio. Match	SPS M@HM	0005H

Instruction: Select Persistent Destination

Operation	Mnemonic	Op-Code
Comparand Register	SPD CR	0100H
Masked by MR1	SPD CR[MR1]	0140H
Masked by MR2	SPD CR[MR2]	0180H
Mask Register 1	SPD MR1	0108H
MaskRegister 2	SPD MR2	0110H
Mem. at Addr. Reg. set Valid	SPD M@[AR],V	0124H
Masked by MR1	SPD M@[AR][MR1],V	0164H
Masked by MR2	SPD M@[AR][MR2],V	01A4H
Mem. at Addr. Reg. set Empty	SPD M@[AR],E	0125H
Masked by MR1	SPD M@[AR][MR1],E	0165H
Masked by MR2	SPD M@[AR][MR2],E	01A5H

Instruction: Select Persistent Destination *Cont.*

Operation	Mnemonic	Op-Code
Mem. at Addr. Reg. set Skip	SPD M@[AR],S	0126H
Masked by MR1	SPD M@[AR][MR1],S	0166H
Masked by MR2	SPD M@[AR][MR2],S	01A6H
Mem. at Addr. Reg. set Random	SPD M@[AR],R	0127H*
Masked by MR1	SPD M@[AR][MR1],R	0167H*
Masked by MR2	SPD M@[AR][MR2],R	01A7H*
Memory at Address set Valid	SPD M@aaaH,V	0924H*
Masked by MR1	SPD M@aaaH[MR1],V	0964H*
Masked by MR2	SPD M@aaaH[MR2],V	09A4H
Memory at Addr. set Empty	SPD M@aaaH,E	0925H
Masked by MR1	SPD M@aaaH[MR1],E	0965H
Masked by MR2	SPD M@aaaH[MR2],E	09A5H
Memory at Address set Skip	SPD M@aaaH,S	0926H
Masked by MR1	SPD M@aaaH[MR1],S	0966H
Masked by MR2	SPD M@aaaH[MR2],S	09A6H
Mem. at Address set Random	SPD M@aaaH,R	0927H
Masked by MR1	SPD M@aaaH[MR1],R	0967H
Masked by MR2	SPD M@aaaH[MR2],R	09A7H
Mem. at Highest-Prio. Match, Valid	SPD M@HM,V	012CH
Masked by MR1	SPD M@HM[MR1],V	016CH
Masked by MR2	SPD M@HM[MR2],V	01ACH
Mem. at Highest-Prio. Match, Emp.	SPD M@HM,E	012DH
Masked by MR1	SPD M@HM[MR1],E	016DH
Masked by MR2	SPD M@HM[MR2],E	01ADH
Mem. at Highest-Prio. Match, Skip	SPD M@HM,S	012EH
Masked by MR1	SPD M@HM[MR1],S	016EH
Masked by MR2	SPD M@HM[MR2],S	01AEH

INSTRUCTION SET SUMMARY *Continued*

Instruction: Select Persistent Destination *Cont.*

Operation	Mnemonic	Op-Code
Mem. at High.-Prio. Match, Random	SPD M@HM,R	012FH
Masked by MR1	SPD M@HM[MR1],R	016FH
Masked by MR2	SPD M@HM[MR2],R	01AFH
Mem. at Next Free Addr., Valid	SPD M@NF,V	0134H
Masked by MR1	SPD M@NF[MR1],V	0174H
Masked by MR2	SPD M@NF[MR2],V	01B4H
Mem. at Next Free Addr., Empty	SPD M@NF,E	0135H
Masked by MR1	SPD M@NF[MR1],E	0175H
Masked by MR2	SPD M@NF[MR2],E	01B5H
Mem. at Next Free Addr., Skip	SPD M@NF,S	0136H
Masked by MR1	SPD M@NF[MR1],S	0176H
Masked by MR2	SPD M@NF[MR2],S	01B6H
Mem. at Next Free Addr., Random	SPD M@NF,R	0137H
Masked by MR1	SPD M@NF[MR1],R	0177H
Masked by MR2	SPD M@NF[MR2],R	01B7H

Instruction: Temporary Command Override

Operation	Mnemonic	Op-Code
Control Register	TCO CT	0n00H
Page Address Register	TCO PA	0n08H
Segment Control Register	TCO SC	0n10H
Read Next Free Address	TCO NF	0218H
Address Register	TCO AR	0n20H
Device Select Register	TCO DS	0n28H
Read Persistent Source	TCO PS	0230H
Read Persistent Destination	TCO PD	0238H

*Note: n = 2 for register read access
n = A for register write access

Instruction: Data Move

Operation	Mnemonic	Op-Code
Comparand Register from:		
No Operation	NOP	0300H
Mask Register 1	MOV CR,MR1	0301H
Mask Register 2	MOV CR,MR2	0302H
Memory at Address Reg.	MOV CR,[AR]	0304H
Masked by MR1	MOV CR,[AR][MR1]	0344H
Masked by MR2	MOV CR,[AR][MR2]	0384H
Memory at Address	MOV CR,aaaH	0B04H
Masked by MR1	MOV CR,aaaH[MR1]	0B44H
Masked by MR2	MOV CR,aaaH[MR2]	0B84H
Mem. at Highest-Prio. Match	MOV CR,HM	0305H
Masked by MR1	MOV CR,HM[MR1]	0345H
Masked by MR2	MOV CR,HM[MR2]	0385H
Mask Register 1 from:		
Comparand Register	MOV MR1,CR	0308H
No Operation	NOP	0309H
Mask Register 2	MOV MR1,MR2	030AH
Memory at Address Reg.	MOV MR1,[AR]	030CH
Memory at Address	MOV MR1,aaaH	0B0CH
Mem. at Highest-Prio. Match	MOV MR1,HM	030DH

Instruction: Data Move *Continued*

Operation	Mnemonic	Op-Code
Mask Register 2 from:		
Comparand Register	MOV MR2,CR	0310H
Mask Register 1	MOV MR2,MR1	0311H
No Operation	NOP	0312H
Memory at Address Reg.	MOV MR2,[AR]	0314H
Memory at Address	MOV MR2,aaaH	0B14H
Mem. at Highest-Prio. Match	MOV MR2,HM	0315H
Memory at Address Register, No Change to Validity bits, from:		
Comparand Register	MOV [AR],CR	0320H
Masked by MR1	MOV [AR],CR[MR1]	0360H
Masked by MR2	MOV [AR],CR[MR2]	03A0H
Mask Register 1	MOV [AR],MR1	0321H
Mask Register 2	MOV [AR],MR2	0322H
Memory at Address Register, Location set Valid, from:		
Comparand Register	MOV [AR],CR,V	0324H
Masked by MR1	MOV [AR],CR[MR1],V	0364H
Masked by MR2	MOV [AR],CR[MR2],V	03A4H
Mask Register 1	MOV [AR],MR1,V	0325H
Mask Register 2	MOV [AR],MR2,V	0326H
Memory at Address, No Change to Validity bits, from:		
Comparand Register	MOV aaaH,CR	0B20H
Masked by MR1	MOV aaaH,CR[MR1]	0B60H
Masked by MR2	MOV aaaH,CR[MR2]	0BA0H
Mask Register 1	MOV aaaH,MR1	0B21H
Mask Register 2	MOV aaaH,MR2	0B22H
Memory at Address, Location set Valid, from:		
Comparand Register	MOV aaaH,CR,V	0B24H
Masked by MR1	MOV aaaH,CR[MR1],V	0B64H
Masked by MR2	MOV aaaH,CR[MR2],V	0BA4H
Mask Register 1	MOV aaaH,MR1,V	0B25H
Mask Register 2	MOV aaaH,MR2,V	0B26H
Memory at Highest-Priority Match, No Change to Validity bits, from:		
Comparand Register	MOV HM,CR	0328H
Masked by MR1	MOV HM,CR[MR1]	0368H
Masked by MR2	MOV HM,CR[MR2]	03A8H
Mask Register 1	MOV HM,MR1	0329H
Mask Register 2	MOV HM,MR2	032AH
Memory at Highest-Priority Match, Location set Valid, from:		
Comparand Register	MOV HM,CR,V	032CH
Masked by MR1	MOV HM,CR[MR1],V	036CH
Masked by MR2	MOV HM,CR[MR2],V	03ACH
Mask Register 1	MOV HM,MR1,V	032DH
Mask Register 2	MOV HM,MR2,V	032EH
Memory at Next Free Address, No Change to Validity bits, from:		
Comparand Register	MOV NF,CR	0330H
Masked by MR1	MOV NF,CR[MR1]	0370H
Masked by MR2	MOV NF,CR[MR2]	03B0H
Mask Register 1	MOV NF,MR1	0331H
Mask Register 2	MOV NF,MR2	0332H

INSTRUCTION SET SUMMARY *Continued*

Instruction: Data Move *Continued*

Operation	Mnemonic	Op-Code
Memory at Next Free Address, Location set Valid, from:		
Comparand Register	MOV NF,CR,V	0334H
Masked by MR1	MOV NF,CR[MR1],V	0374H
Masked by MR2	MOV NF,CR[MR2],V	03B4H
Mask Register 1	MOV NF,MR1,V	0335H
Mask Register 2	MOV NF,MR2,V	0336H

Instruction: Validity Bit Control

Operation	Mnemonic	Op-Code
Set Validity bits at Address Register		
Set Valid	VBC [AR],V	0424H
Set Empty	VBC [AR],E	0425H
Set Skip	VBC [AR],S	0426H
Set Random Access	VBC [AR],R	0427H
Set Validity bits at Address		
Set Valid	VBC aaaH,V	0C24H
Set Empty	VBC aaaH,E	0C25H
Set Skip	VBC aaaH,S	0C26H
Set Random Access	VBC aaaH,R	0C27H
Set Validity bits at Highest-Priority Match		
Set Valid	VBC HM,V	042CH
Set Empty	VBC HM,E	042DH
Set Skip	VBC HM,S	042EH
Set Random Access	VBC HM,R	042FH

Instruction: Validity Bit Control *Continued*

Operation	Mnemonic	Op-Code
Set Validity bits at All Matching Locations		
Set Valid	VBC ALM,V	043CH
Set Empty	VBC ALM,E	043DH
Set Skip	VBC ALM,S	043EH
Set Random Access	VBC ALM,R	043FH

Instruction: Compare

Operation	Mnemonic	Op-Code
Compare Valid Locations	CMP V	0504H
Compare Empty Locations	CMP E	0505H
Compare Skipped Locations	CMP S	0506H
Comp. Random Access Locations	CMP R	0507H

Instruction: Special Instructions

Operation	Mnemonic	Op-Code
Shift Comparand Right	SFT CR, R	0600H
Shift Comparand Left	SFT CR, L	0601H
Shift Mask Register 2 Right	SFT M2, R	0610H
Shift Mask Register 2 Left	SFT M2, L	0611H
Select Foreground Registers	SFR	0618H
Select Background Registers	SBR	0619H
Reset Seg. Cont. Reg. to Initial Val.	RSC	061AH

Instruction: Miscellaneous Instructions

Operation	Mnemonic	Op-Code
No Operation	NOP	0300H
Set Full Flag	SFF	0700H

CYCLE LENGTH	CYCLE TYPE			
	Command Write	**Command Read**	**Data Write**	**Data Read**
Short	MOV reg, reg (except -70) TCO reg (except CT) TCO CT (non-reset, HMA invalid) SPS, SPD, SFR SBR, RSC, NOP		Comparand register (not last segment) Mask register (not last segment)	
Medium	MOV reg, reg (-70) MOV reg, mem TCO CT (reset) VBC (NFA invalid) SFT	Status register or 16-bit register	Memory array (NFA invalid)	Comparand register Mask register Memory array
Long	MOV mem, reg TCO CT (non-reset, HMA valid) CMP SFF VBC (NFA valid)		Memory array (NFA valid) Comparand register (last segment) Mask register (last segment)	

Note: The specific timing requirements for Short, Medium, and Long cycles are given in the Switching Characteristics section under the tELEH parameter. For two cycle TCO reads of a register's contents, the first cycle (Command Write TCO) is short, and the second cycle (Command read) is medium.

Table 9: Instruction Cycle Lengths

REGISTER BIT ASSIGNMENTS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	Match Flag		Full Flag		Translation		CAM/RAM Part.			Comp. Mask		AR Inc/Dec		Mode	
R E S E T = 0	Enable =00 Disable = 01 No Change = 11		Enable = 00 Disable = 01 No Change = 11		Input Not Translated = 00 Input Translated = 01 No Change = 11		64 CAM/0 RAM = 000 48 CAM/16 RAM = 001 32 CAM/32 RAM = 010 16 CAM/48 RAM = 011 48 RAM/16 CAM = 100 32 RAM/32 CAM = 101 16 RAM/48 CAM = 110 No Change = 111			None = 00 MR1 = 01 MR2 = 10 No Change = 11		Increment = 00 Decrement = 01 Disable = 10 No Change = 11		Standard Mode = 00 Enhanced Mode = 01 Reserved = 10 No Change = 11	

Note: D15 reads back as 0.

Table 10: Control Register Bit Assignments

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0		**0**			**0**		**0**			**0**			**0**	
Set Dest. Seg. Limits = 0 No Chng. = 1	Reserved	Dest. Count Start Limit	Reserved	Dest. Count End Limit	Set Source Seg. Limits = 0 No Chng. = 1	Reserved	Src. Count Start Limit	Reserved	Src. Count End Limit	Load Dest. Seg. Count = 0 No Chng. = 1	Reserved	Dest. Seg. Count Value	Load Src. Seg. Count = 0 No Chng. = 1	Reserved	Src. Seg. Count Value

Note: D15, D10, D5, and D2 read back as 0s. Reserved locations D14, D12, D9, D7, D4, and D1 should always be set to 0.

Table 11: Segment Control Register Bit Assignments

REGISTER BIT ASSIGNMENTS *Continued*

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
7485	/MA	/MM	/FL	Skip	Empty	Page Address Bits, PA11–1										
6485	/MA	/MM	/FL	Skip	Empty	Page Address Bits, PA12–2										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7485	PA0	Next Free Address, NF14–0														
6485	PA1–0	Next Free Address, NF13–0														

Note: The Next Free Address register is read only, and is accessed by performing a Command Read cycle immediately following a TCO NF instruction.

Table 12: Next Free Address Register Bit Assignments

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
7485	/MA	/MM	/FL	Skip	Empty	Page Address Bits, PA11–1										
6485	/MA	/MM	/FL	Skip	Empty	Page Address Bits, PA12–2										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7485	PA0	Match Address, AM14–0														
6485	PA1–0	Match Address, AM13–0														

Note: The Status register is read only, and is accessed by performing a Command Read cycle.

Table 13: Status Register Bit Assignments

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
7485	/MA	/MM	/FL	Skip	Empty	Page Address Bits, PA11–1										
6485	/MA	/MM	/FL	Skip	Empty	Page Address Bits, PA12–2										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7485	Device ID = 745 H												PS			
6485	Device ID = 645 H												PS			

Note: The Persistent Source register is read only, and is accessed by performing a Command Read cycle immediately following a TCO PS instruction.

Table 14: Persistent Source Register Bit Assignments

OPERATIONAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 4.6 Volts
Voltage on all other pins	-0.5 to VCC +0.5 Volts (-2 Volts for 10 ns, measured at the 50% point)
Temperature under bias	-55°C to 125°C
Storage Temperature	-55°C to 125°C
DC Output Current	20 mA (per output, one at a time, one second duration.

Stresses exceeding those listed under Absolute Maximum Ratings may include failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages referenced to GND.

OPERATING CONDITIONS (voltages referenced to GND at the device pin)

Symbol	Parameter		Min	Typical	Max	Units	Notes
V_{CC}	Operating Supply Voltage		3.0	3.3	3.6	Volts	
V_{IH}	Input Voltage Logic 1		2.0		V_{CC} + 0.5	Volts	
V_{IL}	Input Voltage Logic 0		-0.5		0.8	Volts	1, 2
T_A	Ambient Operating Temperature	Commercial	0		70	°C	Still Air
		Industrial	-40		85	°C	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typical	Max	Units	Notes
I_{CC}	Average Power Supply Current	7485		TBD	TBD	mA	tELEL=tELEL(min.); 9
		6485		TBD	TBD	mA	
$I_{CC(SB)}$	Stand-by Power Supply Current				2	mA	
V_{OH}	Output Voltage Logic “1”		2.4			Volts	I_{OH} = -2.0mA
V_{OL}	Output Voltage Logic “0”				0.4	Volts	I_{OL} = 4.0mA
I_{IZ}	Input Leakage Current	/RESET	6	9	12	Kohms	V_{IN} = 0 V
		Others	-2		+2	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OZ}	Output Leakage Current		-10		10	µA	$V_{SS} \le V_{OUT} \le V_{CC;}$ DQ_N = High Impedance

CAPACITANCE

Symbol	Parameter	Max	Units	Notes
C_{IN}	Input Capacitance	6	pF	f = 1 MHz, V_{IN} = 0 V
C_{OUT}	Output Capacitance	7	pF	f = 1 MHz, V_{OUT} = 0 V

OPERATIONAL CHARACTERISTICS *Continued*

AC TEST CONDITIONS

Input Signal Transitions	0.0 Volts to 3.0 Volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 Volts
Output Timing Reference Level	1.5 Volts

SWITCHING TEST FIGURES

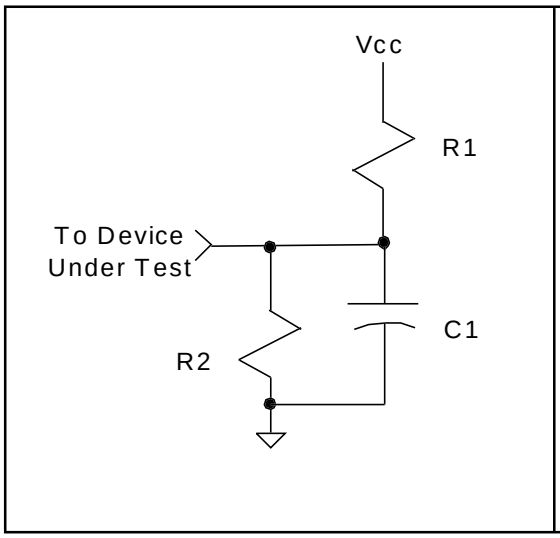


Figure7: AC Test Load

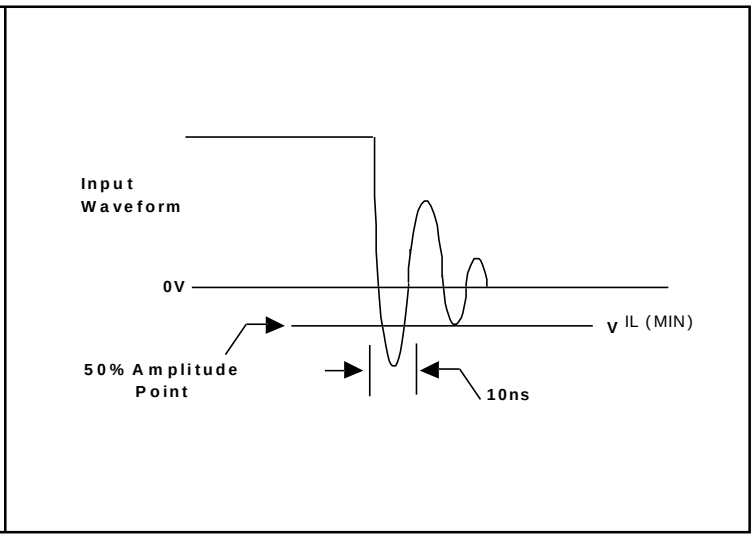


Figure 8: Input Signal Waveform

SWITCHING TEST FIGURE COMPONENT VALUES

Parameter		Value	Units
VCC		3.3	Volts
R1		635	Ohm
R2		702	Ohm
C1 (Includes jig)	Test Load A	30	pF
	Test Load B	5	pF

OPERATIONAL CHARACTERISTICS *Continued*

SWITCHING CHARACTERISTICS *(see Note 3)*

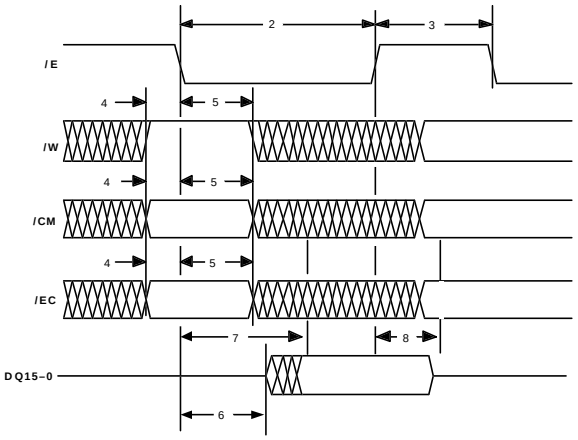
		Cycle Time	-50		-70		-90		-12		
No	**Symbol**	**Parameter (all times in nanoseconds)**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Notes**
1	t_{ELEL}	Chip Enable Compare Cycle Time	50		70		90		120		
2	t_{ELEH}	Chip Enable LOW Short Cycle:	15		15		25		35		4
		Pulse Width Medium Cycle:	30		35		50		75		4
		Long Cycle:	45		55		75		100		4
3	t_{EHEL}	Chip Enable HIGH Pulse Width	5		15		15		20		
4	t_{CVEL}	Control Input to Chip Enable LOW Set-up Time	0		0		0		0		5
5	t_{ELCX}	Control Input from Chip Enable LOW Hold Time	10		10		10		15		5
6	t_{ELQX}	Chip Enable LOW to Outputs Active	3		3		3		3		6
7	t_{ELQV}	Chip Enable LOW to Outputs Valid		30		30		50		70	4,6
				40		52		75		85	4,6
8	t_{EHQZ}	Chip Enable HIGH to Outputs High-Z	3	10	3	10	3	15	3	20	7
9	t_{DVEL}	Data to Chip Enable LOW Set-up Time	0		0		0		0		
10	t_{ELDX}	Data from Chip Enable LOW Hold Time	10		10		10		15		
11	t_{FIVEL}	Full In Valid to Chip Enable LOW Set-up Time	0		0		0		0		
12	t_{FIVFFV}	Full In Valid to Full Flag Valid		5		5		7		8	
13	t_{ELFFV}	Chip Enable LOW to Full Flag Valid		35		50		75		90	
14	t_{MIVEL}	Match in Valid to Chip Enable LOW Set-up Time	0		0		0		0		
15	t_{EHMFX}	Chip Enable HIGH to /MF, /MA, /MM Invalid	0		0		0		0		
16	t_{MIVMFV}	Match In Valid to /MF, /MM, Valid		4		5		7		8	
17	t_{EHMFV}	Chip Enable HIGH to /MF Valid		16		16		25		30	
18	t_{EHMXV}	Chip Enable HIGH to /MA and /MM Valid		18		18		25		30	
19	t_{RLRH}	Reset LOW Pulse Width	50		100		100		100		8

Notes:

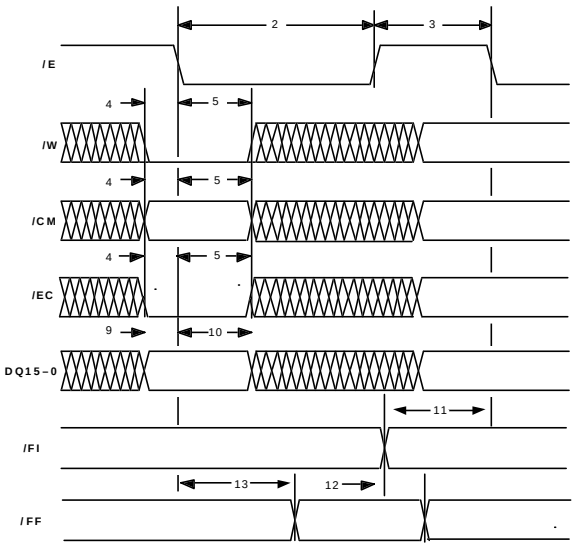
1. -1.0 Volts for a duration of 10 ns measured at the 50% amplitude points for Input-only lines (Figure 8).
2. Common I/O lines are clamped, so that signal transients cannot fall below -0.5 Volts.
3. Over Ambient Operating Temperature and Vcc(min) to Vcc(max).
4. See Table 9 on page 22.
5. Control signals are /W, /CM, and /EC.
6. With load specified in Figure 7, Test Load A.
7. With load specified in Figure 7, Test Load B.
8. /E must be HIGH during this period to ensure accurate default values in the configuration registers.
9. With output and I/O pins unloaded.

TIMING DIAGRAMS

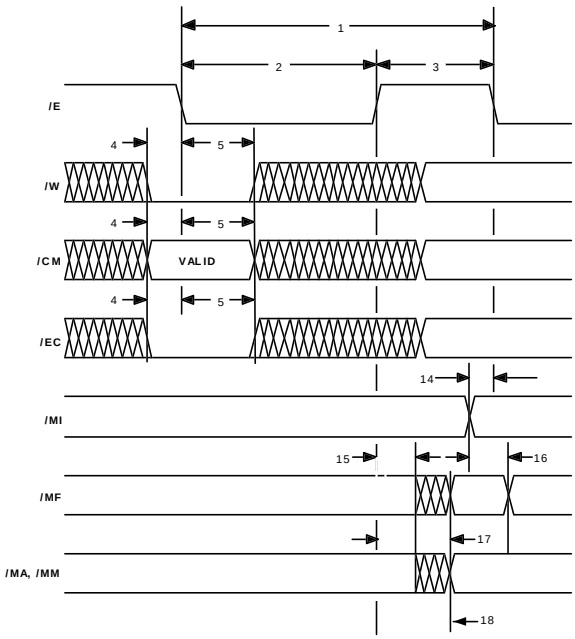
READ CYCLE



WRITE CYCLE



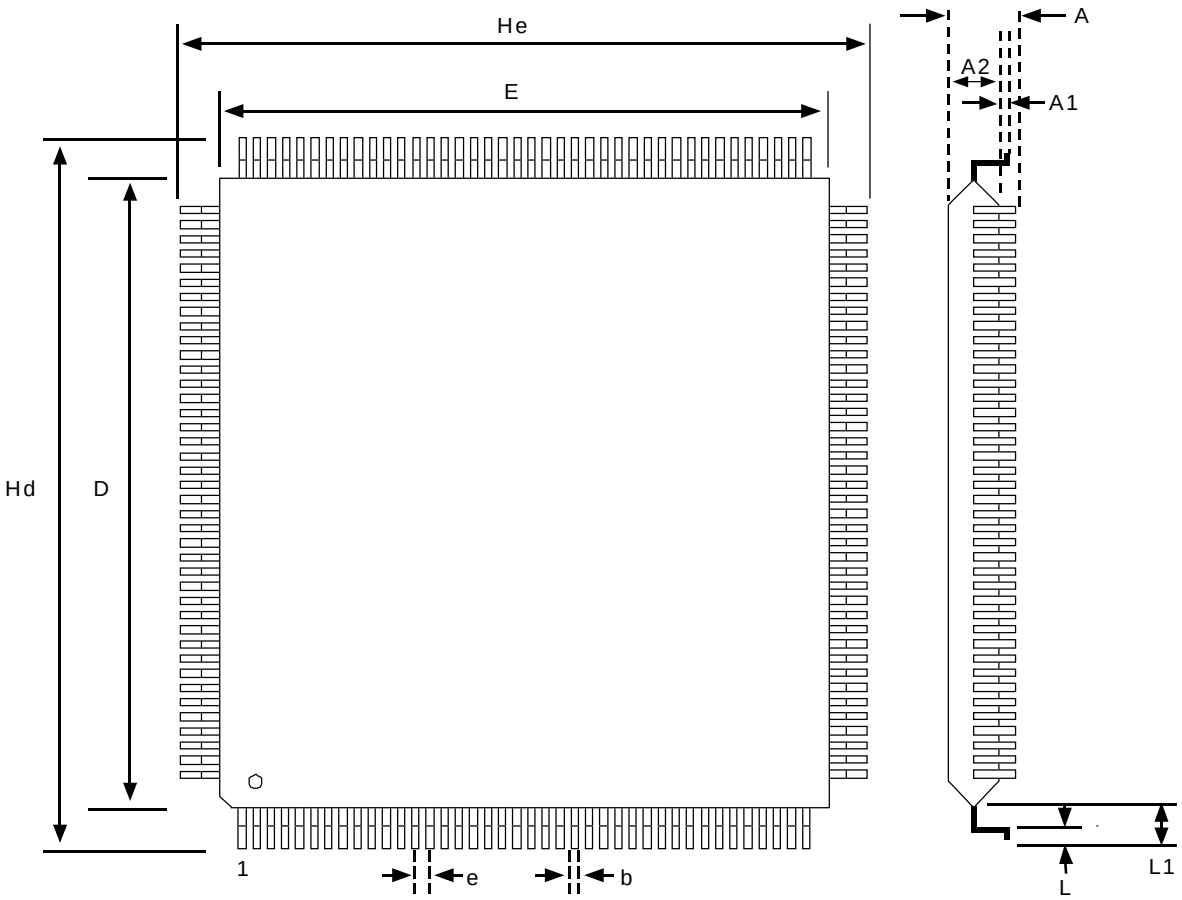
COMPARE CYCLE



NOTES

NOTES

PACKAGE OUTLINE



Dimensions are in mm.

160-pin PQFP	Dim. A	Dim. A1	Dim. A2	Dim. b	Dim. D	Dim. E	Dim. e	Dim. Hd	Dim. He	Dim. L	Dim. L1
Min		0.25	3.20	0.22						0.73	
Nom			3.32	.30	28.0	28.0	0.65	31.20	31.20	0.88	1.60 Ref
Max	4.1		3.60	0.38						1.03	

ORDERING INFORMATION

Part Number	Organization	Cycle Time	Package	Temperature	Voltage
MU9C7485 - 50QGC	32,768 x 64	50ns	160-PIN PQFP	0–70° C	3.3 ± 0.3
MU9C7485 - 70QGC	32,768 x 64	70ns	160-PIN PQFP	0–70° C	3.3 ± 0.3
MU9C7485 - 90QGC	32,768 x 64	90ns	160-PIN PQFP	0–70° C	3.3 ± 0.3
MU9C7485 - 12QGC	32,768 x 64	120ns	160-PIN PQFP	0–70° C	3.3 ± 0.3
MU9C7485 - 50QGI	32,768 x 64	50ns	160-PIN PQFP	-40–85° C	3.3 ± 0.3
MU9C7485 - 70QGI	32,768 x 64	70ns	160-PIN PQFP	-40–85° C	3.3 ± 0.3
MU9C7485 - 90QGI	32,768 x 64	90ns	160-PIN PQFP	-40–85° C	3.3 ± 0.3
MU9C7485 - 12QGI	32,768 x 64	120ns	160-PIN PQFP	-40–85° C	3.3 ± 0.3
MU9C6485 - 50QGC	16,384 x 64	50ns	160-PIN PQFP	0–70° C	3.3 ± 0.3
MU9C6485 - 70QGC	16,384 x 64	70ns	160-PIN PQFP	0–70° C	3.3 ± 0.3
MU9C6485 - 90QGC	16,384 x 64	90ns	160-PIN PQFP	0–70° C	3.3 ± 0.3
MU9C6485 - 12QGC	16,384 x 64	120ns	160-PIN PQFP	0–70° C	3.3 ± 0.3
MU9C6485 - 50QGI	16,384 x 64	50ns	160-PIN PQFP	-40–85° C	3.3 ± 0.3
MU9C6485 - 70QGI	16,384 x 64	70ns	160-PIN PQFP	-40–85° C	3.3 ± 0.3
MU9C6485 - 90QGI	16,384 x 64	90ns	160-PIN PQFP	-40–85° C	3.3 ± 0.3
MU9C6485 - 12QGI	16,384 x 64	120ns	160-PIN PQFP	-40–85° C	3.3 ± 0.3

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