HARRIS   HD-15530/883

June 1989   CMOS Manchester Encoder-Decoder

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**

- Support of MIL-STD-1553

- 1.25 Megabit/Sec Data Rate

- Sync Identification and Lock-in

- Clock Recovery

- Manchester II Encode, Decode

- Separate Encode and Decode

- Low Operating Power .... 50mW @ 5 Volts
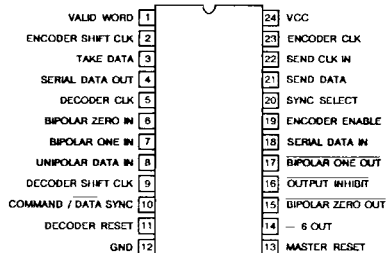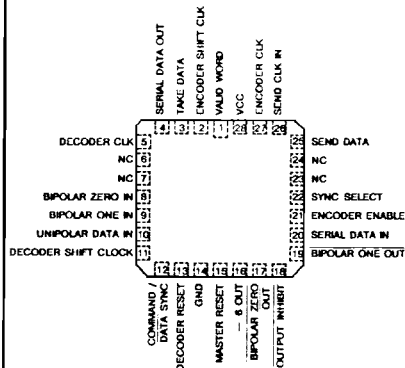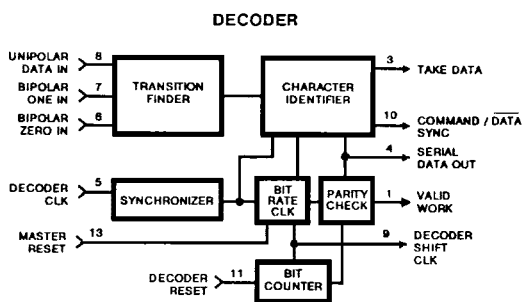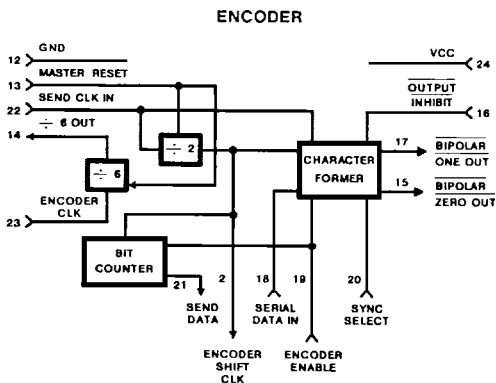
Description

The Harris HD-15530/883 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

The HD-15530/883 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable of fiber optic cable throughout the building.

Pinouts

HD1-15530/883 (CERAMIC DIP)
TOP VIEW

VALID WORD	1	24	VCC
ENCODER SHIFT CLK	2	23	ENCODER CLK
TAKE DATA	3	22	SEND CLK IN
SERIAL DATA OUT	4	21	SEND DATA
DECODER CLK	5	20	SYNC SELECT
BIPOLAR ZERO IN	6	19	ENCODER ENABLE
BIPOLAR ONE IN	7	18	SERIAL DATA IN
UNIPOLAR DATA IN	8	17	BIPOLAR ONE OUT
DECODER SHIFT CLK	9	16	OUTPUT INHIBIT
COMMAND / DATA SYNC	10	15	BIPOLAR ZERO OUT
DECODER RESET	11	14	÷ 6 OUT
GND	12	13	MASTER RESET

HD4-15530/883 (CERAMIC LCC)
TOP VIEW

Block Diagrams

ENCODER

DECODER

CMOS DATA COMMUNICATIONS

6

Pin Description

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
2	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low–to–high transition of Encoder Shift Clock.
3	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
5	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder, input a frequency equal to 12X the data rate.
6	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the Unipolar input is used.
8	I	UNIPOLAR DATA IN	Decoder	With pin 6 high and pin 7 low, this pin enters unipolar data into the transtition finder circuit. If not used this input must be held low.
9	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GROUND	Both	Ground Supply pin.
13	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and resets the ÷ 6 circuit.
14	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	BIPOLAR ZERO OUT	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	OUTPUT INHIBIT	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
17	O	BIPOLAR ONE OUT	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
20	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
21	O	SEND DATA	Encoder	An active high output which enables the external source of serial data.
22	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
23	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
24	I	VCC	Both	VCC is the +5V power supply pin. A 0.1 µF decoupling capacitor from VCC (pin 24) to GROUND (pin 12) is recommended.

I = Input   O = Output

Absolute Maximum Ratings

Supply Voltage . . . . +7.0V
Input, Output or I/O Voltage Applied . . . . . . GND-0.3V to VCC+0.3
Storage Temperature Range . . . . −65°C to +150°C
Junction Temperature . . . . +175°C
Lead Temperature (Soldering 10 sec) . . . . +300°C
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	50.4°C/W	11.7°C/W
Ceramic LCC Package	71.1°C/W	16.8°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 992mW
Ceramic LCC Package 703mW
Gate Count . . . . 456 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage . . . . +4.5V to +5.5V
Ambient Operating Temperature Range (T_A) . . . −55°C to +125°C
Encoder/Decoder Clock Rise Time . . . . 8ns Max
Encoder/Decoder Clock Fall Time . . . . 8ns Max

Sync Transition Span (TD2) . . . . 18 TDC Typical (Note1)
Short Data Transition Span (TD4) . . . . 6 TDC Typical (Note1)
Long Data Transition Span (TD5) . . . . 12 TDC Typical (Note1)

TABLE 1. HD-15530/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	VIL	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	–	0.2 VCC	V
Input HIGH Voltage	VIH	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	0.7 VCC	–	V
Input LOW Clock Voltage	VILC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	–	GND+0.5	V
Input HIGH Clock Voltage	VIHC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC-0.5	–	V
Output LOW Voltage	VOL	IOL = 1.8mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	–	0.4	V
Output HIGH Voltage	VOH	IOH = -3mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	–	V
Input Leakage Current	II	VI = GND or VCC VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Standby Supply Current	ICCSB	VIN = VCC = 5.5V Output Open	1, 2, 3	$-55°C \leq T_A \leq +125°C$	–	2	mA
Function Test	FT	(Note 3)	7, 8	$-55°C \leq T_A \leq +125°C$	–	–	–

NOTES: 1. TDC = Decoder clock period = 1/FDC

2. Interchanging of force and sense conditions is permitted.

3. Tested as follows: f = 15MHz, VIH = 70% VCC, VIL = 20% VCC, CL = 50pF, VOH ≥ 1.5V and VOL ≤ 1.5V.

6

CMOS DATA COMMUNICATIONS

TABLE 2. HD-15530/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ENCODER TIMING							
Encoder Clock Frequency	FEC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–	15	MHz
Send Clock Frequency	FESC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–	2.5	MHz
Encoder Data Rate	FED	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–	1.25	MHz
Master Reset Pulse Width	TMR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	–	ns
Shift Clock Delay	TE1	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–	125	ns
Serial Data Setup	TE2	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	–	ns
Serial Data Hold	TE3	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	–	ns
Enable Setup	TE4	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	–	ns
Enable Pulse Width	TE5	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	–	ns
Sync Setup	TE6	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	55	–	ns
Sync Pulse Width	TE7	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	–	ns
Send Data Delay	TE8	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	50	ns
Bipolar Output Delay	TE9	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–	130	ns
Enable Hold	TE10	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	–	ns
Sync Hold	TE11	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	95	–	ns
DECODER TIMING							
Decoder Clock Frequency	FDC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–	15	MHz
Decoder Data Rate	FDD	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–	1.25	MHz
Decoder Reset Pulse Width	TDR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	–	ns
Decoder Reset Setup Time	TDRS	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	–	ns
Decoder Reset Hold Time	TDRH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	–	ns
Master Reset Pulse	TMR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	–	ns
Bipolar Data Pulse Width	TD1	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TDC+10 (Note 1)	–	ns
One Zero Overlap	TD3	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–	TDC–10 (Note 1)	ns
Sync Delay (ON)	TD6	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–20	110	ns
Take Data Delay (ON)	TD7	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Serial Data Out Delay	TD8	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	–	80	ns
Sync Delay (OFF)	TD9	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Take Data Delay (OFF)	TD10	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Valid Word Delay	TD11	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns

NOTES: 1. TDC = Decoder clock period = 1/FDC

2. A.C. Testing as follows: Input levels: VIH = 70% VCC, VIL = 20% VCC; Input rise/fall times driven at 1ns/V; Timing reference levels: 1.5V; Output load: CL = 50pF

TABLE 3. HD-15530/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	–	15	pF
Input/Output Capacitance	CIO	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	–	15	pF
Operating Power Supply Current	ICCOP	VCC = 5.5V, f = 1MHz	1, 2	$-55^oC \leq T_A \leq +25^oC$	–	10	mA

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

2. Guaranteed but not 100% tested.

TABLE 4. APPLICABLE SUBGROUPS

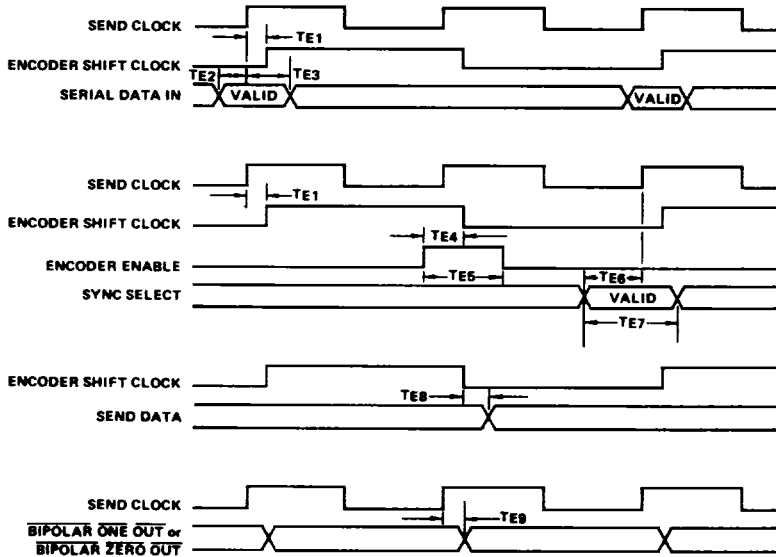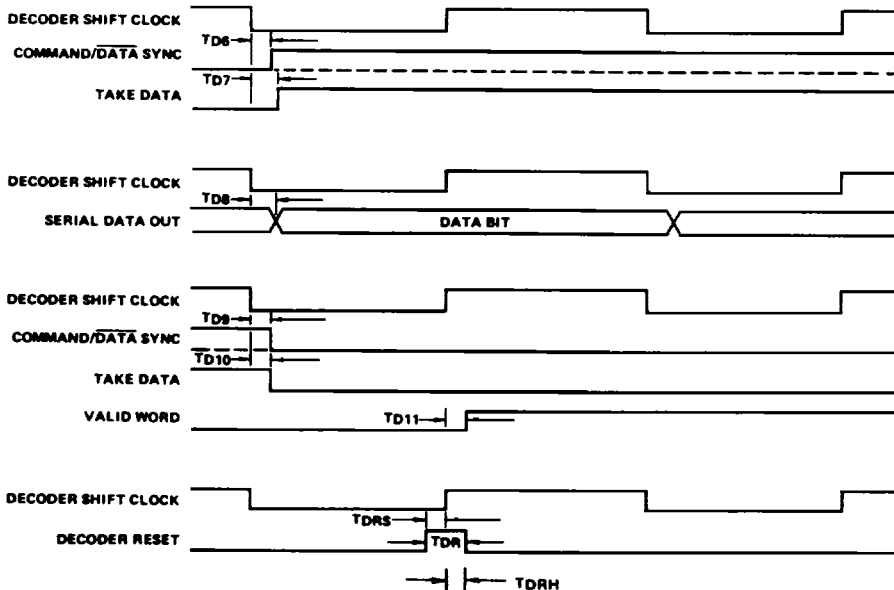| CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	–
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Test Load Circuit

DUT o———

C_{L^*}
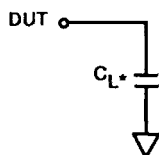
*Includes Stray and Jig Capacitance

6

CMOS DATA
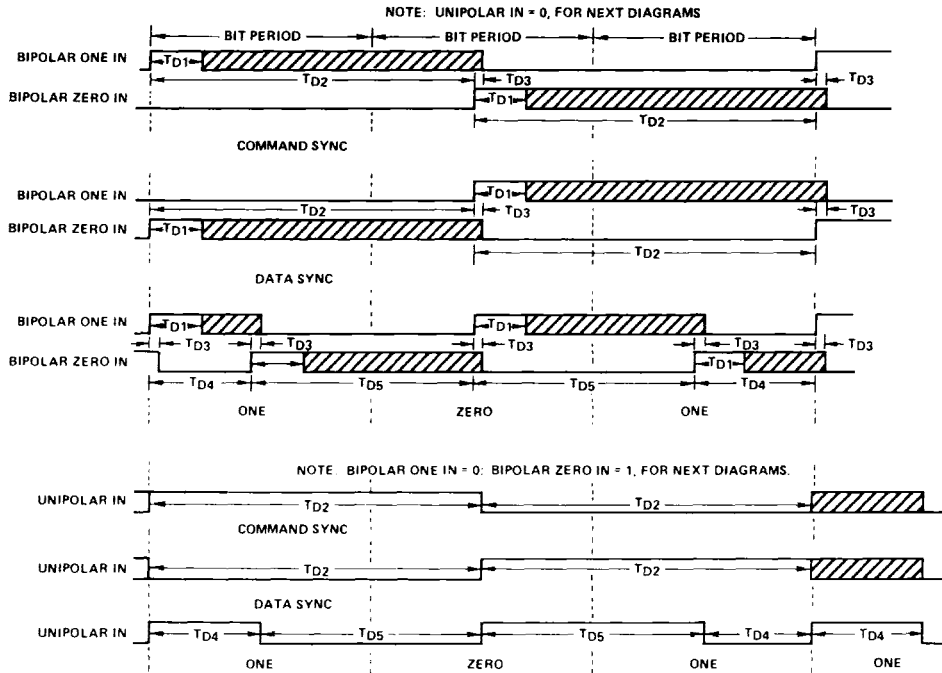COMMUNICATIONS

Timing Waveforms

ENCODER TIMING

DECODER TIMING

Timing Waveforms (Continued)

DECODER TIMING (Continued)

NOTE: UNIPOLAR IN = 0, FOR NEXT DIAGRAMS

COMMAND SYNC

DATA SYNC

ONE   ZERO   ONE

NOTE: BIPOLAR ONE IN = 0; BIPOLAR ZERO IN = 1, FOR NEXT DIAGRAMS.

COMMAND SYNC

DATA SYNC

ONE   ZERO   ONE   ONE

6

CMOS DATA
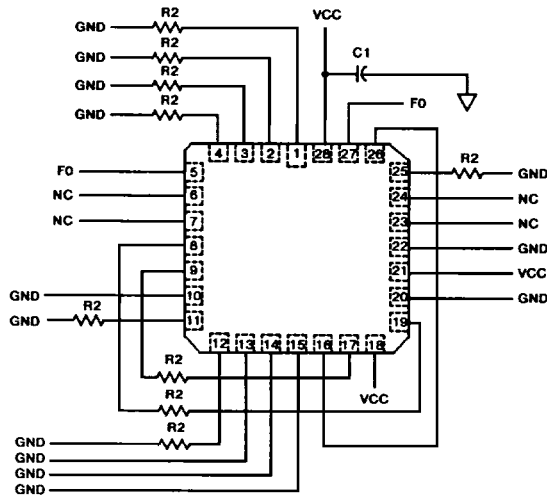COMMUNICATIONS

Burn-In Circuits

HD1-15530/883 CERAMIC DIP
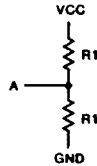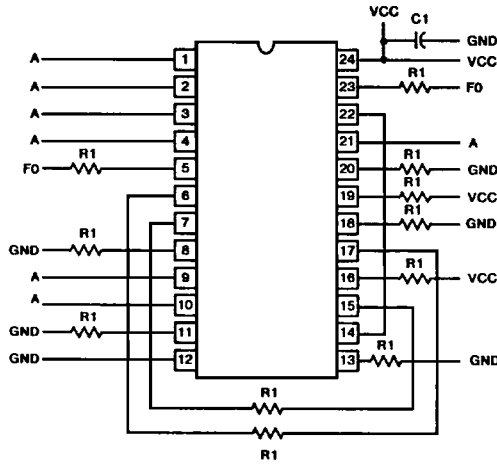
NOTES:
VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.4V
R1 = 47KΩ ± 5%
F0 = 100KHz ± 10%
C1 = 0.01µF Min.

HD4-15530/883 CERAMIC LCC

NOTES:
VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.4V
R2 = 1.8KΩ ± 5%
F0 = 100KHz ± 10%
C1 = 0.0µF Min.

Metallization Topology

DIE DIMENSIONS:
155 x 195 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
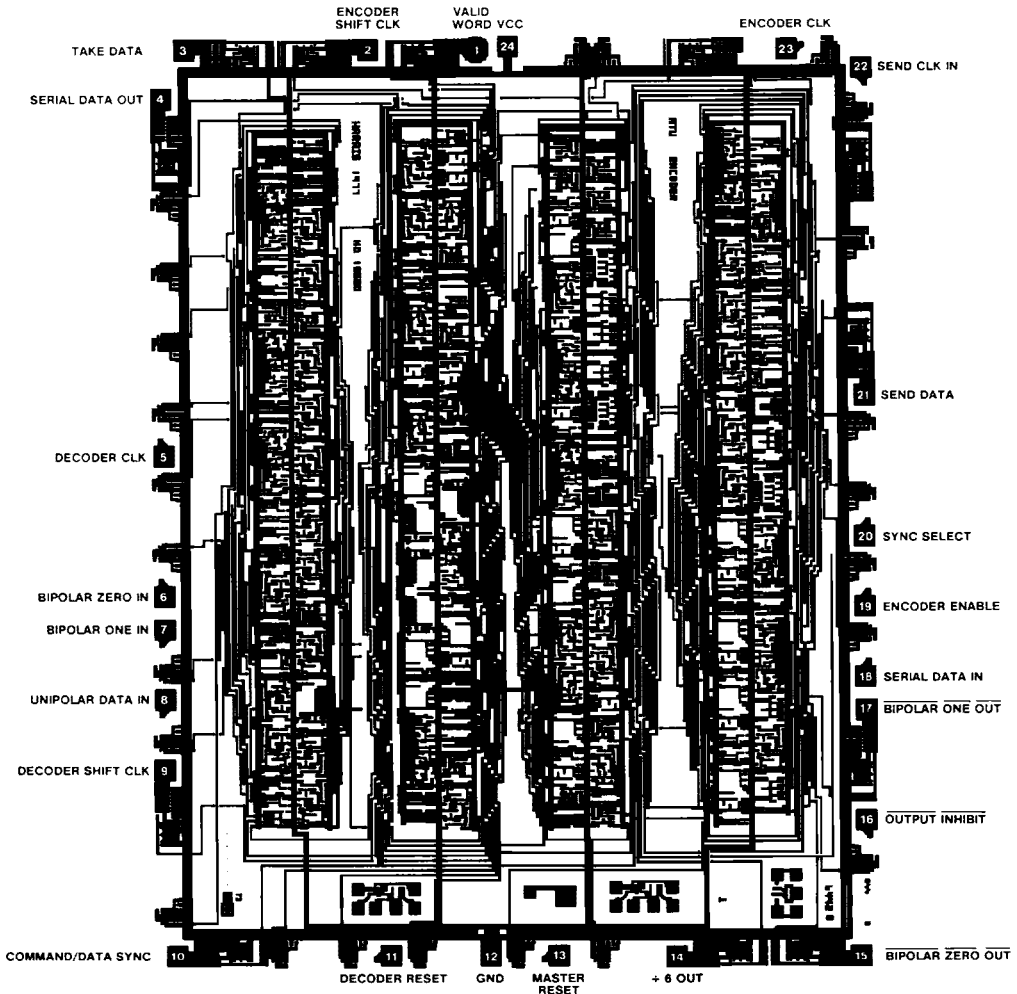
WORST CASE CURRENT DENSITY:
$1.8 \times 10^5 A/cm^2$
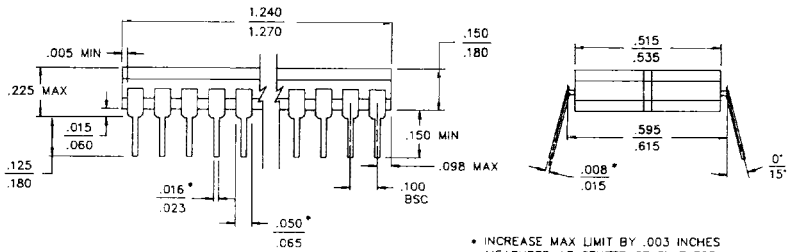
LEAD TEMPERATURE (10 seconds soldering):
$\leq 275°C$

Metallization Mask Layout

HD-15530/883

Pin	Signal
3	TAKE DATA
4	SERIAL DATA OUT
5	DECODER CLK
6	BIPOLAR ZERO IN
7	BIPOLAR ONE IN
8	UNIPOLAR DATA IN
9	DECODER SHIFT CLK
10	COMMAND/DATA SYNC
11	DECODER RESET
12	GND
13	MASTER RESET
14	+ 6 OUT
15	BIPOLAR ZERO OUT
16	OUTPUT INHIBIT
17	BIPOLAR ONE OUT
18	SERIAL DATA IN
19	ENCODER ENABLE
20	SYNC SELECT
21	SEND DATA
22	SEND CLK IN
23	ENCODER CLK
24	VALID WORD
2	ENCODER SHIFT CLK
1	VCC

6

CMOS DATA
COMMUNICATIONS

Packaging†

24 PIN (.600) CERAMIC DIP

* INCREASE MAX LIMIT BY .003 INCHES
  MEASURED AT CENTER OF FLAT FOR
  SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
  Material: Glass Frit
  Temperature: 450°C ± 10°C
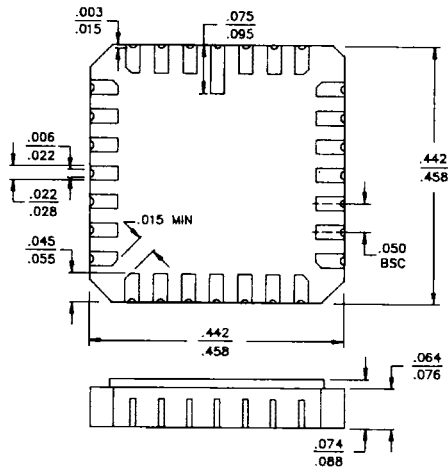 Method: Furnace Seal

INTERNAL LEAD WIRE:
  Material: Aluminum
  Diameter: 1.25 Mil
  Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

28 PAD CERAMIC LCC

PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
  Material: Gold/Tin (80/20)
  Temperature: 320°C ± 10°C
  Method: Furnace Braze

INTERNAL LEAD WIRE:
  Material: Aluminum
  Diameter: 1.25 Mil
  Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{Min}{Max}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

CMOS Manchester Encoder-Decoder

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③. During these sixteen periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the

ENCODER SHIFT CLOCK so it can be sampled on the low-to-high transition ③ - ④. After the sync and Manchester II coded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ as shown to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.
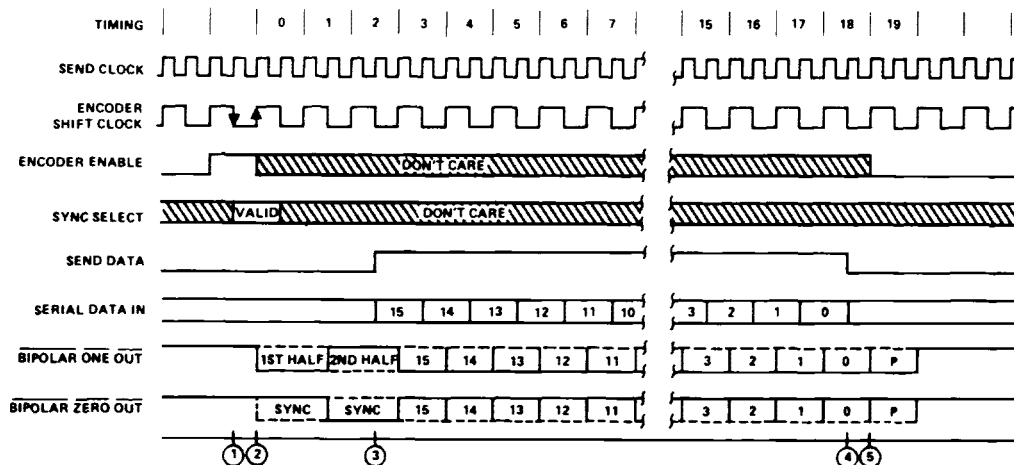
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from BIPOLAR ONE OUT of an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/DATA SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixteen DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The

decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.
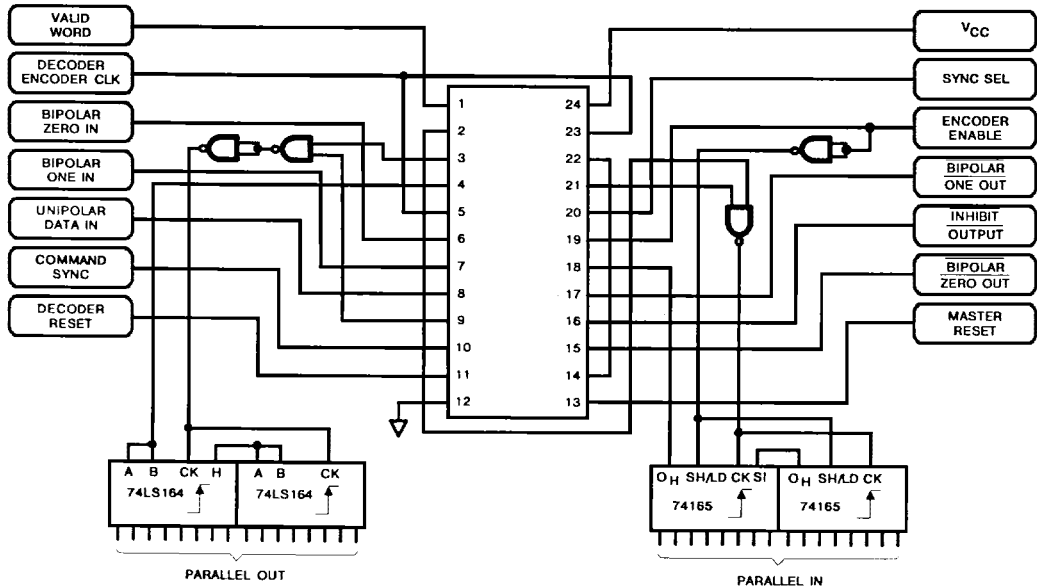
At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.
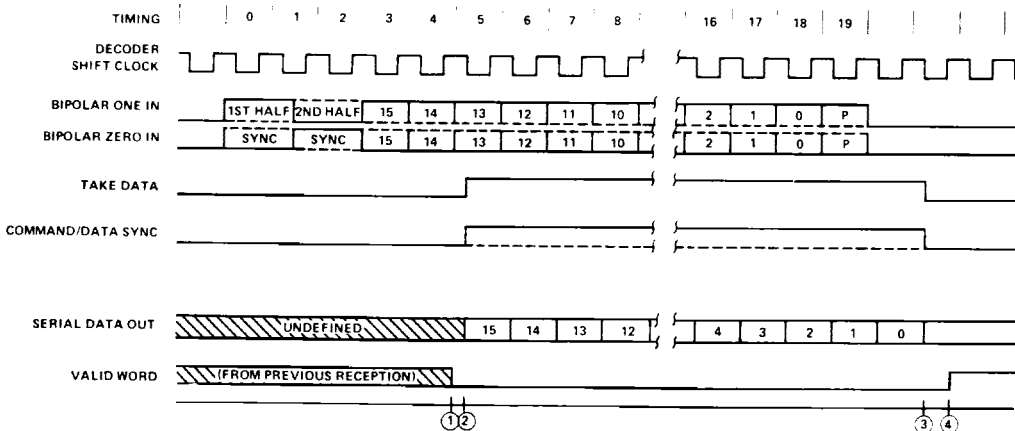
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

How to Make Our MTU Look Like a Manchester Encoded UART

VALID WORD		V_CC
DECODER ENCODER CLK		SYNC SEL
BIPOLAR ZERO IN		ENCODER ENABLE
BIPOLAR ONE IN		BIPOLAR ONE OUT
UNIPOLAR DATA IN		INHIBIT OUTPUT
COMMAND SYNC		BIPOLAR ZERO OUT
DECODER RESET		MASTER RESET

Pin diagram:
Left side 1–12, Right side 13–24

A B CK H 74LS164
A B CK 74LS164
PARALLEL OUT

O_H SH/LD CK SI 74165
O_H SH/LD CK 74165
PARALLEL IN

Typical Timing Diagrams for a Manchester Encoded UART

ENCODER TIMING

ENCODER ENABLE — VALID — VALID
SYNC SELECT
PARALLEL IN
BIPOLAR ONE OUT — P
BIPOLAR ZERO OUT — P
SYNC   MSB   LSB   PARITY

DECODER TIMING

SYNC   MSB   LSB   PARITY
BIPOLAR ONE IN — P
BIPOLAR ZERO IN — P
COMMAND SYNC
PARALLEL OUT — VALID — VALID
VALID WORD — FROM PREVIOUS RECEPTION