Signetics

Military Logic Products

54F350
Shifter

4-Bit Shifter (3-State)

Product Specification

FEATURES

- **Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines**
- **3-State outputs for bus organized systems**

DESCRIPTION

The 54F350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.

The 54F350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical – with logic zeros filled in at either end of the shifting field.
2. Arithmetic – where the sign bit is extended during a shift down.
3. End around – where the data word forms a continuous loop.

The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active Low Output Enable ($\overline{OE}$) input controls the state of the outputs. The outputs are in the High impedance "off" state when $\overline{OE}$ is High, and they are active when $\overline{OE}$ is Low.

ORDERING INFORMATION

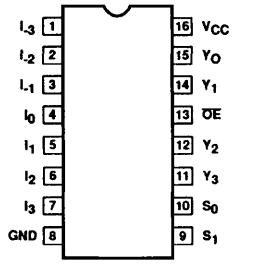
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F350/BEA
16-Pin Ceramic FlatPack	54F350/BFA
20-Pin Ceramic LLCC	54F350/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
S_0, S_1	Select inputs	1.0/2.0	20μA/1.2mA
I_{-3} - I_3	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{OE}$	Output enable input (Active Low)	1.0/2.0	20μA/1.2mA
Y_0 - Y_3	3-State outputs	150/33.3	3.0mA/20mA

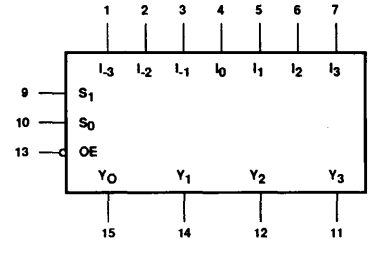
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.

PIN CONFIGURATION



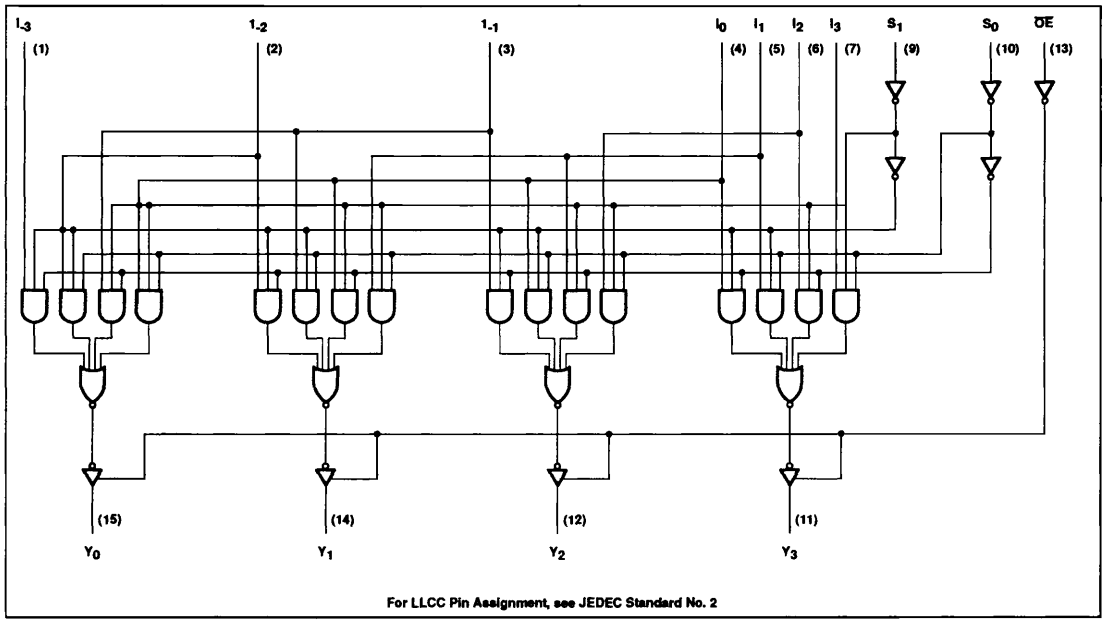
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC Pin Assignment, see JEDEC Standard No. 2

FUNCTION TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state
D_n = High or Low state of referenced I_n input

LOGIC EQUATIONS

$$Y_0 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_0 + S_0 \cdot \overline{S}_1 \cdot I_{-1} + \overline{S}_0 \cdot S_1 \cdot I_{-2} + S_0 \cdot S_1 \cdot I_{-3}$$
$$Y_1 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_1 + S_0 \cdot \overline{S}_1 \cdot I_0 + \overline{S}_0 \cdot S_1 I_{-1} + S_0 \cdot S_1 \cdot I_{-2}$$
$$Y_2 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_2 + S_0 \cdot \overline{S}_1 \cdot I_1 + \overline{S}_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot I_{-1}$$
$$Y_3 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_3 + S_0 \cdot \overline{S}_1 \cdot I_2 + \overline{S}_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0$$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH2}	High-level output current			-3	mA
I_{OH1}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH2}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH2} = -3mA	2.4			V
V_{OH1}	High-level output voltage			I_{OH1} = -1mA	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.9	-1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-90	-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max			22	35	mA
		I_{CCL}				26	41	mA
		I_{CCZ}				26	42	mA

AC ELECTRICAL CHARACTERISTICS

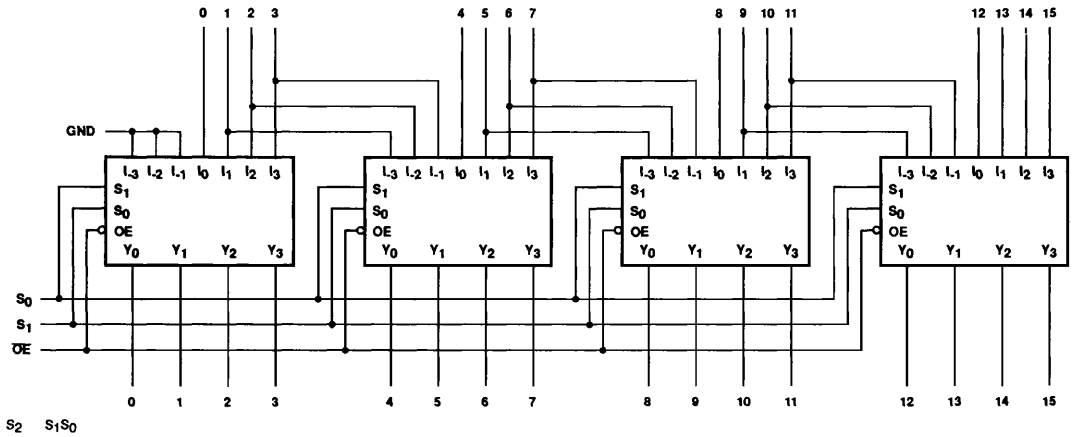
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic."

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 2.5	4.5 4.0	6.0 5.5	3.0 2.5	7.0 6.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 1	4.0 3.0	7.8 6.5	10 8.5	4.0 3.0	11 9.5	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	2.5 4.0	5.0 7.0	7.0 9.0	2.5 4.0	10 10	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	3.9 4.0	5.5 5.5	2.0 2.0	6.5 6.5	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

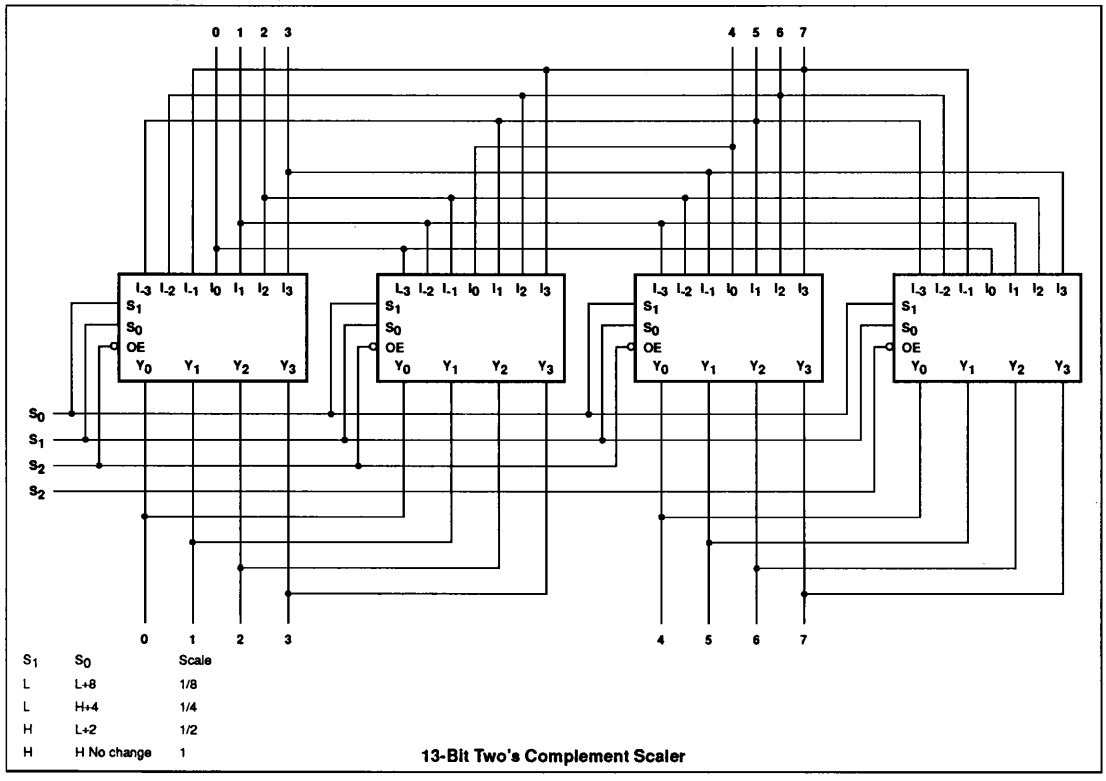
APPLICATIONS



S_2	S_1S_0	
L	L L	No shift
L	L H	Shift end around 1
L	H L	Shift end around 2
L	H H	Shift end around 3
H	L L	Shift end around 4
H	L H	Shift end around 5
H	H L	Shift end around 6
H	H H	Shift end around 7

8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places

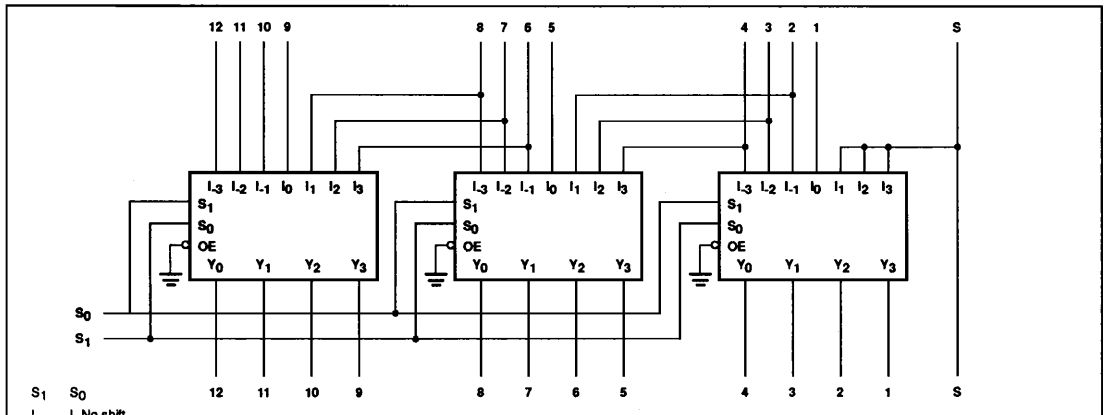
APPLICATIONS (Continued)



S_1	S_0	Scale
L	L+8	1/8
L	H+4	1/4
H	L+2	1/2
H	H No change	1

13-Bit Two's Complement Scaler

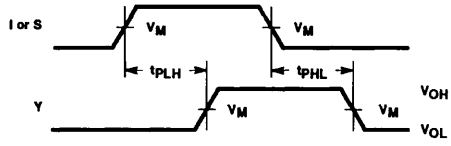
APPLICATIONS (Continued)



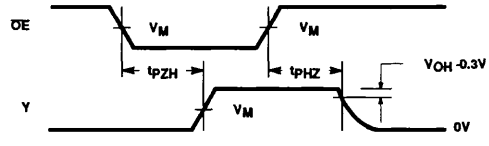
S_1	S_0	
L	L	No shift
L	H	Shift 1 place
H	L	Shift 2 places
H	H	Shift 3 places

16-Bit Shift Up 0, 1, 2, or 3 Places

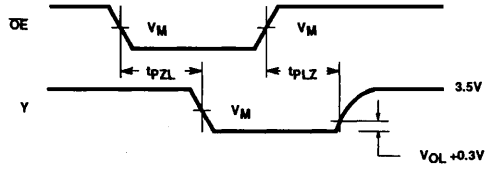
AC WAVEFORMS



Waveform 1. Propagation Delay Data and Select to Output



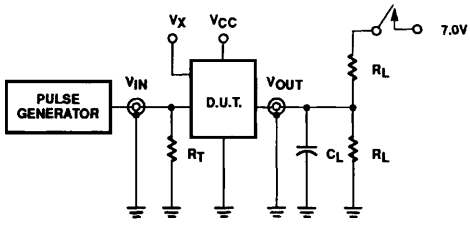
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



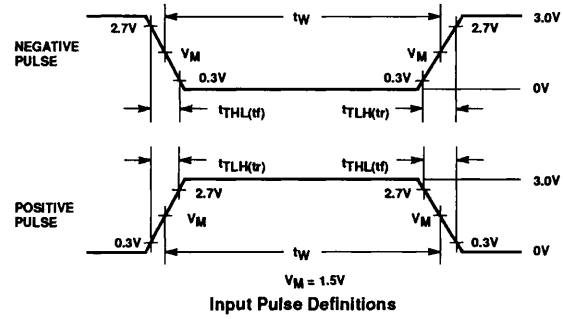
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.