

54H/74H106

DESCRIPTION

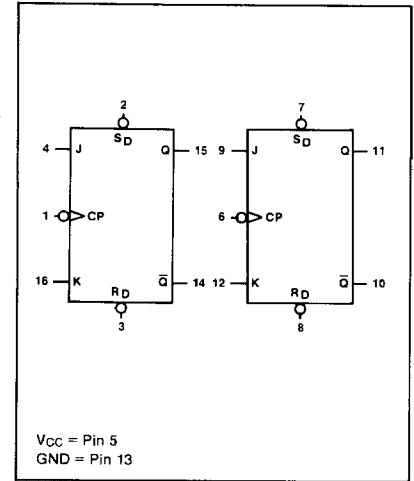
The "106" is a Dual JK Negative Edge-Triggered Flip-Flop with individual JK, Clock, direct Set and direct Reset inputs. The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the Clock and data inputs forcing the outputs to their steady state level as shown in the Truth Table.

A HIGH level on the Clock (\overline{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may change while the \overline{CP} is HIGH, and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of \overline{CP} .

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	Fig. A	N74H106N	
Ceramic DIP	Fig. A	N74H106F	S54H106F
Flatpak	Fig. A		S54H106W

LOGIC SYMBOL



PIN CONFIGURATION

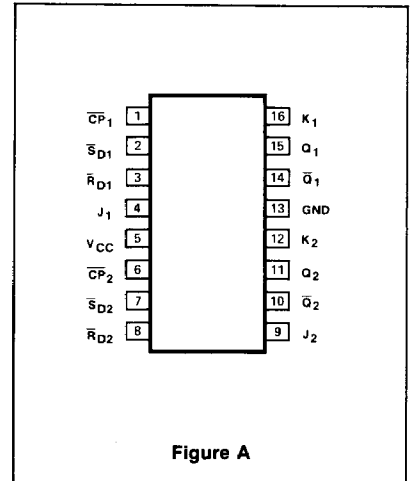


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
\overline{CP}	Clock input				
	I_{IH} (mA)		-1.0		
	I_{IL} (mA)		-4.8		
\bar{R}_D	Reset input				
	I_{IH} (μA)		100		
	I_{IL} (mA)		-2.0		
\bar{S}_D	Set input				
	I_{IH} (μA)		100		
	I_{IL} (mA)		-2.0		
JK	Data inputs				
	I_{IH} (μA)		50		
	I_{IL} (mA)		-2.0		
Q & \bar{Q} Outputs	I_{OH} (μA)		-500		
	I_{OL} (mA)		20		

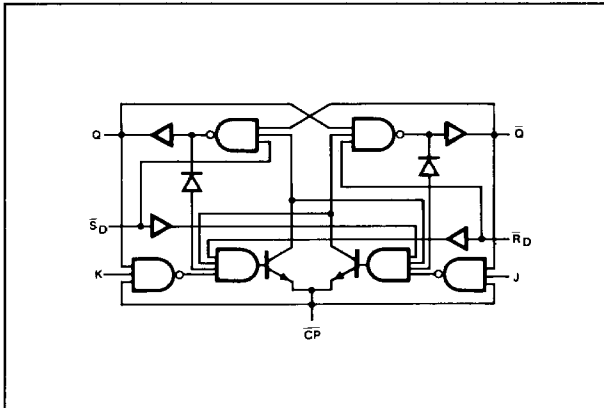
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$I_{IH}(\overline{CP})$	Input HIGH current			0	-1.0					mA
I_{CC}	Supply current				76					mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	CP	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (C)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	\bar{q}	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
		f_{MAX}	Maximum Clock frequency			40				
t_{PLH} t_{PHL}	Propagation delay Clock to Output				15 20					ns ns
t_{PLH}	Propagation delay Set or Reset to Output	Waveform 5			12					ns
t_{PHL}		Waveform 5, CP = HIGH			20					ns
t_{PHL}		Waveform 5, CP = LOW			35					ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)			10						ns
$t_{w(L)}$	Clock pulse width (LOW)			15						ns
$t_{w(L)}$	Set or Reset pulse width (LOW)			16						ns
$t_s(H)$	Setup time HIGH J or K to Clock			10						ns
$t_h(H)$	Hold time HIGH J or K to Clock			0						ns
$t_s(L)$	Setup time LOW J or K to Clock			13						ns
$t_h(L)$	Hold time LOW J or K to Clock			0						ns

NOTE

c. Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.