

524,288 WORD X 32 BIT (EDO) DYNAMIC RAM

Description

The TC5118325BJ/BFT is the Hyper Page Mode (EDO) dynamic RAM organized 524,288 words by 32 bits. The TC5118325BJ/BFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5118325BJ/BFT to be packaged in 70 pin plastic SOJ (400mil) and 70 pin plastic TSOP (400mil). The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

B-DRAM
Components
16M DRAM

Features

- 524,288 word by 32 bit organization
- Fast access time and cycle time
- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low Power
 - 1128mW MAX. Operating (TC5118325BJ/BFT-60)
 - 990mW MAX. Operating (TC5118325BJ/BFT-70)
 - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, \overline{CAS} before \overline{RAS} refresh, \overline{RAS} -only refresh, Hidden refresh, Hyper Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC5118325BJ: SOJ70-P-400A
TC5118325BFT: TSOP70-P-400G

Key Parameters

| ITEM | TC5118325BJ/BFT | |
|--------------------------------------|-----------------|--------|
| | -60 | -70 |
| t_{RAC} RAS Access Time | 60ns | 70ns |
| t_{AA} Column Address Access Time | 30ns | 35ns |
| t_{CAC} CAS Access Time | 15ns | 20ns |
| t_{RC} Cycle Time | 110ns | 1230ns |
| t_{HPC} Hyper Page Mode Cycle Time | 25ns | 30ns |

Note: For packaging details see Mechanical Dimensions section.

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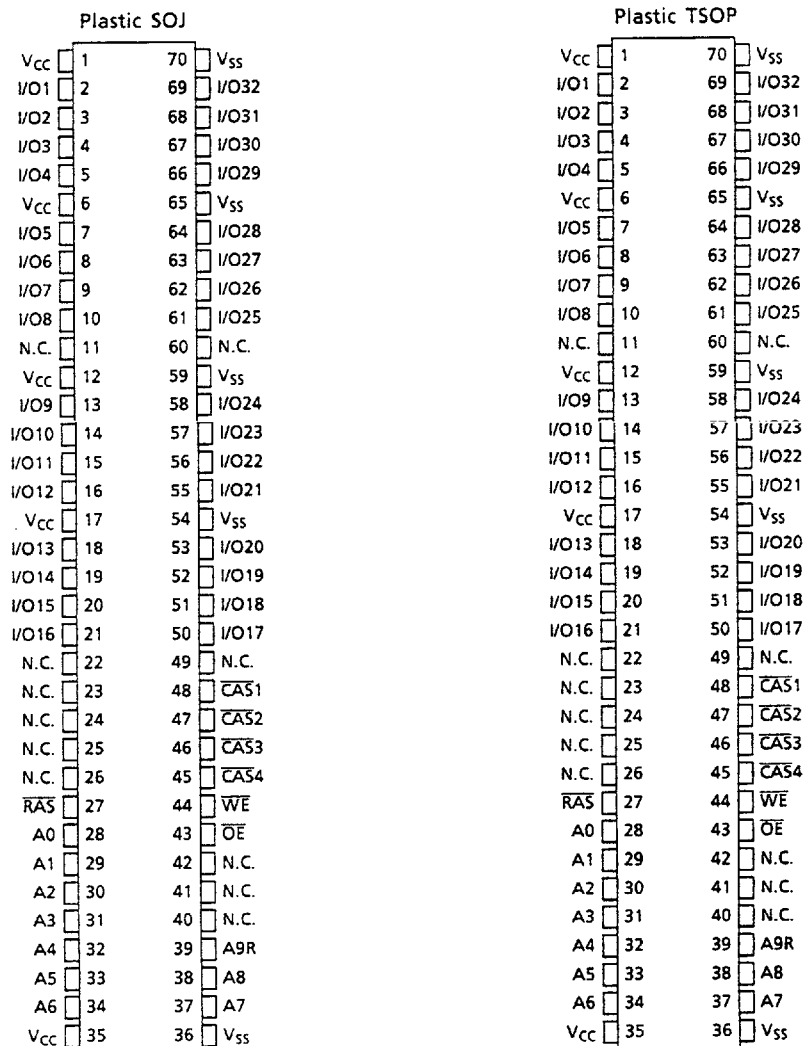
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Pin Name

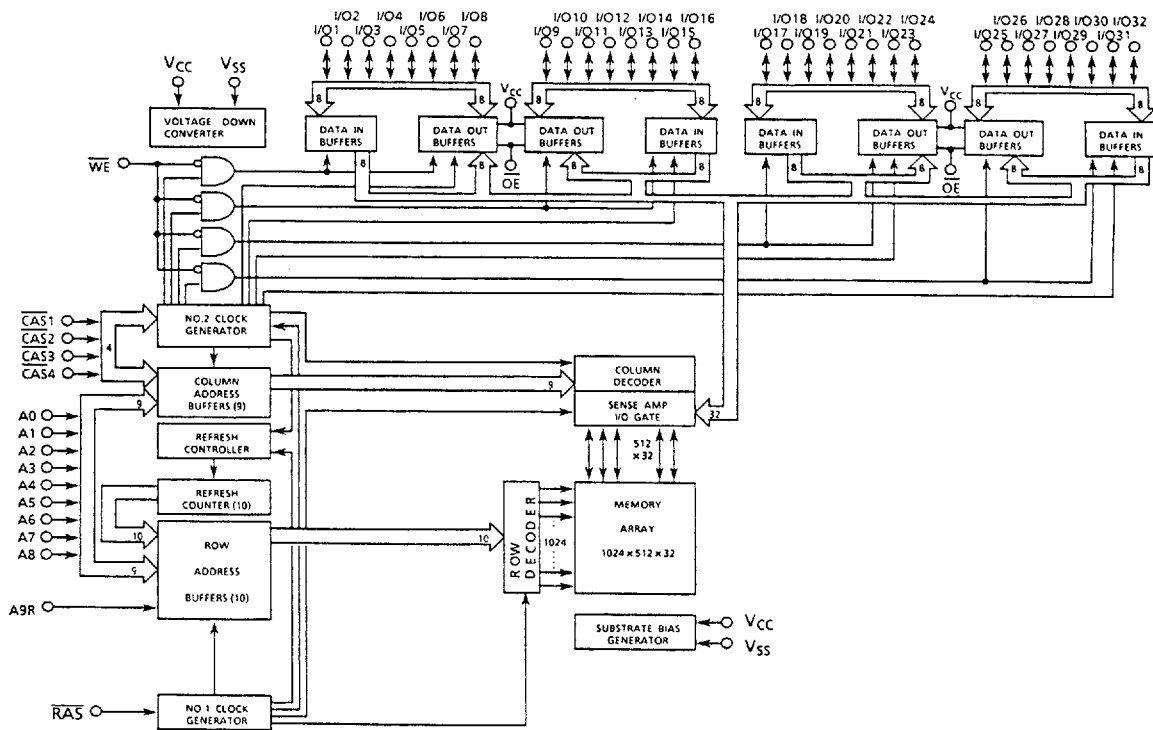
| | |
|-----------------|-----------------------|
| A0 ~ A9 | Address Inputs |
| RAS | Row Address Strobe |
| CAS1 ~ CAS4 | Column Address Strobe |
| WE | Write Enable |
| OE | Output Enable |
| I/O1 ~ I/O32 | Data Input/Output |
| V _{CC} | Power (+5V) |
| V _{SS} | Ground |
| NC | No Connection |

Pin Connection (Top View)



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Block Diagram



B. DRAM Components 16M DRAM

Absolute Maximum Ratings

| ITEM | SYMBOL | RATING | UNIT | NOTE |
|------------------------------|--------------|-----------------------|------|------|
| Input Voltage | V_{IN} | -0.5 ~ $V_{CC} + 0.5$ | V | 1 |
| Output Voltage | V_{OUT} | -0.5 ~ $V_{CC} + 0.5$ | V | 1 |
| Power Supply Voltage | V_{CC} | -0.5 ~ 7.0 | V | 1 |
| Operating Temperature | T_{OPR} | 0 ~ 70 | °C | 1 |
| Storage Temperature | T_{STG} | -55 ~ 150 | °C | 1 |
| Soldering Temperature (10s) | T_{SOLDER} | 260 | °C | 1 |
| Power Dissipation | P_D | 1.2 | W | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

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Recommended DC Operating Conditions ($T_a = 0 \sim 70^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP | MAX | UNIT | NOTE |
|----------|--------------------|--------|-----|------------------|------|------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | - | $V_{CC} + 0.5^*$ | V | 2 |
| V_{IL} | Input Low Voltage | -0.5** | - | 0.8 | V | 2 |

* $V_{CC} + 2.0\text{V}$ at pulse width $\leq 20\text{ns}$ (pulse width is measured at V_{CC}).

** -2.0V at pulse width $\leq 20\text{ns}$ (pulse width is measured at V_{SS}).

DC Electrical Characteristics ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0 \sim 70^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | MAX | UNIT | NOTES | |
|------------|---|--------------------|-----|---------------|-------|---------|
| I_{CC1} | OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS, Address Cycling: $t_{RC}=t_{RC}$ MIN.) | TC5118325BJ/BFT-60 | - | 205 | mA | 3, 4, 5 |
| | | TC5118325BJ/BFT-70 | - | 180 | | |
| I_{CC2} | STANDBY CURRENT Power Supply Standby Current (RAS=CAS= V_{IH}) | | - | 2 | mA | |
| | | | | | | |
| I_{CC3} | RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, $\overline{\text{CAS}}=V_{IH}$; $t_{RC}=t_{RC}$ MIN.) | TC5118325BJ/BFT-60 | - | 205 | mA | 3, 5 |
| | | TC5118325BJ/BFT-70 | - | 180 | | |
| I_{CC4} | HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode (RAS= V_{IL} , $\overline{\text{CAS}}$, Address Cycling: $t_{HPC}=t_{HPC}$ MIN.) | TC5118325BJ/BFT-60 | - | 145 | mA | 3, 5 |
| | | TC5118325BJ/BFT-70 | - | 125 | | |
| I_{CC5} | STANDBY CURRENT Power Supply Standby Current (RAS=CAS= $V_{CC}-0.2\text{V}$) | - | 1 | mA | | |
| I_{CC6} | CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Mode (RAS, $\overline{\text{CAS}}$, Cycling: $t_{RC}=t_{RC}$ MIN.) | TC5118325BJ/BFT-60 | - | 205 | mA | 3, 5 |
| | | TC5118325BJ/BFT-70 | - | 180 | | |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0\text{V} \leq V_{IN} \leq V_{CC}$, All Other Pins Not Under Test= 0V) | -10 | 10 | μA | | |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, ($0\text{V} \leq V_{OUT} \leq V_{CC}$)) | -10 | 10 | μA | | |
| V_{OH} | OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -2\text{mA}$) | 2.4 | - | V | | |
| V_{OL} | OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 2\text{mA}$) | - | 0.4 | V | | |

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Electrical Characteristics and Recommended AC Operating Conditions ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

(Notes 6,7,8)

| SYMBOL | PARAMETER | TC5118325BJ/BFT | | | | UNIT | NOTES |
|------------|--|-----------------|---------|-----|---------|------|-----------|
| | | -60 | | -70 | | | |
| | | MIN | MAX | MIN | MAX | | |
| t_{RC} | Random Read or Write Cycle Time | 110 | - | 130 | - | ns | |
| t_{RMW} | Read-Modify-Write Cycle | 137 | - | 159 | - | ns | |
| t_{RAC} | Access Time from \overline{RAS} | - | 60 | - | 70 | ns | 9, 14, 15 |
| t_{CAC} | Access Time from \overline{CAS} | - | 15 | - | 20 | ns | 9, 14 |
| t_{AA} | Access Time from Column Address | - | 30 | - | 35 | ns | 9, 15 |
| t_{CPA} | Access Time from \overline{CAS} Precharge | - | 35 | - | 40 | ns | 9 |
| t_{CLZ} | \overline{CAS} to Output in Low-Z | 0 | - | 0 | - | ns | 9 |
| t_{OFF} | Output Buffer Turn-off Delay | 0 | 15 | 0 | 15 | ns | 10, 16 |
| t_T | Transition Time (Rise and Fall) | 1 | 50 | 1 | 50 | ns | 8 |
| t_{RP} | \overline{RAS} Precharge Time | 40 | - | 50 | - | ns | |
| t_{RAS} | \overline{RAS} Pulse Width | 60 | 10,000 | 70 | 10,000 | ns | |
| t_{RASP} | \overline{RAS} Pulse Width (Hyper Page Mode) | 60 | 100,000 | 70 | 100,000 | ns | |
| t_{RSH} | \overline{RAS} Hold Time | 10 | - | 12 | - | ns | |
| t_{RHCP} | \overline{RAS} Hold Time from \overline{CAS} Precharge (Hyper Page Mode) | 35 | - | 40 | - | ns | |
| t_{CSH} | \overline{CAS} Hold Time | 40 | - | 45 | - | ns | |
| t_{CAS} | \overline{CAS} Pulse Width | 10 | 10,000 | 12 | 10,000 | ns | |
| t_{RCD} | \overline{RAS} to \overline{CAS} Delay Time | 14 | 50 | 14 | 50 | ns | 14 |
| t_{RAD} | \overline{RAS} to Column Address Delay Time | 12 | 35 | 12 | 35 | ns | 15 |
| t_{CRP} | \overline{CAS} to \overline{RAS} Precharge Time | 5 | - | 5 | - | ns | |
| t_{CP} | \overline{CAS} Precharge Time | 10 | - | 10 | - | ns | |
| t_{ASR} | Row Address Set-Up Time | 0 | - | 0 | - | ns | |
| t_{RAH} | Row Address Hold Time | 10 | - | 10 | - | ns | |
| t_{ASC} | Column Address Set-Up Time | 0 | 0 | 0 | 0 | ns | |
| t_{CAH} | Column Address Hold Time | 10 | - | 12 | - | ns | |
| t_{RAL} | Column Address to \overline{RAS} Lead Time | 30 | - | 35 | - | ns | |
| t_{RCS} | Read Command Set-Up Time | 0 | - | 0 | - | ns | |
| t_{RCH} | Read Command Hold Time | 0 | - | 0 | - | ns | 11 |
| t_{RRH} | Read Command Hold Time referenced to \overline{RAS} | 0 | - | 0 | - | ns | 11 |
| t_{WCH} | Write Command Hold Time | 10 | - | 12 | - | ns | |
| t_{WP} | Write Command Pulse Width | 7 | - | 9 | - | ns | |
| t_{RWL} | Write Command to \overline{RAS} Lead Time | 12 | - | 14 | - | ns | |

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Electrical Characteristics and Recommended AC Operating Conditions (Cont)

| SYMBOL | PARAMETER | TC5118325BJ/BFT | | | | UNIT | NOTES |
|------------|---|-----------------|-----|-----|-----|------|-------|
| | | -0 | | -70 | | | |
| | | MIN | MAX | MIN | MAX | | |
| t_{CWL} | Write Command to \overline{CAS} Lead Time | 12 | - | 14 | - | ns | |
| t_{DS} | Data Set-Up Time | 0 | - | 0 | - | ns | 12 |
| t_{DH} | Data Hold Time | 10 | - | 12 | - | ns | 12 |
| t_{REF} | Refresh Period | - | 16 | - | 64 | ms | |
| t_{WCS} | Write Command Set-Up Time | 0 | - | 0 | - | ns | 13 |
| t_{CWD} | \overline{CAS} to \overline{WE} Delay Time | 34 | - | 39 | - | ns | 13 |
| t_{RWD} | \overline{RAS} to \overline{WE} Delay Time | 79 | - | 89 | - | ns | 13 |
| t_{AWD} | Column Address to \overline{WE} Delay Time | 49 | - | 54 | - | ns | 13 |
| t_{CPWD} | \overline{CAS} Precharge to \overline{WE} Delay Time | 54 | - | 59 | - | ns | 13 |
| t_{CSR} | \overline{CAS} Set-Up Time (\overline{CAS} before \overline{RAS} Cycle) | 5 | - | 5 | - | ns | |
| t_{CHR} | \overline{CAS} Hold Time (\overline{CAS} before \overline{RAS} Cycle) | 10 | - | 15 | - | ns | |
| t_{RPC} | \overline{RAS} to \overline{CAS} Precharge Time | 5 | - | 5 | - | ns | |
| t_{CPT} | \overline{CAS} Precharge Time (\overline{CAS} before \overline{RAS} Counter Test Cycle) | 20 | - | 30 | - | ns | |
| t_{ROH} | \overline{RAS} Hold Time referenced to \overline{OE} | 10 | - | 10 | - | ns | |
| t_{OEA} | \overline{OE} Access Time | - | 20 | - | 20 | ns | 9 |
| t_{OED} | \overline{OE} to Data Delay | 15 | - | 15 | - | ns | |
| t_{OLZ} | \overline{OE} to Output in Low-Z | 0 | - | 0 | - | ns | |
| t_{OEZ} | Output buffer turn off Delay Time from \overline{OE} | 0 | 15 | 0 | 15 | ns | 10 |
| t_{OEH} | \overline{OE} Command Hold Time | 15 | - | 15 | - | ns | |
| t_{ODS} | Output Disable Set-Up Time | 0 | - | 0 | - | ns | |

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Electrical Characteristics and Recommended AC Operating Conditions (Cont)

| SYMBOL | PARAMETER | TC5118325BJ/BFT | | | | UNIT | NOTES |
|--------------------|--|-----------------|-----|-----|-----|------|--------|
| | | -60 | | -70 | | | |
| | | MIN | MAX | MIN | MAX | | |
| t _{RNCD} | RAS to next CAS Delay Time (Hyper Page Mode) | 65 | - | 70 | - | ns | |
| t _{HPC} | Hyper Page Mode Cycle Time | 25 | - | 30 | - | ns | |
| t _{HPRWC} | Hyper Page Mode Read-Modify-Write Cycle Time | 70 | - | 77 | - | ns | |
| t _{COH} | Output Data Hold Time | 5 | - | 5 | - | ns | |
| t _{REZ} | Output Buffer Turn-off Delay from RAS | 0 | 15 | 0 | 20 | ns | 10, 16 |
| t _{WEZ} | Output Buffer Turn-off Delay from WE | 0 | 15 | 0 | 20 | ns | 10 |
| t _{WED} | WE to Data Delay | 15 | - | 20 | - | ns | |
| t _{OE} | OE Pulse Width | 15 | - | 20 | - | ns | |
| t _{OEP} | OE Precharge Time | 10 | - | 12 | - | ns | |
| t _{CPO} | CAS to OE Precharge Time | 5 | - | 5 | - | ns | |

Capacitance (V_{CC} = 5V±10%, f = 1MHz, Ta = 0 ~ 70°C)

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|-----------------|---|-----|-----|------|
| C _{I1} | Input Capacitance (A0 ~ A9, RAS, CAS1 ~ CAS4, WE, OE) | - | 7 | pF |
| C _O | Input Capacitance (I/O1 ~ I/O32) | - | 7 | |

Note: Please refer to Timing Diagrams Number 2.

B-DRAM
Components
16M DRAM

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Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} depend on cycle rate.
4. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4} , it can be changed once or less during a hyper page mode cycle (t_{HP0}).
6. An initial pause of 200 μ s is required after power-up followed by 8 \overline{RAS} only refresh cycles before proper device operation is achieved. When the internal refresh counter is used, a minimum of 8 \overline{CAS} before \overline{RAS} refresh cycles instead of 8 \overline{RAS} only refresh cycles are required.
7. AC measurements assume $t_f=2$ ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
9. This parameter is measured with a load equivalent to 1 TTL load and 50pF and at $V_{OH}=2.0V$ ($I_{OUT}=-2mA$), $V_{OL}=0.8V$ ($I_{OUT}=2mA$).
10. t_{OFF} (max.), t_{OEZ} (max.), t_{REZ} (max.) and t_{WEZ} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in Read-Modify-Write cycles.
13. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.) (Hyper Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only; If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC} .
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA} .
16. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going (t_{OFF}). If \overline{CAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going (t_{REZ}).

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B-DRAM
Components
16M DRAM

Data Out Hi-Z Control Logic

| RAS | CAS1 ~ 4 | OE | WE | Timing Specification |
|-----|----------|-----|-----|----------------------|
| "H" | | "L" | "H" | t_{OFF} |
| | "H" | "L" | "H" | t_{REZ} |
| "L" | "L" | | "H" | t_{OEZ} |
| "L" | "H" | "L" | | t_{WEZ} |

Data Out Lo-Z Control Logic

| RAS | CAS1 ~ 4 | OE | WE | Timing Specification |
|-----|----------|-----|-----|----------------------|
| "L" | | "L" | "H" | t_{CLZ} |
| "L" | "L" | | "H" | t_{OLZ} |
| "L" | "L" | | "H" | t_{OLZ} |

CAS Combination Table and I/O Assignment

| | m | n | m_x | n_x |
|---------|---------|--------------|-----------------------------|-----------------------------|
| CAS | 1 | 2, 3, 4 | I/O1 ~ I/O8 | I/O9 ~ I/O32 |
| | 2 | 1, 3, 4 | I/O9 ~ I/O16 | I/O1 ~ I/O8, I/O17 ~ I/O32 |
| | 3 | 1, 2, 4 | I/O17 ~ I/O24 | I/O1 ~ I/O16, I/O25 ~ I/O32 |
| | 4 | 1, 2, 3 | I/O25 ~ I/O32 | I/O1 ~ I/O24 |
| | 1, 2 | 3, 4 | I/O1 ~ I/O16 | I/O17 ~ I/O32 |
| | 1, 3 | 2, 4 | I/O1 ~ I/O8, I/O17 ~ I/O24 | I/O9 ~ I/O16, I/O25 ~ I/O32 |
| | 1, 4 | 2, 3 | I/O1 ~ I/O8, I/O25 ~ I/O32 | I/O17 ~ I/O24 |
| | 2, 3 | 1, 4 | I/O9 ~ I/O24 | I/O1 ~ I/O8, I/O25 ~ I/O32 |
| | 2, 4 | 1, 3 | I/O9 ~ I/O16, I/O25 ~ I/O32 | I/O1 ~ I/O8, I/O17 ~ I/O24 |
| | 3, 4 | 1, 2 | I/O17 ~ I/O32 | I/O1 ~ I/O16 |
| | 1, 2, 3 | 4 | I/O1 ~ I/O24 | I/O25 ~ I/O32 |
| | 1, 2, 4 | 3 | I/O1 ~ I/O16, I/O25 ~ I/O32 | I/O17 ~ I/O24 |
| | 1, 3, 4 | 2 | I/O1 ~ I/O8, I/O17 ~ I/O32 | I/O9 ~ I/O16 |
| 2, 3, 4 | 1 | I/O9 ~ I/O32 | I/O1 ~ I/O8 | |

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