HARRIS

HM-8816H-8

16K x 8 High Speed Asynchronous CMOS Static RAM Module

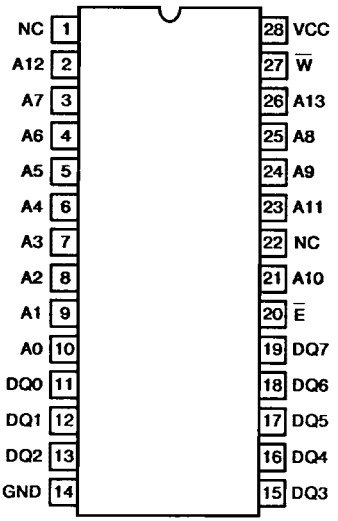
June 1989

Features

- Low Standby Supply Current 800µA
- Low Operating Supply Current 400mA
- Fast Access Time 70ns
- Low Data Retention Supply Voltage 2.0V
- Wide Operating Temperature Range ..... -55°C to +125°C
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Full CMOS — Six Transistor RAM Cells
- No Clocks or Strobes Required
- Single 5V Power Supply
- Standard DIP Size ..... 0.6" x 1.5"
- Easy Microprocessor Interfacing
- Gated Inputs

Pinout

TOP VIEW

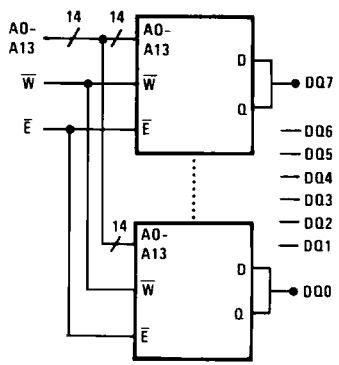


Description

The HM-8816H-8 is a high speed, asynchronous CMOS static RAM module, based on a multi-layer, co-fired, dual-in-line ceramic substrate and eight HM-65262 16K x 1 asynchronous CMOS static RAMs packaged in leadless chip carriers. The HM-8816H-8 uses on-substrate decoupling capacitors packaged in leadless chip carriers to reduce electrical noise and improve reliability. The pinout of the HM-8816H-8 conforms to the JEDEC 8-bit wide, 28 pin RAM standard, which allows the system designer to design sockets that will accomodate a variety of industry standard RAMs and EPROMs. The HM-8816H-8 also has gated inputs to simplify system design for optimum standby supply current.

The HM-65262 RAMs used in this module are full CMOS devices, utilizing arrays of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to electrical noise and alpha particles. This stability also improves the radiation tolerance of the RAMs over that of four transistor devices.

Functional Diagram



TRUTH TABLE

MODE	Ē	W̄
Standby (CMOS)	VCC	X
Standby (TTL)	VIH	X
Read	VIL	VIH
Write	VIL	VIL

PIN DESCRIPTIONS

PIN	FUNCTION
A0-A13	Address Inputs
DQ0-DQ7	Data Input/Outputs
Ē	Chip Enable
W̄	Write Enable
VCC	Power (+5V)
GND	Ground

3 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count 210000
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage ..... 4.5V to 5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSBI	Standby Supply Current (CMOS)	-	800	µA	IO = 0, $\overline{E}$ = VCC - 0.3V
ICCSB	Standby Supply Current (TTL)	-	40	mA	IO = 0, $\overline{E}$ = VIH
ICCEN	Enabled Supply Current	-	400	mA	IO = 0, $\overline{E}$ = VIL, VIN = VIH or VIL
ICCOP	Operating Supply Current (Note 3)	-	400	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL, VIN = VCC or GND
ICCDR	Data Retention Supply Current	-	320	µA	VCC = 2.0V, $\overline{E}$ = VCC - 0.3V, IO = 0
II	Input Leakage Current	-1	+1	µA	VIN = VCC or GND
IIOZ	IsO Leakage Current	-1	+1	µA	VIO = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0	-	V	$\overline{E}$ = VCC
VOL	Output Voltage Low	-	0.4	V	IOL = 8.0mA
VOH1	Output Voltage High	2.4	-	V	IOH = -4.0mA
VOH2	Output Voltage High (Note 2)	VCC-0.4	-	V	IOH = 100µA
VIL	Input Voltage Low	0	0.8	V	
VIH	Input Voltage High	2.4	VCC	V	

Capacitance (Note 2)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	70	pF	f = 1MHz, VIN = VCC or GND
CIO	Input/Output Capacitance	25	pF	f = 1MHz, VIO = VCC or GND

NOTES: 1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns max.; Input and output timing reference level: 1.5V; Output Load: 1TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.

2. Tested at initial design and after major design changes.

3. Typical derating: 40mA/MHz increase in ICCOP.

4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C

NO.	SYMBOL		PARAMETER		HM-8816HB MIN	HM-8816HB MAX	HM-8816H MIN	HM-8816H MAX	UNITS	NOTES
READ CYCLE										
(1)	TAVAX	tRC	Read Cycle Time		70	-	85	-	ns	1, 4
(2)	TAVQV	tAA	Address Access Time		-	70	-	85	ns	1, 4
(3)	TELQV	tCE	Chip Enable Access Time		-	70	-	85	ns	1, 4
(4)	TELQX	tLZ	Chip Enable Output Enable Time		5	-	5	-	ns	2, 4
(5)	TEHQX		Chip Enable Output Hold Time		5	-	5	-	ns	2, 4
(6)	TAXQX	tOH	Address Ouptut Hold Time		5	-	5	-	ns	2, 4
(7)	TEHQZ	tHZ	Chip Disable Output Disable Time		0	40	0	40	ns	2, 4
WRITE CYCLE										
(8)	TAVAX	tWC	Write Cycle Time		70	-	85	-	ns	1, 4
(9)	TELWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	65	-	75	-	ns	1, 4
(10)	TELEH	tCW	Chip Enable to End of Write	$\overline{E}$ Controlled	65	-	75	-	ns	2, 4
(11)	TWLWH	tWP	Write Pulse Width		55	-	60	-	ns	1, 4
(12)	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	0	-	0	-	ns	1, 4
(13)	TAVEL	tAS	Address Setup Time	$\overline{E}$ Controlled	0	-	0	-	ns	2, 4
(14)	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10	-	10	-	ns	1, 4
(15)	TEHAX	tWR	Write Recovery Time	$\overline{E}$ Controlled	10	-	10	-	ns	2, 4
(16)	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	30	-	35	-	ns	1, 4
(17)	TDVEH	tDW	Data Setup Time	$\overline{E}$ Controlled	30	-	35	-	ns	2, 4
(18)	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	5	-	5	-	ns	1, 4
(19)	TEHDX	tDH	Data Hold Time	$\overline{E}$ Controlled	10	-	10	-	ns	1, 4
(20)	TWLQZ	tWZ	Write Enable Low to Output Off		-	40	-	40	ns	2, 4
(21)	TWHQX	tOW	Write Enable High to Output On		0	-	0	-	ns	2, 4

NOTES: 1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns max.; Input and output timing reference level: 1.5V; Output Load: 1 TTL gate equivalent and CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.

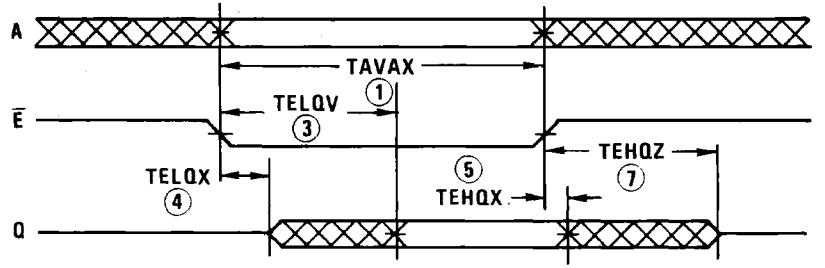
2. Tested at initial design and after major design changes.

3. Typical derating: 40mA/MHz increase in ICCOP.

4. VCC = 4.5V and 5.5V.

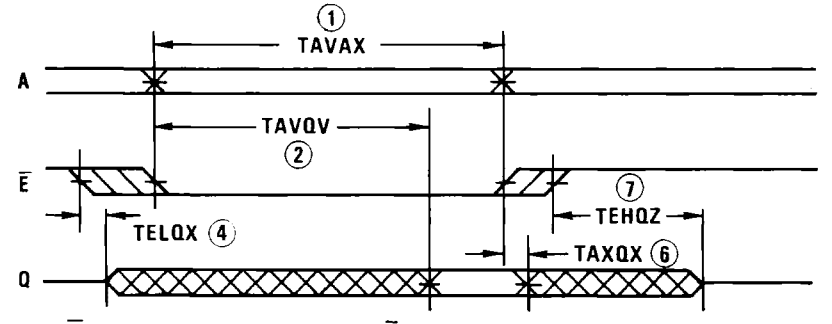
Timing Diagrams

READ CYCLE 1: CONTROLLED BY $\overline{E}$



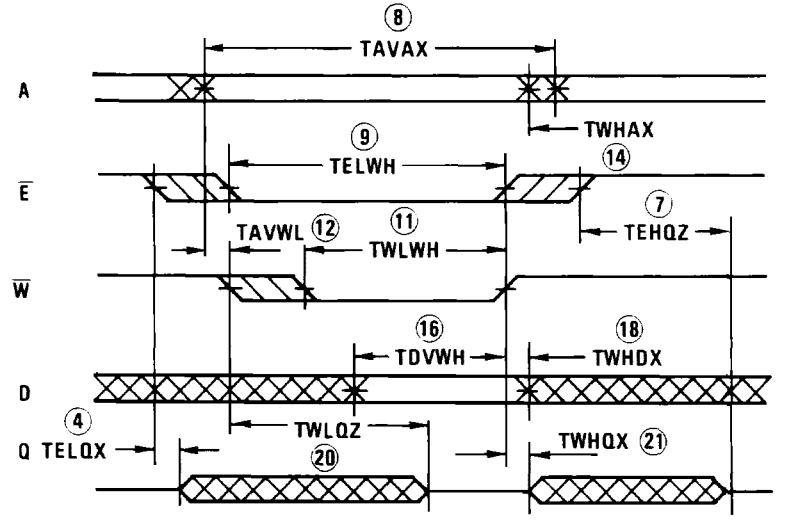
NOTE: $\overline{W}$ is held high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until $\overline{E}$ goes high.

READ CYCLE 2: CONTROLLED BY ADDRESS



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

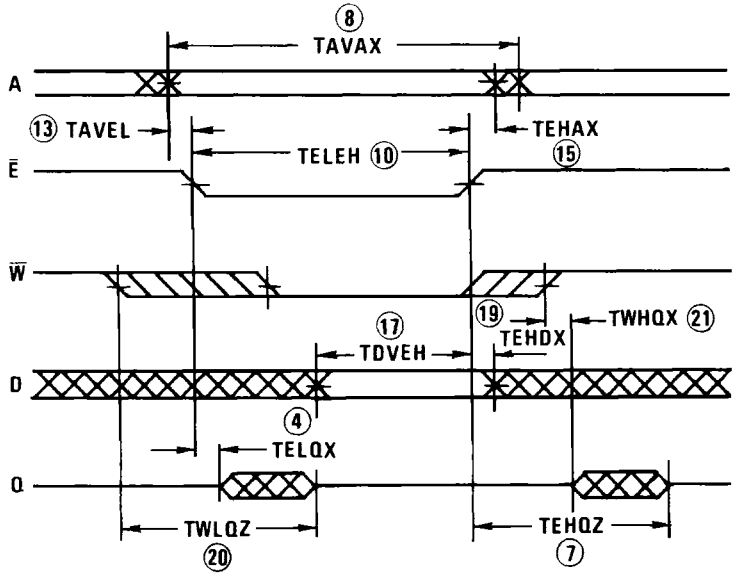
WRITE CYCLE 1: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are Low.

Timing Diagrams

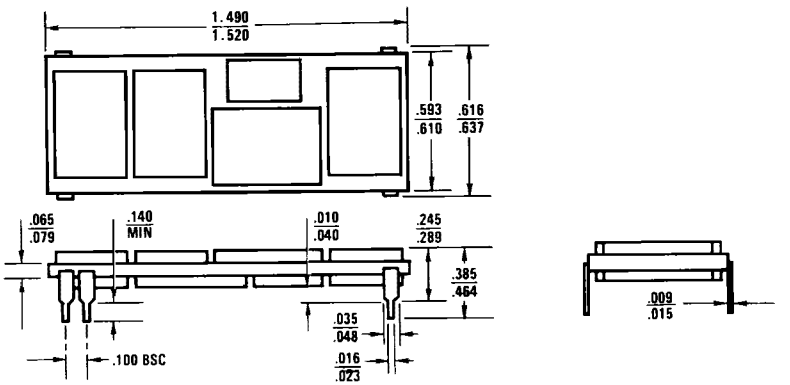
WRITE CYCLE 2: CONTROLLED BY $\overline{E}$ (EARLY WRITE)



NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$. If $\overline{W}$ falls before $\overline{E}$ by a time exceeding TWLQZ (Max) - TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) - TWHQZ (Min), then Q will remain in the high impedance state throughout the cycle. The address must remain stable whenever $\overline{E}$ and $\overline{W}$ are both low.

Packaging

28 PIN MODULE



NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.