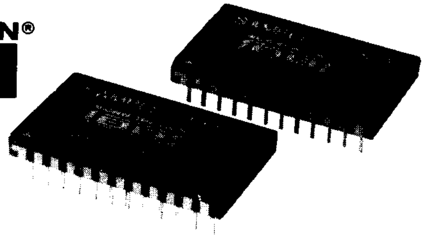
BURR-BROWN®



SHC601BH

Ultra-High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- 100MHz SAMPLE RATE
- ±0.02% MAX LINEARITY ERROR
- ACQUISITION TIME (2.5V STEP):
  1% FSR 8ns
  0.1% FSR 12ns
  0.02% FSR 22ns
- 350V/μs SLEW RATE
- 900 FEMTO SECONDS RMS APERTURE UNCERTAINTY
- REPLACES HTS-0010

APPLICATIONS

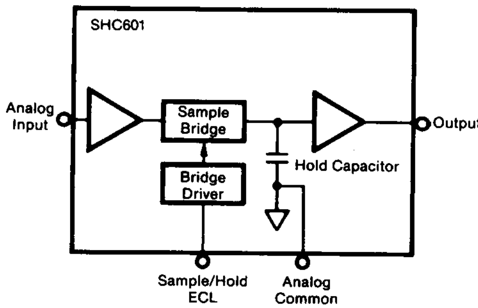
- IMPROVING FLASH ADCs
- WAVEFORM DIGITIZERS
- VIDEO PROCESSORS
- PEAK DETECTORS
- BOXCAR INTEGRATORS
- DOWN CONVERTERS
- DAC DEGLITCHING

DESCRIPTION

The SHC 601 is a high speed sample/hold amplifier designed for use in ultra-fast, 12-bit data acquisition and signal processing systems. It acquires input step changes of 2.5V to 1% accuracy in 8ns and 0.02% accuracy in 22ns, typically. The open-loop output amplifier provides a maximum linearity error of ±0.02% with an output impedance of 10Ω.

A 100MHz sample rate and extremely low aperture uncertainty (0.9ps rms) make the SHC601 suitable for RF signal processing applications.

In the sample (track) mode the SHC601 operates as a unity-gain buffer with a small signal bandwidth of 115MHz.



International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

PDS-784

SPECIFICATIONS

ELECTRICAL

At +25°C ambient temperature, 10 SCFM airflow, and rated power supplies unless otherwise specified.

PARAMETER	SHC601BH MIN	SHC601BH TYP	SHC601BH MAX	UNITS
SAMPLE/HOLD INPUTS				
ANALOG				
Voltage Range		±1.25	±2	V
R_{IN}		100		kΩ
Input Bias Current		25	75	µA
DIGITAL (ECL Compatible): V_{IH} (HOLD)	−1.1		−0.8	V
V_{IL} (SAMPLE)	−1.8		−1.5	V
I_{IH}, $V_{IN} = -1.1V$			265	µA
I_{IL}, $V_{IN} = -1.8V$	0.5			µA
SAMPLE/HOLD OUTPUT				
Voltage Range		±1.25	±2	V
Output Current	±40			mA
Short Circuit Protection		None		
Output Impedance (at DC)		10		Ω
Noise in Track Mode (wideband 100MHz into 50Ω load)		400		µVrms
SAMPLE/HOLD TRANSFER CHARACTERISTICS				
DC ACCURACY/STABILITY				
Gain, $R_L = \infty$ [1]	0.96	0.98	1.00	V/V
Gain Temperature Coefficient		±28	±40	ppm/°C
Linearity Error (±1.25V Input)		±0.0095	±0.02	% of FSR[2]
Zero Offset		±2	±5	mV
Temperature Coefficient		±80	±175	µV/°C
Power Supply Sensitivity of Offset: V_{DD1} (+5V)		±2		mV/V
V_{DD2} (−5.2V)		±4		mV/V
$+V_{CC}$ (+15V)		±11		mV/V
$-V_{CC}$ (−15V)		±20		mV/V
HOLD-TO-TRACK (SAMPLE) DYNAMICS; $R_L = 100Ω$, $C_L = 3pF$				
Acquisition Time (with 2.5V step)[2]: To within ±1% of FSR (25mV)		8	11	ns
To within ±0.1% of FSR (2.5mV)		12	16	ns
To within ±0.02% of FSR (0.5mV)		22		ns
Switch Delay Time		1.5		ns
TRACK (SAMPLE)-TO-HOLD DYNAMICS; $R_L = 100Ω$, $C_L = 3pF$				
Aperture Delay Time		4	7	ns
Aperture Uncertainty (jitter)		0.9		ps (rms)
Offset Step (pedestal)		±5	±20	mV
Temperature Coefficient		±50	±140	µV/°C
Sensitivity to V_{DD2} (−5.2V)		±0.6		mV/V
Switch Delay Time		1.5		ns
SwitchingTransient: Amplitude		7	25	mVpk
Settling to within ±1mV		9	14	ns
TRACK (SAMPLE) MODE DYNAMICS				
Frequency Response: Full Power Bandwidth (V_O = 2.5Vp-p)	38	45		MHz
Small Signal Bandwidth (V_O = 100mVp-p)	100	115		MHz
Output Slew Rate	±300	±350		V/µs
Harmonic Distortion (2Vp-p input at 20MHz): $R_L \geq 250Ω$		−55		dBC
HOLD MODE DYNAMICS				
Droop Rate: at +25°C case temp		±20	±100	µV/µs
at +85°C case temp		±0.9	±2	mV/µs
Feedthrough Rejection: 2.5Vp-p input; $R_L = 100Ω$, $C_L = 3pF$ at 10MHz	65	77		dB
POWER SUPPLY REQUIREMENTS				
Supply Voltages: V_{DD1}	+4.75	+5.0	+5.25	V
V_{DD2}	−4.95	−5.2	−5.4	V
$+V_{CC}$	+14.25	+15	+15.75	V
$-V_{CC}$	−14.25	−15	−15.75	V
Quiescent Current: V_{DD1} (+5V)		16	25	mA
V_{DD2} (−5.2V)		60	85	mA
$+V_{CC}$ (+15V)		30	40	mA
$-V_{CC}$ (−15V)		27	40	mA
Power Dissipation (I_{OUT} = 0mA)		1.25	1.7	W
TEMPERATURE RANGE				
Specification[3]	−25		+85	°C
Storage	−55		+125	°C

NOTES: (1) Gain Accuracy: Gain = R_L (0.98V/V)/(R_L + 10Ω). (2) FSR means Full-Scale Range. For SHC601 FSR= 2.5V. (3) SHC601BH is tested and specified in a forced air environment with a 10 SCFM airflow. For a normal convection environment θ_{JC} = 28.7°C/W and θ_{CA} = 23.3°C/W. Case temperature is measured on top surface of package.

PIN ASSIGNMENTS

1	V_{DD1} (+5V)	13	Analog Input
2	V_{DD2} (−5.2V)	14	NIC*
3	NIC*	15	NIC*
4	V_{DD2} (−5.2V)	16	NIC*
5	Hold Command	17	NIC*
6	Digital Common	18	Analog Common
7	Power Common	19	Analog Common
8	$+V_{CC}$ (+15V)	20	NIC*
9	NIC*	21	NIC*
10	V_{DD2} (−5.2V)	22	$+V_{CC}$ (+15V)
11	Power Common	23	NIC*
12	$-V_{CC}$ (−15V)	24	Analog Output

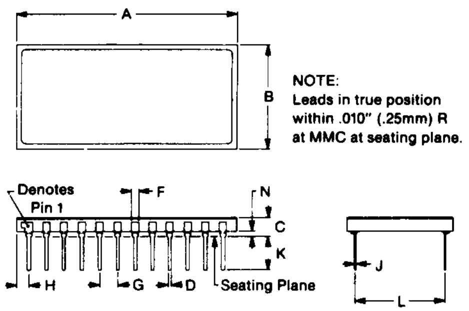
* NIC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	16.5V
V_{DD1}	+7.0V
V_{DD2}	−7.0V
Analog Input	±5.0V
Logic Input	V_{DD2} to +0.5V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	−40°C to +100°C

Stresses above these ratings may cause permanent damage to the device.

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.280	1.310	32.51	33.27
B	.780	.800	19.81	20.32
C	.153	.207	3.89	5.26
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.087	.091	2.21	2.31
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.600 BASIC		15.24 BASIC	
N	.015	.035	.38	.89

ORDERING INFORMATION

SHC601 B H Q

Basic Model Number — SHC601

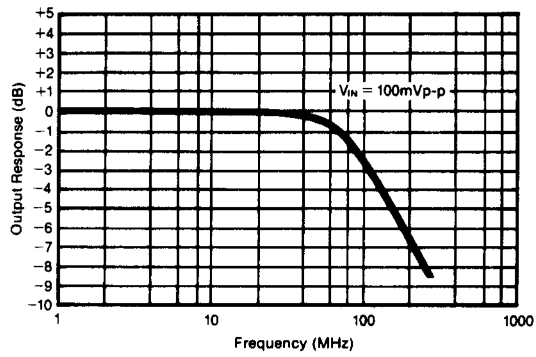
Performance Grade Code — B
B = −25°C to +85°C

Package — H
H = ceramic DIP

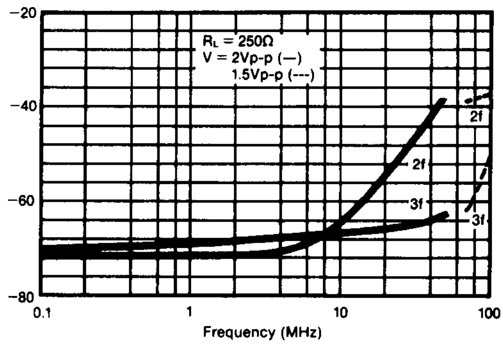
Reliability Screening — Q
Q = Q-screened

TYPICAL PERFORMANCE CURVES

ANALOG INPUT BANDWIDTH



HARMONIC DISTORTION VS FREQUENCY



THEORY OF OPERATION

The SHC601 is a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 8ns. The low-bias-current output buffer droop appears only as an offset error and does not affect linearity.

LAYOUT

Each power supply pin should be bypassed with a 1μF tantalum capacitor connected directly from each pin to a heavy copper ground plane. All unused pins should be connected to ground and input and output connections should be short and direct in keeping with the high frequency performance of the SHC601.

Good RF layout techniques should be used—a heavy two ounce copper ground plane is strongly recommended. Wire-wrap or "prototype" boards will not give satisfactory performance.

Longer input/output traces or capacitive loads (such as a flash ADC) may require decoupling with a series resistor of 10Ω to 50Ω.

DISCUSSION OF PERFORMANCE

HARMONIC DISTORTION

Figure 1 shows the harmonic distortion at various frequency ranges. Figure 2 is a block diagram of the Harmonic Distortion Test.

APERTURE JITTER

An ECL signal with rising and falling edges of 1V/ns is applied to both the S/H input and the analog input (see Figure 3). A delay line is used to compensate for the aperture delay time and can be made up of various coax lengths or by using a calibrated line such as an Allen Avionics Model VRM011. Because of the variation in the other cable lengths, coax (A) length may have to be adjusted to locate the sample and hold point at the midpoint of the signal transition.

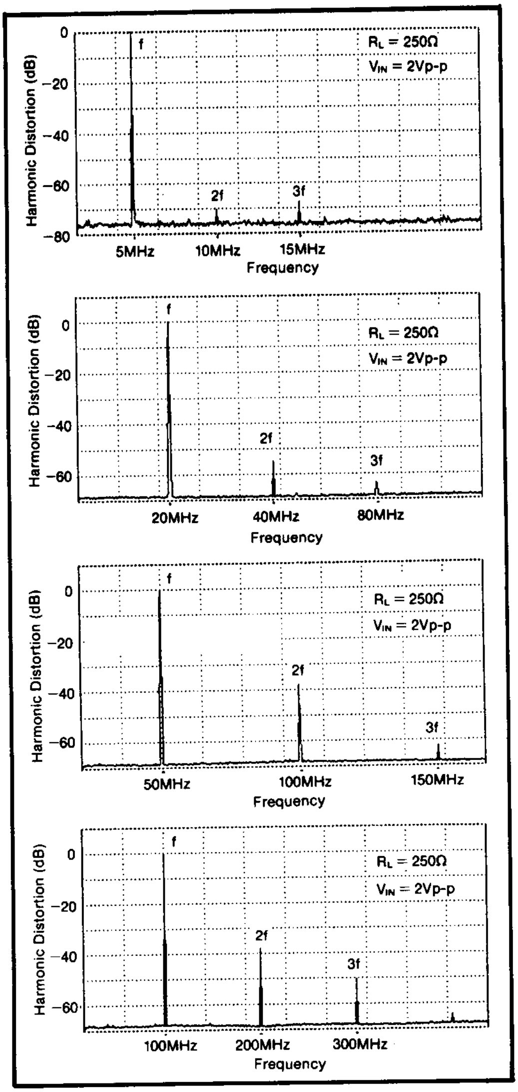


Figure 1. Harmonic Distortion vs Frequency.

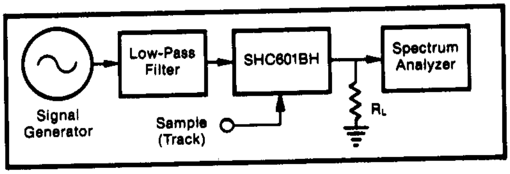


Figure 2. Harmonic Distortion Test Block Diagram.

In this test the midpoint of the ECL signal is held; approximately −1.3V. Once the cable delays have been adjusted, the scope presentation will consist of noise due to aperture jitter on the held value of −1.3V. The peak-to-peak value of the noise band around the held value, divided by four, gives the approximate rms value of the noise. When divided by the rate of change of the input signal, the result will be aperture jitter.

It is important that the rate of change used is the effective slew rate seen at the switching mechanism inside the SHC601. For example, this signal will be slower than the pulse generator slew rate due to the slew rate limitations of an input buffer. The effective slew rate is determined by measuring the amount the held value changes versus a known change in delay of the delay line.

For example:

Effective Slew Rate = 0.35V/ns

Noise band = 1.4mVp-p = 0.35mVrms

If rms noise is in mV and slew rate in V/ns, the jitter will be in ps rms:

(0.35mVrms) ÷ (0.35V/ns) = 1ps rms

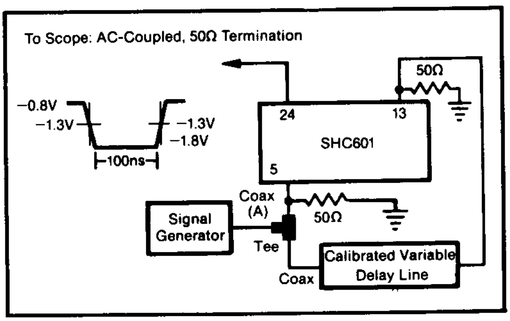


Figure 3. Aperture Jitter Test Circuit.