SYNCHRONOUS GRAPHICS RAM DIMM

MT2LG25664(K)H
MT4LG51264(K)H

FEATURES

- 144-pin, small-outline, dual in-line memory module (DIMM)
- 2MB (256K x 64) and 4MB (512K x 64)
- Fully synchronous; all signals registered on positive edge of system clock
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are LVTTL-compatible
- Internal pipelined operation; column address can be changed every clock cycle
- Programmable burst lengths: 1, 2, 4, 8 or full page
- BLOCK WRITE and WRITE-PER-BIT modes
- Independent byte operation via DQM0-7
- AUTO PRECHARGE and AUTO REFRESH modes
- 17ms, 1,024-cycle refresh (16.6µs/row)
- Optional Serial Presence-Detect (SPD)

OPTIONS

OPTIONS	MARKING
• Frequency	
83 MHz	-83
66 MHz	-66
• SPD	
With SPD	Blank
Without SPD	K
• Package	
144-pin Small-Outline DIMM (gold)	G

SGRAM COMPONENT KEY TIMING PARAMETERS

MODULE FREQUENCY	SPEED GRADE	ACCESS TIME	SET-UP TIMES	HOLD TIMES
83 MHz	10ns	9ns	3ns	1ns
66 MHz	12ns	11ns	3.5ns	1.5ns

PART NUMBERS

PART NUMBER	CONFIGURATION	OPTIONS
MT2LG25664HG-xx	256K x 64	SPD
MT2LG25664KHG-xx	256K x 64	
MT4LG51264HG-xx	512K x 64	SPD
MT4LG51264KHG-xx	512K x 64	

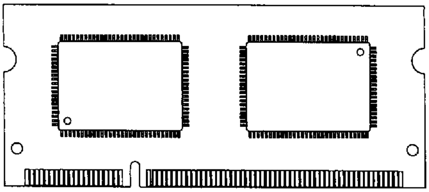
xx = frequency

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PIN ASSIGNMENT (Front View)

144-Pin Small-Outline DIMM

(DF-5) 256K x 64 (shown)
(DF-4) 512K x 64



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	Vss	2	Vss	73	NC/CLK1*	74	CLK0
3	DQ63	4	DQ62	75	Vcc	76	Vcc
5	DQ61	6	DQ60	77	RSVD	78	RSVD
7	DQ59	8	DQ58	79	NC (A11)	80	NC (A10)
9	DQ57	10	DQ56	81	A9	82	A8
11	Vcc	12	Vcc	83	A7	84	A6
13	DQ55	14	DQ54	85	Vss	86	Vss
15	DQ53	16	DQ52	87	A5	88	A4
17	DQ51	18	DQ50	89	A3	90	A2
19	DQ49	20	DQ48	91	A1	92	A0
21	Vss	22	Vss	93	Vcc	94	Vcc
23	DQMB7	24	DQMB6	95	DQ31	96	DQ30
25	DQMB5	26	DQMB4	97	DQ29	98	DQ28
27	Vcc	28	Vcc	99	DQ27	100	DQ26
29	DQ47	30	DQ46	101	DQ25	102	DQ24
31	DQ45	32	DQ44	103	Vss	104	Vss
33	DQ43	34	DQ42	105	DQ23	106	DQ22
35	DQ41	36	DQ40	107	DQ21	108	DQ20
37	Vss	38	Vss	109	DQ19	110	DQ18
39	DQ39	40	DQ38	111	DQ17	112	DQ16
41	DQ37	42	DQ36	113	Vcc	114	Vcc
43	DQ35	44	DQ34	115	DQMB3	116	DQMB2
45	DQ33	46	DQ32	117	DQMB1	118	DQMB0
47	Vcc	48	Vcc	119	Vss	120	Vss
49	RSVD	50	RSVD	121	DQ15	122	DQ14
51	RSVD	52	RSVD	123	DQ13	124	DQ12
53	RSVD	54	RSVD	125	DQ11	126	DQ10
55	Vss	56	Vss	127	DQ9	128	DQ8
57	DSF	58	RFU	129	Vcc	130	Vcc
59	RFU	60	RFU	131	DQ7	132	DQ6
61	RFU	62	SA0/NC**	133	DQ5	134	DQ4
63	Vcc	64	Vcc	135	DQ3	136	DQ2
65	NC/CS1*	66	CS0	137	DQ1	138	DQ0
67	RAS#	68	CAS#	139	Vss	140	Vss
69	WE#	70	CKE	141	SDA/NC**	142	SCL/NC**
71	Vss	72	Vss	143	Vcc	144	Vcc

* 4MB version only
** K version only

GENERAL DESCRIPTION

The MT2LG25664H and MT4LG51264H SGRAM modules are high-speed CMOS, dynamic random-access 2MB and 4MB memories organized in a small outline x64 configuration.

READ and WRITE accesses to the module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A8 select the row). Then the address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles and provide seamless high-speed random-access operation.

Synchronous graphics RAMs (SGRAMs) differ from synchronous DRAMs (SDRAMs) by providing an eight-column BLOCK WRITE function and a MASKED WRITE (or WRITE-PER-BIT) function to accommodate high-performance graphics applications. The BLOCK WRITE and MASKED WRITE functions may be combined with individual byte enables (DQ mask, or DQM, pins).

The CMOS dynamic memory structure of these modules is designed to operate in 3.3V, low-power memory systems. An AUTO REFRESH mode is provided along with a power-saving POWER-DOWN mode. All inputs and outputs are LVTTL-compatible. (Reference MT41LC256K32D4 SGRAM data sheet for additional information on SGRAM functionality.)

RESISTOR STRAPPING DETECTION

Three resistor straps are used to indicate the module frequency and timing. Table 1 shows the settings. A logic LOW (i.e. 0) indicates the strapping resistor is tied to Ground (Vss). A logic HIGH (i.e. 1) indicates that the strapping resistor is tied to Vcc.

SERIAL PRESENCE-DETECT OPERATION

These modules can also incorporate Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(0), which provide two unique DIMM/EEPROM addresses.

Table 1

MODULE FREQUENCY	DQ31	DQ30	DQ29
66 MHz	0	0	0
83 MHz	0	0	1

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the serial PD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

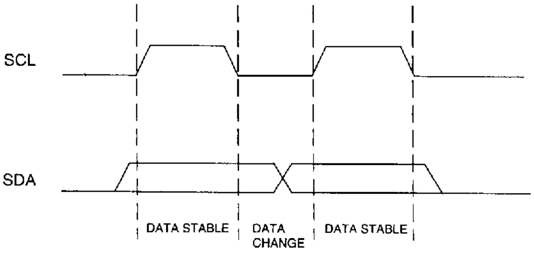


Figure 1
DATA VALIDITY

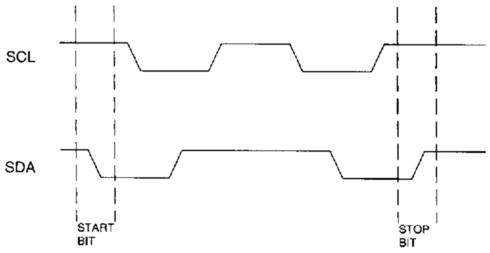


Figure 2
DEFINITION OF START AND STOP

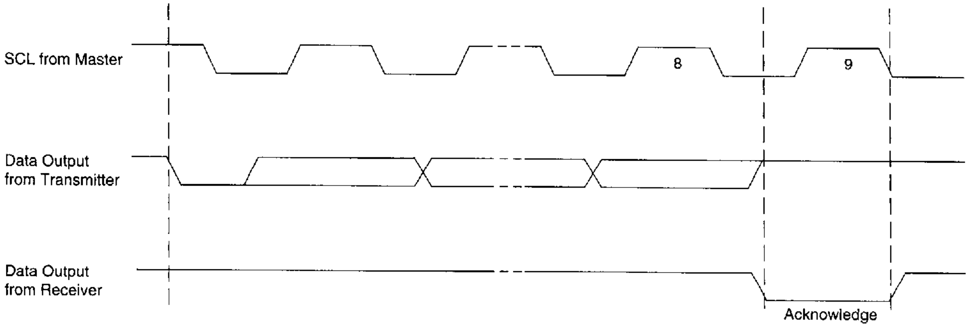
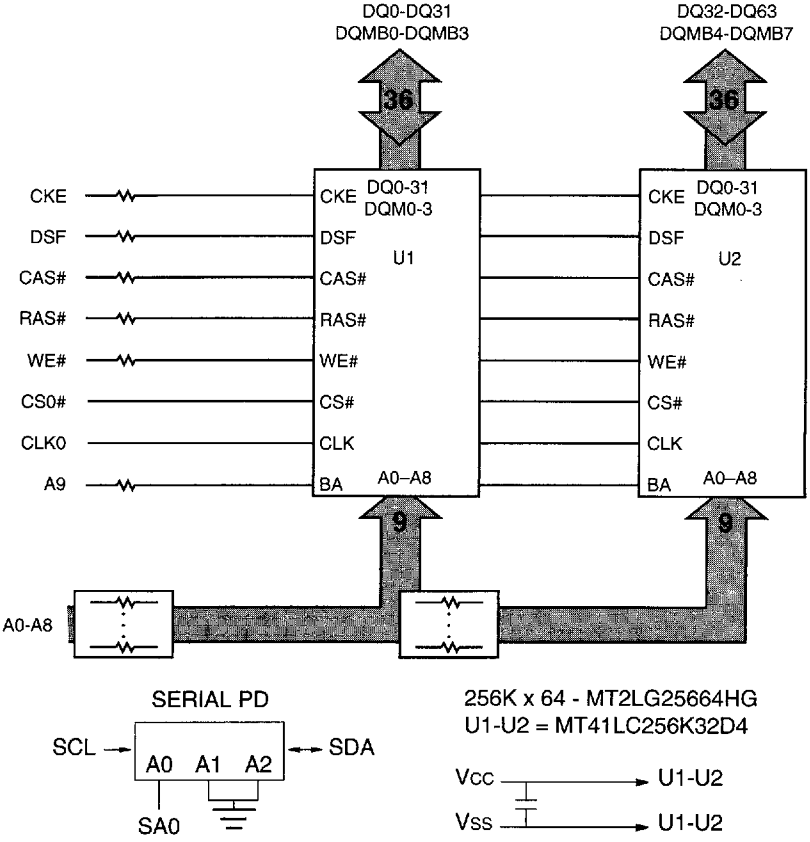


Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

NEW SGRAM SODIMM

FUNCTIONAL BLOCK DIAGRAM
MT2LG25664H (2MB)



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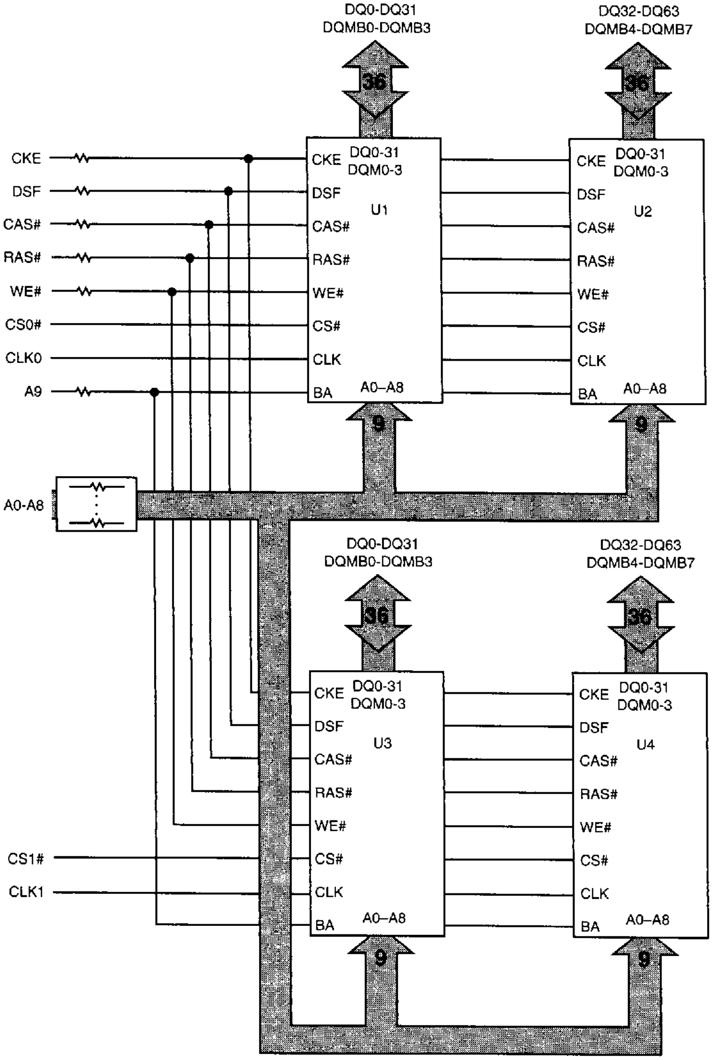
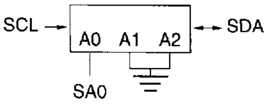
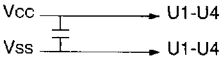
FUNCTIONAL BLOCK DIAGRAM
MT4LG51264H (4MB)



SERIAL PD



512K x 64 - MT4LG51264HG
U1-U4 = MT41LC256K32D4



PIN DESCRIPTIONS

MODULE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
73, 74	CLK0, CLK1	Input	Clock: CLK is driven by the system clock. All SGRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
70	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. After both banks are precharged, deactivating the clock provides POWER-DOWN mode and SELF REFRESH mode. CKE is synchronous except after the device enters POWER-DOWN and SELF REFRESH modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during POWER-DOWN and SELF REFRESH modes, providing low standby power. CKE may be tied HIGH.
65, 66	CS0#, CS1#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
57, 67-69	RAS#, CAS# DSF, WE#	Input	Command Inputs: RAS#, WE#, CAS#, and DSF define the command being entered.
23-26, 115-118	DQMB0-DQMB7	Input	Input/Output Mask: DQMB0-DQMB3 are byte specific, nonpersistent I/O buffer controls. The I/O buffers are placed in a High-Z state when DQMB is sampled HIGH. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. Output data is masked (two-clock latency) when DQMB is sampled HIGH during a READ cycle. DQMB0 masks DQ0-DQ7, DQMB1 masks DQ8-DQ15, DQMB2 masks DQ16-DQ23, and DQMB3 masks DQ24-DQ31. This pattern repeats for the remaining DQMBs.
81	A9 (BA)	Input	Bank Address: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the 10th bit of the MODE and SPECIAL MODE registers.
82-84, 87-92	A0-A8	Input	Address Inputs: A0-A8 are sampled during the ACTIVE command (row-address A0-A8) and READ/WRITE command (column-address A0-A7 with A8 defining AUTO PRECHARGE) to select one location out of the 128,000 available in the respective bank. A8 is sampled during a precharge command to determine if both banks are to be precharged (A8 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER or LOAD SPECIAL MODE REGISTER command.
3-10, 13-20, 29-36, 39-46, 95-102, 105-112, 121-128, 131-138	DQ0-DQ63	Input/ Output	Data I/O: Data bus. The I/Os are byte-maskable during READs and WRITEs.The DQs also serve as column/byte mask inputs during BLOCK WRITEs.
141	SDA	Input/ Output	Serial Presence-Detect Data. SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
142	SCL	Input	Serial Clock for Presence-Detect. SCL is used to synchronize the presence-detect data transfer to and from the module.
62	SA0	Input	Presence-Detect Address Input. This pin is used to configure the presence-detect device.

PIN DESCRIPTIONS (Continued)

MODULE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
11, 12, 27, 28, 47, 48, 63, 64, 75, 76, 93, 94, 113, 114, 129, 130,143, 144	Vcc	Supply	Power Supply: +3.3V ±0.3V.
1, 2, 21, 22, 37, 38, 55, 56, 71, 72, 85, 86, 103, 104, 119, 120, 139, 140,	Vss	Supply	Ground
58-61	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
49-54, 77, 78	RSVD	—	RSVD: These pins are reserved.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .... -1V to +4.6V
Voltage on Inputs or I/O pins
relative to V_{SS} .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Note: 1) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC} +0.3	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.3	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-8	8	µA	15
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-20	20	µA	15
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

Icc SPECIFICATIONS AND MAXIMUM LIMITS

(Notes: 1, 8, 14) (V_{CC} = +3.3V ±0.3V)

			MAX			
PARAMETER/CONDITION	SYMBOL	SIZE	-83	-66	UNITS	NOTES
STANDBY CURRENT: POWER-DOWN mode, CKE ≤ V_{IL} (MAX), both banks idle	I_{CC1}	2MB 4MB	3 6	3 6	mA	
STANDBY CURRENT: CS# ≥ V_{IH} (MIN), ${}^{t}CK \geq {}^{t}CK$ (MIN), CKE ≥ V_{IH} (MIN), both banks idle	I_{CC2}	2MB 4MB	90 93	80 83	mA	3, 4, 13
STANDBY CURRENT: CS# ≥ V_{IH} (MIN), ${}^{t}CK \geq {}^{t}CK$ (MIN), CKE ≥ V_{IH} (MIN), both banks active after ${}^{t}RCD$ met	I_{CC3}	2MB 4MB	110 113	100 103	mA	3, 4, 13
AUTO REFRESH CURRENT (${}^{t}RC = {}^{t}RC$ [MIN])	I_{CC4}	2MB 4MB	220 223	190 193	mA	4, 13
OPERATING CURRENT: ACTIVE mode, burst = 2, READ or WRITE, ${}^{t}RC \geq {}^{t}RC$ (MIN), one bank active	I_{CC5}	2MB 4MB	290 293	260 263	mA	3, 4, 13
OPERATING CURRENT: ACTIVE mode, burst = 2, READ or WRITE, ${}^{t}RC \geq {}^{t}RC$ (MIN), two banks active	I_{CC6}	2MB 4MB	440 443	360 363	mA	3, 4, 13
OPERATING CURRENT: BURST mode, full-page burst after ${}^{t}RCD$ met READ or WRITE, ${}^{t}CK \geq {}^{t}CK$ (MIN), other bank idle	I_{CC7}	2MB 4MB	360 363	320 323	mA	3, 4, 13
OPERATING CURRENT: BLOCK WRITE ${}^{t}CK \geq {}^{t}CK$(MIN), ${}^{t}BWC \geq {}^{t}BWC$(MIN), one bank active	I_{CC8}	2MB 4MB	290 293	260 263	mA	3, 4, 13

CAPACITANCE

PARAMETER	SYMBOL	2MB	4MB	UNITS	NOTES
Input Capacitance: A0-A8, A9 (BA)	C_{I1}	12	24	pF	2
Input Capacitance: RAS#, CAS#, WE#, CKE, DSF	C_{I2}	14	28	pF	2
Input Capacitance: CS0#, CS1#, CLK0, CLK1	C_{I3}	14	14	pF	2
Input Capacitance: DQMB0-DQMB7	C_{I4}	8	16	pF	2
Input Capacitance: SCL, SA0	C_{I5}	6	6	pF	2
Input/Output Capacitance: DQ0-DQ63, SDA	C_{IO}	9	18	pF	2

SGRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

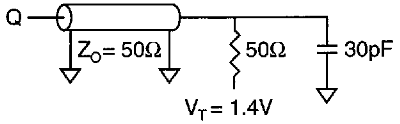
(Notes: 6, 7, 8, 9, 10, 12) Listed alphabetically by symbol subscript.

AC CHARACTERISTICS			-10 (83 MHz)		-12 (66 MHz)			
PARAMETER		SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (positive edge)		^{t}AC		9		11	ns	
Address hold time		^{t}AH	1		1.5		ns	
Address setup time		^{t}AS	3		3.5		ns	
BLOCK WRITE to PRECHARGE delay		^{t}BPL	3		3		^{t}CK	
BLOCK WRITE cycle time		^{t}BWC	2		2		^{t}CK	
CS#, RAS#, CAS#, WE#, DSF, DQM hold time		^{t}CH	1		1.5		ns	
CLK high level width		^{t}CHI	3.5		4		ns	
System clock cycle time	CAS# Latency = 2	^{t}CK	15		18		ns	
	CAS# Latency = 3	^{t}CK	10		12		ns	
CKE hold time		^{t}CKH	1		1.5		ns	
CKE setup time		^{t}CKS	3		3.5		ns	
CLK low level width		^{t}CL	3.5		4		ns	
CS#, RAS#, CAS#, WE#, DSF, DQM setup time		^{t}CS	3		3.5		ns	
Data-in hold time		^{t}DH	1		1.5		ns	
Data-in setup time		^{t}DS	3		3.5		ns	
Data-out high-impedance time		^{t}HZ		10		10	ns	11
Data-out low-impedance time		^{t}LZ	3		3		ns	
LOAD MODE REGISTER command to command		^{t}MTC	2		2		^{t}CK	
Data-out hold time		^{t}OH	4		4		ns	
ACTIVE to PRECHARGE command period		^{t}RAS	60	120,000	72	120,000	ns	
AUTO REFRESH and ACTIVE to ACTIVE command period		^{t}RC	90		108		ns	
ACTIVE to READ, WRITE or BLOCK WRITE delay		^{t}RCD	20		24		ns	
Refresh period (1,024 cycles)		^{t}REF		17		17	ms	7
PRECHARGE command period		^{t}RP	30		36		ns	
ACTIVE bank A to ACTIVE bank B command period		^{t}RRD	20		24		ns	
LOAD SPECIAL MODE REGISTER command to command		^{t}SML	2		2		^{t}CK	
Transition time		^{t}T	1	30	1	30	ns	
Write recovery time		^{t}WR	2		2		^{t}CK	

*Specifications for the SGRAM components used on the modules.

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V ±0.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
7. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 1ns.
9. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
10. Outputs measured at 1.4V with equivalent load:



11. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The last valid data element will meet ^{t}OH before going HIGH-Z.
12. AC timing tests have VIL = 0V and VIH = 3V with timing referenced to 1.4V crossover point.
13. Control, address, and data inputs transition (to TTL levels) no more than once during the clock period.
14. Icc specifications are tested after the device is properly initialized.
15. 2MB module values will be half of those shown.