HARRIS SEMICONDUCTOR

GP511

July 1996

Radiation Hardened 8-Bit Level Converter

Features

- Electrically screened to SMD #5962R9673601VXC
- Devices QML Qualified in Accordance with MIL-PRF-58535, Level V
- Radiation Hardened to 100K RADs (Si)
- Latch-Up Free Under Any Conditions
- Eight Inverting Channels with Conversion from V_{DD} to V_{CC} or V_{CC} to V_{DD}
  - ($4V \leq V_{DD} \leq 10V$ and $4V \leq V_{CC} \leq V_{DD}$)
- Four Operating Modes
  - CMOS to TTL Level Conversion
  - TTL to CMOS Level Conversion
  - Interface Off, High Impedance On Both Sides
  - Buffer, No Conversion
- Full Military Temperature Range Operation
- Low Propagation Delay Time
  - CMOS to TTL. . . . . 18ns (Typ)
  - TTL to CMOS. . . . . 25ns (Typ)
  - V_{DD} = 10V, V_{CC} = 5V
- High TTL Sink Current. . . . . 11mA (Typ)
- No External TTL Input Pull-Up Resistors Required
- High Speed Drive of Large Data Bus Capacitance
- Input/Output and Power Supply Terminals Located for Ease of PC Board Layout
- CMOS/SOS Processing

Applications

- Interface CMOS Microprocessor with TTL Memories and Peripheral Devices
- Interface Between and Within Logic Systems which Combine CMOS and TTL Devices

Description

The Harris GP511 is a high speed 8-bit, integrated circuit designed to interface CMOS logic levels with TTL logic levels on the data bus of microprocessor-based systems. CMOS/TTL interface is provided by eight parallel bidirectional buffer/level converters. Buffer INPUT/OUTPUT terminals are either inputs or outputs depending on the desired direction of data flow.

A low level on the DISABLE input with the ENABLE input either high or low permits conversion of CMOS inputs to TTL outputs. A high level on both the DISABLE and ENABLE inputs permits data flow from TTL inputs to CMOS outputs. A low level on the ENABLE input and high level on the DISABLE input sets both inputs/outputs to the high impedance state.

The TTL INPUT/OUTPUT terminals and the ENABLE and DISABLE control inputs are TTL compatible without the use of external pull-up resistors. The TTL input logic 0 to logic 1 transition occurs at a level of approximately 1.5V. The ENABLE and DISABLE inputs may be driven to the V_{DD} rail, therefore, either TTL or CMOS logic drivers capable of sinking one TTL load, may be used to determine the direction of data flow. The large CMOS and TTL output buffers in this device have a high output sink and source current capability and can drive the data bus capacitance with a transition time of approximately 0.25ns/pF. This fast output transition time, together with the small propagation delay time of the device, allow high speed operation.

Lead 16 is an additional V_{SS} lead which is connected directly to the TTL to CMOS converters to avoid oscillation in these amplifiers. Lead 16 is connected to lead 14 through a polysilicon resistor which isolates lead 16 from V_{SS} switching noise (ground noise).

These devices are QML approved and are processed and screened in full compliance with MIL-PRF-38535. **Detailed electrical specifications are contained in SMD 5962R9673601VXC, available on the Harris Website or AnswerFAX systems (document # 967360).**

Ordering Information

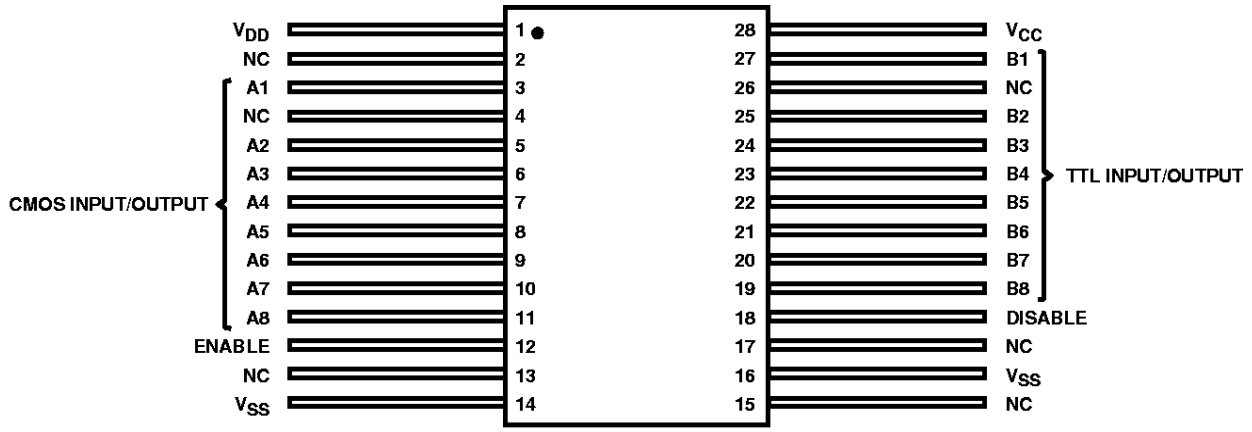
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
GP511K1RZ	-55 to 125	28 Ld Ceramic Flatpack	CDFP3-F28
GP511K/SAMPLE	25	28 Ld Ceramic Flatpack	CDFP3-F28

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

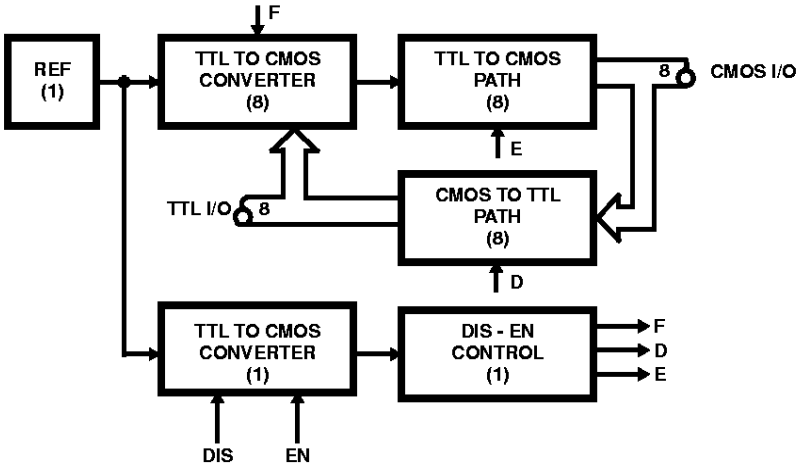
File Number **4128**

Pinout

GP511K1RZ (CERAMIC FLATPACK)
TOP VIEW



Functional Block Diagram

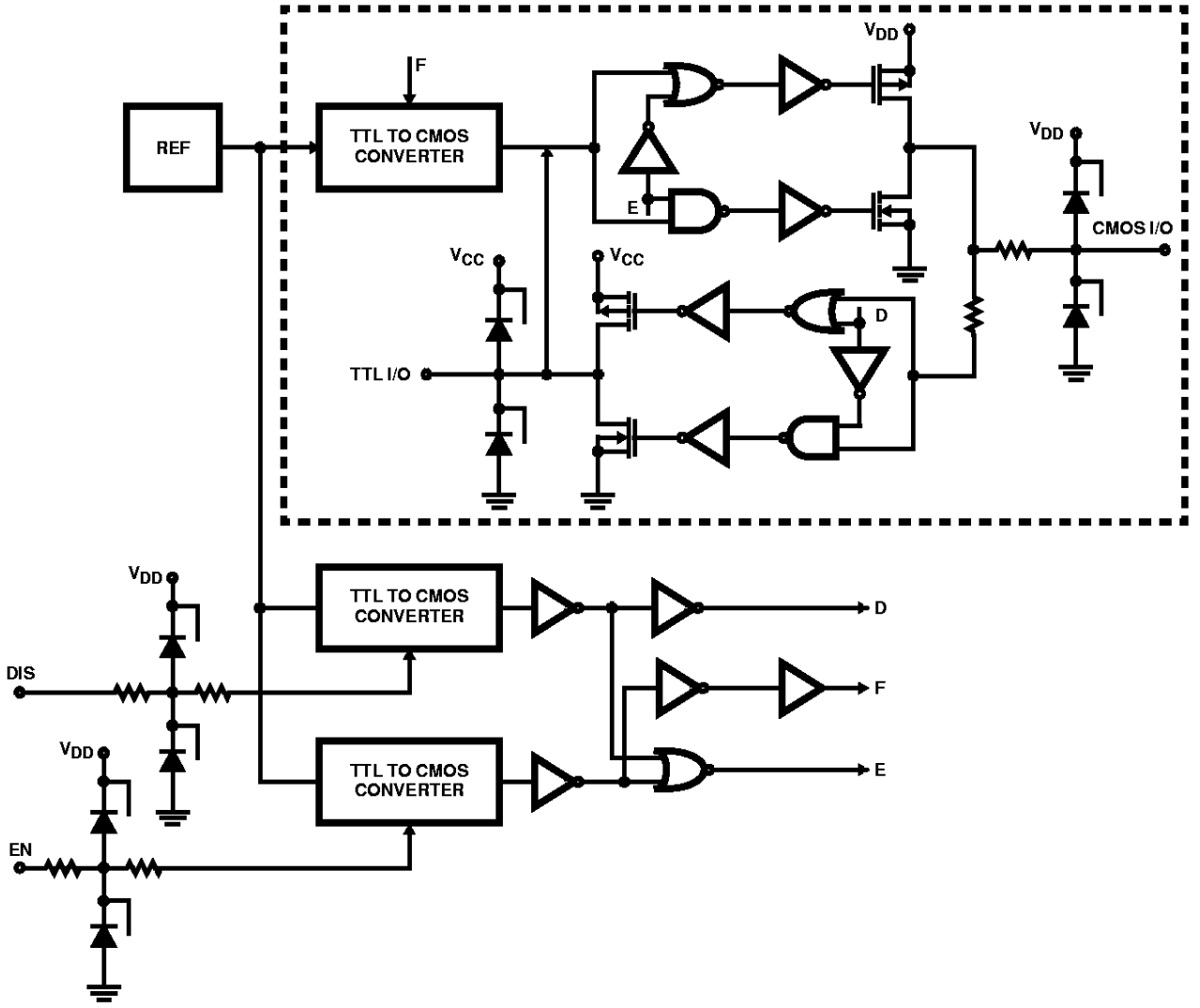


TRUTH TABLE

ENABLE	DISABLE	FUNCTION
X	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z) on Both CMOS and TTL Sides.

0 = Low Level, 1 = High Level, X = Don't Care

Logic Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{DD}	Powers the CMOS output stage.
3, 5, 6, 7, 8, 9, 10, 11	A1 thru A8	CMOS inputs or outputs depending on direction of data flow.
12	ENABLE	Used to control device function. (Refer to Truth Table)
14, 16	V_{SS}	Device ground.
18	DISABLE	Used to control device function. (Refer to Truth Table)
19, 20, 21, 22, 23, 24, 25, 27	B1 thru B8	TTL inputs or outputs depending on direction of data flow.
28	V_{CC}	Powers the TTL output stage.
2, 4, 13, 15, 17, 26	NC	No internal connection.

Die Characteristics

DIE DIMENSIONS:
100 mils x 88 mils

METALLIZATION:
Type: AlSi
Thickness: 11kÅ ±1kÅ

SUBSTRATE POTENTIAL:
Insulated

BACKSIDE FINISH:
Sapphire

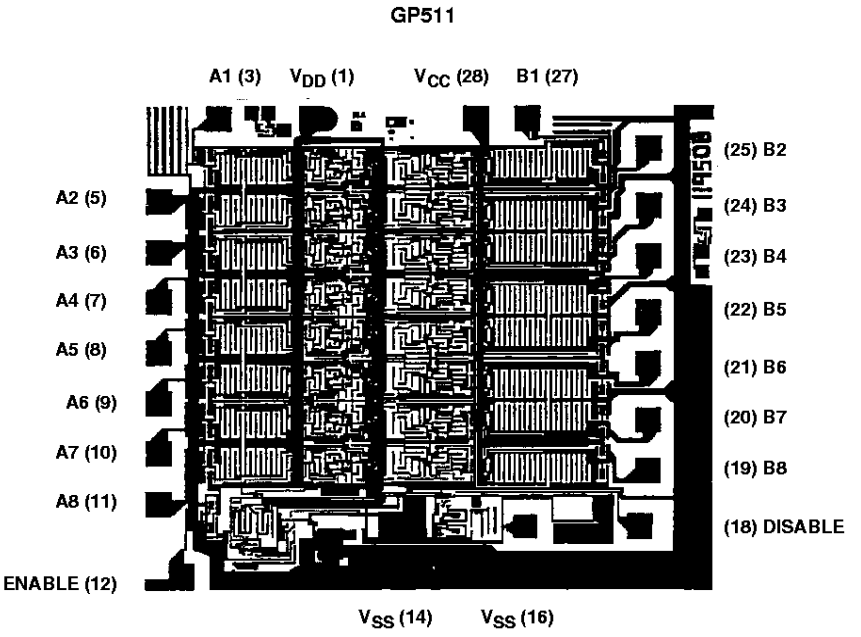
PASSIVATION:
Type: SiO_2
Thickness: 13kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:
2.0×10^5 A/cm^2

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

PROCESS:
SOS

Metallization Mask Layout



All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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