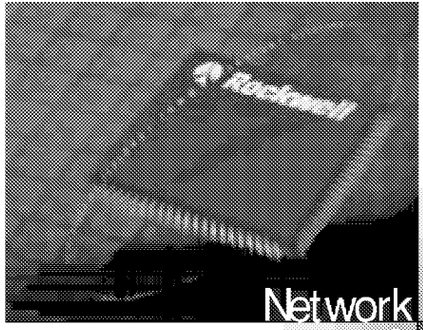


Network access

RS825x
155 Mbps ATM PHY

product brief

PROVIDING

HIGH

SPEED

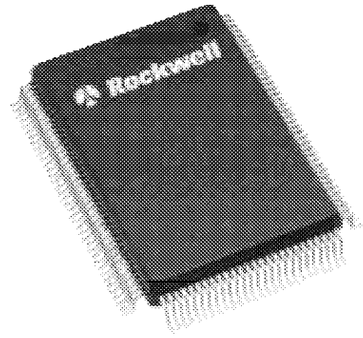
MULTIMEDIA

CONNECTIONS

155 Mbps ATM PHY with

Clock Recovery and UTOPIA Level 2

Rockwell's RS825x family of PHYs with UTOPIA (Universal Test and Operations Physical Interface ATM) Level 2 interface provides ATM service termination according to ATM Forum, ITU, and ANSI standards. In addition, the RS825x delivers HEC alignment operation for ATM cell streams SONET format per the ATM Forum UNI standards. This single-chip solution is perfect for applications in ATM LAN and WAN equipment, and ATM switches.



The RS825x family consists of 6 devices in two categories, WAN and LAN:

WAN Device No.	Number of Ports	LAN Device No.
RS8250	one port	RS8251
RS8252	two ports	RS8253
RS8254	four ports	RS8255

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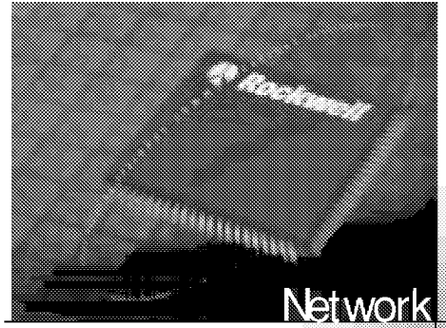

Network access

PROVIDING

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RS825x

155 Mbps ATM PHY

Compliant Functionality

The RS825x host interface consists of an ATM Forum-compliant UTOPIA Level 2 interface with a four-cell FIFO and multiple PHY addressing. The ATM Forum-compliant WIRE line interface delivers full functionality for Physical Media Dependent (PMD) devices such as fiber or Cat 5 UTP. The PMD interface block can provide or synchronize to an 8 KHz frame, 19.44 MHz byte or 155.52 MHz bit clock.

The RS825x has an extensive SONET overhead processing block with an integral HDLC controller for message processing over SONET section overhead bits D1, D2, and D3. The RS825x has all the necessary counters for capturing SONET and ATM error events as specified by the ATM Forum for both B-ICI and UNI interfaces. The RS825x ATM cell framer block provides for ATM cell HEC generation, checking, and alignment operations.

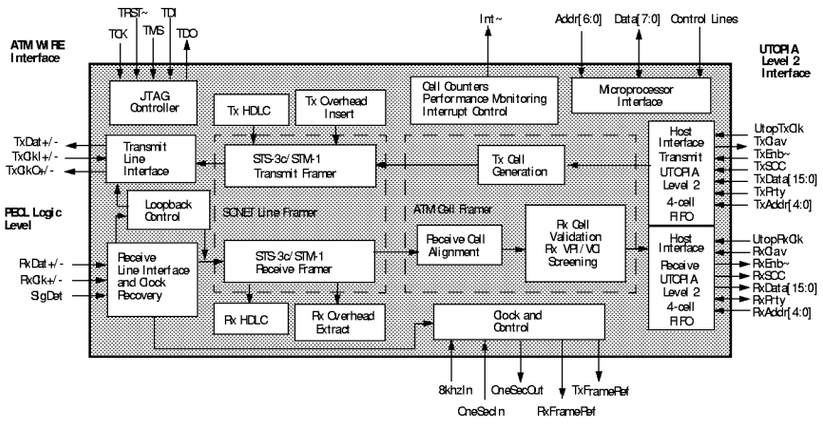
The RS825x's diagnostic capabilities include the ability to corrupt BIP-8 parity generation, source loopback at the SONET framer, and line loopback at the WIRE PMD interface. The RS825x's built-in JTAG port allows for easy diagnostics. The microprocessor control interface emulates an 8-bit SRAM.

Line Interface

- ATM Forum WIRE interface specification-compliant
- PECL I/O, compatible with PMD optical and UTP interface devices
- Clock recovery from NRZ input data
- Recovery of receive-octet alignment and octet clock from F6/28 framing patterns
- Select transmit clock from input or recovered receive clock
- PMD (line) and Framer (source) loopbacks for diagnostic testing
- Loss of Signal (LOS) detection

UTOPIA Level 2 Interface

- PHY cell to UTOPIA interface
- 50 MHz maximum data rate
- 8/16-bit data path interface
- Multi-PHY support
- Mode-compatible with UTOPIA Level 1
- Configurable cell buffer depth



RS8250 Block Diagram

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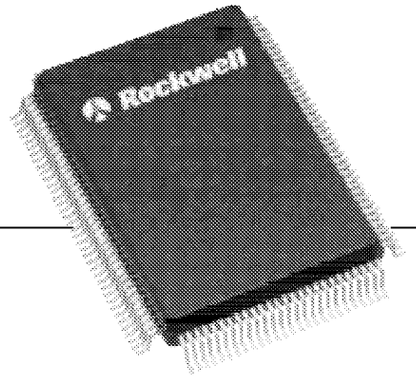


SONET STS-3c/STM-1 Framer

Overhead-Section octets supported

	Transmit	Receive
A1/A2	F6/28 or disable 00	Monitor out-of-frame state machine
J0	01 or 64-byte trace buffer	Monitor Rx trace buffer, interrupt on change
Z0, Z0	02, 03 or via register	Not checked
B1	Calculated, error insertion	Checked, errors counted
D1, D2, D3	HDLC data link formatter (WAN only)	HDLC data link formatter (WAN only)

Data Link Features (WAN only)

- Internal HDLC formatter provided to service 192 kbps data link
- Provides all bit-level processing
- Zero insertion and deletion
- Flag generation and detection
- Abort generation and detection
- 16/32-bit CRC calculation and checking
- 8-octet transmit and receive buffers
- Control/status register interface to local processor
- Example software drivers available

Overhead-Line octets supported

	Transmit	Receive
H1/H2	620A/93FF pointer	Full GR253 pointer processor
H3	Set to 00	Used in pointer processor
B2	Calculated, error insertion	Checked, errors counted
K1/K2	Insertable, via register	Checked, interrupt on change (WAN only)
S1	Insertable, via register	Checked, interrupt on change (WAN only)
M1	Line FEBE inserted	Checked, errors counted

Overhead-Path octets supported

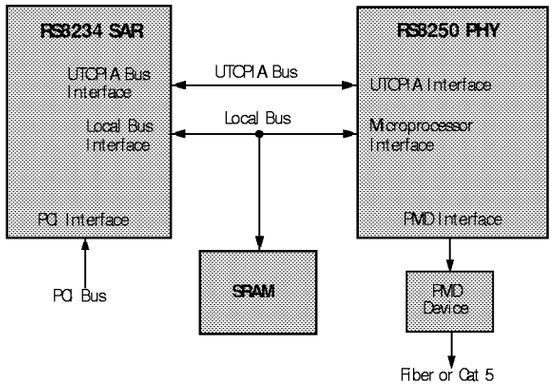
	Transmit	Receive
J1	00 or 64-byte trace buffer	Monitor Rx trace buffer, Interrupt on change
B3	Calculated, error insertion	Checked, errors counted
C2	13 hex for ATM mapping	Checked for 01 or 13
G1	Path FEBE, RDI inserted	Checked, errors counted, status

Support for Automatic Protection Switching (APS) (WAN only)

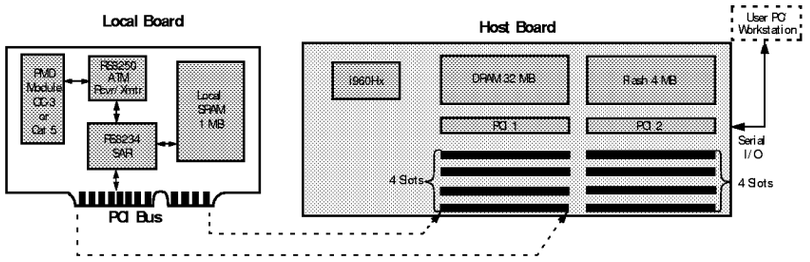
- Register control allows for support of APS
- K1/K2 Transmit control register allows transmission of any value
- Separate control bits for AIS, line FERF
- K1/K2 receive status register allows observation of incoming octet values
- Maskable interrupt on any change in received value
- Software interrupt routine can easily implement APS protocol
- Signal Fail/Signal Detect BER threshold monitoring

SONET Framer Functions

- Recovers frame location using F6/28 framing patterns
- Processes pointer to locate payload envelope
- Provides OOF, LOP, AIS status
- Provides frame and payload position information to other blocks
- Generates clocks and frame counters
- Maps cell data into payload envelope
- Generates all section, line, and path overhead and alarms
- Scrambles data for transmission
- Detects and integrates alarms for reporting in status registers
- Detects BIP and FEBE errors for error counters
- Recovers HDLC data link. (WAN only)



RS8250 Application Block Diagram



RS8250 EVS ATM Evaluation System Block Diagram

Cell Alignment Framer

- Recovers cell alignment from HEC
- Performs HEC error correction
- Matches idle/desired cell headers and generates write strobes and cell sync for UTOPIA interface
- Generates cell status bits, cell counts, and error counts
- Reads cell data from UTOPIA FIFO
- Inserts headers and generates HEC
- Inserts idle cells when no traffic is ready

Control and Status

Microprocessor Interface

- SRAM-like interface mode with high-performance or low-power access selection
- Glueless Bt8230/3 and RS8234 SAR interface mode
- 8-bit data bus
- Open-drain interrupt output

Counters/Status and Interrupt Registers

- Summary interrupt indications
- Configuration of interrupt enables
- One-second status latching
- One-second counter latching

Evaluation Systems

Rockwell developed the RS8250 ATM Evaluation System (EVS) to provide full evaluation capability for the RS8250 PHY chip. This system also serves as a reference design, which greatly shortens the total design cycle time for ATM system designers. The RS8250EVS is a full-scale platform, which can be used to facilitate development of embedded system designs.

The RS8250EVS consists of a complete ATM UNI interface on a PCI card (the RS8250EVM) and a host processor board with dual PCI buses mounted in a chassis with power supply and integral system software. A total of eight PCI slots are provided. The system board is manufactured by Cyclone Microsystems.

Features and Specifications

Product Features

- ATM Forum WIRE PMD interface
- Clock recovery, conforms to GR-253-CORE jitter requirements (WAN only)
- 8K, 19.44M or 155.52M selectable sync inputs and outputs
- UTOPIA Level 2 interface
- HDLC controller
- Multi-PHY capability (1,2 or 4)
- 3.3V power supply
- SONET overhead processing (UNI & B-ICI fields supported)
- Glueless interface to the Bt8230/3 and RS8234 SARs
- Microprocessor interface emulates an 8-bit SRAM with 32-bit aligned addressing
- 24-bit internal statistics counters
- Package: 128 TQFP (RS8250/1 only)
- Industrial temperature range (-40º to 85º C)
- JTAG compliant

Applications

- ATM WAN ports
- ATM switches
- ATM LAN equipment

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