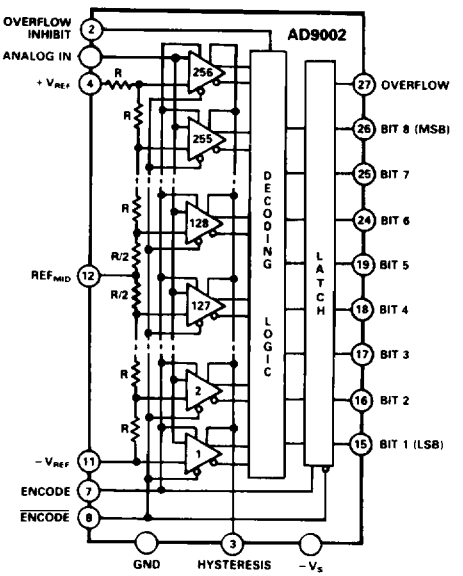
High Speed 8-Bit Monolithic A/D Converter

AD9002

FEATURES
150MSPS Encode Rate
Low Input Capacitance: 17pF
Low Power: 750mW
−5.2V Single Supply
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Radar Systems
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9002 is an 8-bit, high speed, analog-to-digital converter. The AD9002 is fabricated in an advanced bipolar process which allows operation at sampling rates in excess of 150 megasamples/second. Functionally, the AD9002 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the ECL compatible output latches.

An exceptionally wide large signal analog input bandwidth of 160MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9002 allows very accurate acquisition of high speed pulse inputs, without an external track-and-hold. The comparator output decoding scheme minimizes false codes which is critical to high speed linearity.

The AD9002 provides an external hysteresis control pin which can be used to optimize comparator sensitivity to further improve performance. Additionally, the AD9002's low power dissipation of 750mW makes it usable over the full extended temperature range. The AD9002 also incorporates an overflow bit to indicate overrange inputs. This overflow output can be disabled with the overflow inhibit pin.

The AD9002 is available in two grades, one with 0.5LSB linearity and one with 0.75LSB linearity. Both versions are offered in an industrial grade, −25°C to +85°C, packaged in a 28-pin DIP and a 28-pin JLCC. The military temperature range devices, −55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($-V_S$) . . . . . −6V
Analog-to-Digital Supply Voltage Differential 0.5V
Analog Input Voltage . . . . . $-V_S$ to +0.5V
Digital Input Voltage . . . . . $-V_S$ to 0V
Reference Input Voltage ($+V_{REF} - V_{REF}$)[2] . . −3.5V to 0.1V
Differential Reference Voltage 2.1V
Reference Midpoint Current . . . . . ±4mA
ENCODE to $\overline{\text{ENCODE}}$ Differential Voltage 4V
Digital Output Current 20mA
Operating Temperature Range
AD9002AD/BD/AJ/BJ . . . . . −25°C to +85°C
AD9002SE/SD/TD/TE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

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Electrical Characteristics ($-V_S = -5.2V$; Differential Reference Voltage = 2.0V, unless otherwise stated)

Parameter	Temp	Test Level	AD9002AD/AJ Min	AD9002AD/AJ Typ	AD9002AD/AJ Max	AD9002BD/BJ Min	AD9002BD/BJ Typ	AD9002BD/BJ Max	AD9002SD/SE Min	AD9002SD/SE Typ	AD9002SD/SE Max	AD9002TD/TE Min	AD9002TD/TE Typ	AD9002TD/TE Max	Units
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Linearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Linearity	+25°C	I		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full	VI			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR															
Top of Reference Ladder	+25°C	I		8	14		8	14		8	14		8	14	mV
	Full	VI			17			17			17			17	mV
Bottom of Reference Ladder	+25°C	I		4	10		4	10		4	10		4	10	mV
	Full	VI			12			12			12			12	mV
Offset Drift Coefficient	Full	V		20			20			20			20		µV/°C
ANALOG INPUT															
Input Bias Current[4]	+25°C	I		60	100		60	100		60	100		60	100	µA
	Full	VI			200			200			200			200	µA
Input Resistance	+25°C	III	100	200		100	200		100	200		100	200		kΩ
Input Capacitance	+25°C	III		17	22		17	22		17	22		17	22	pF
Large Signal Bandwidth[5]	+25°C	V		160			160			160			160		MHz
Input Slew Rate[6]	+25°C	V		440			440			440			440		V/µs
REFERENCE INPUT															
Reference Ladder Resistance	+25°C	VI	64	80	110	64	80	110	64	80	110	64	80	110	Ω
Ladder Temperature Coefficient		V		0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	+25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE															
Conversion Rate	+25°C	I	125	150		125	150		125	150		125	150		MSPS
Aperture Delay	+25°C	V		1.3			1.3			1.3			1.3		ns
Aperture Uncertainty (Jitter)	+25°C	V		15			15			15			15		ps
Output Delay (t_{PD})[7,8]	+25°C	I	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	ns
Transient Response[9]	+25°C	V		6			6			6			6		ns
Overvoltage Recovery Time[10]	+25°C	V		6			6			6			6		ns
Output Rise Time[7]	+25°C	I			3.0			3.0			3.0			3.0	ns
Output Fall Time[7]	+25°C	I			2.5			2.5			2.5			2.5	ns
Output Time Skew[7,11]	+25°C	V		0.6			0.6			0.6			0.6		ns
ENCODE INPUT															
Logic "1" Voltage[2]	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage[2]	Full	VI			−1.5			-1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI			150			150			150			150	µA
Logic "0" Current	Full	VI			120			120			120			120	µA
Input Capacitance	+25°C	V		3			3			3			3		pF
Encode Pulse Width (Low)[12]	+25°C	I	1.5			1.5			1.5			1.5			ns
Encode Pulse Width (High)[12]	+25°C	I	1.5			1.5			1.5			1.5			ns
OVERFLOW INHIBIT INPUT															
0V Input Current	Full	VI		144	300		144	300		144	300		144	300	µA
AC LINEARITY[13]															
Effective Bits[14]	+25°C	V		7.6			7.6			7.6			7.6		Bits
In-Band Harmonics															
dc to 1.23MHz	+25°C	I	48	55		48	55		48	55		48	55		dB
dc to 9.3MHz	+25°C	V		50			50			50			50		dB
dc to 19.3MHz	+25°C	V		44			44			44			44		dB
Signal-to-Noise Ratio[15]	+25°C	I	46	47.6		46	47.6		46	47.6		46	47.6		dB
Two Tone Intermod Rejection[16]	+25°C	V		60			60			60			60		dB
DIGITAL OUTPUTS[7]															
Logic "1" Voltage	Full	VI	1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			-1.5			−1.5			−1.5	V
POWER SUPPLY[17]															
Supply Current (−5.2V)	+25°C	I		145	175		145	175		145	175		145	175	mA
	Full	VI			200			200			200			200	mA
Nominal Power Dissipation	+25°C	V		750			750			750			750		mW
Reference Ladder Dissipation	+25°C	V		50			50			50			50		mW
Power Supply Rejection Ratio[18]	+25°C	I		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	mV/V

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
[2]$+V_{REF} \geq -V_{REF}$ under all circumstances.
[3]Maximum junction temperature (t_J max) should not exceed 175°C for ceramic packages, and 150°C for plastic packages:

$t_J = PD(\theta_{JA}) + t_A$
$PD(\theta_{JC}) + t_C$

where
PD = power dissipation
θ_{JA} = thermal impedance from junction to ambient (°C/W)
θ_{JC} = thermal impedance from junction to case (°C/W)
t_A = ambient temperature (°C)
t_C = case temperature (°C)

typical thermal impedances are:
Ceramic DIP $\theta_{JA} = 56°C/W$; $\theta_{JC} = 20°C/W$
Plastic DIP $\theta_{JA} = 60°C/W$; $\theta_{JC} = 20°C/W$
Ceramic LCC $\theta_{JA} = 69°C/W$; $\theta_{JC} = 23°C/W$
PLCC $\theta_{JA} = 60°C/W$, $\theta_{JC} = 19°C/W$.

[4]Measured with AIN = 0V.
[5]Measured by FFT analysis where fundamental is −3dB FS.
[6]Input slew rate derived from rise time (10 to 90%) of full scale input.
[7]Outputs terminated through 100Ω to −2V.
[8]Measured from ENCODE in to data out for LSB only.
[9]For full-scale step input, 8-bit accuracy is attained in specified time.
[10]Recovers to 8-bit accuracy in specified time after 150% full-scale input overvoltage.
[11]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.
[12]ENCODE signal rise/fall times should be less than 10ns for normal operation.
[13]Measured at 125MSPS encode rate.
[14]Analog input frequency = 1.23MHz.
[15]RMS signal to rms noise, with 1.23MHz analog input signal.
[16]Input signals 1V p-p @1.23MHz and 1V p-p @2.30MHz.
[17]Supplies should remain stable within ±5% for normal operation.
[18]Measured at −5.2V ±5%.

Specifications subject to change without notice.

Recommended Operating Conditions

Parameter	Input Voltage		
	Min	Nominal	Max
$-V_S$	−5.46	−5.20	−4.94
$+V_{REF}$	$-V_{REF}$	0.0V	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.
Test Level II – 100% production tested at +25°C, and sample tested at specified temperatures.
Test Level III – Sample tested only.
Test Level IV – Parameter is guaranteed by design and characterization testing.
Test Level V – Parameter is a typical value only.
Test Level VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Linearity	Temperature Range	Package Option[1]
AD9002AD	0.75LSB	−25°C to +85°C	D-28
AD9002BD	0.50LSB	−25°C to +85°C	D-28
AD9002AJ	0.75LSB	−25°C to +85°C	J-28
AD9002BJ	0.50LSB	−25°C to +85°C	J-28
AD9002SD[2]	0.75 LSB	−55°C to +125°C	D-28
AD9002SE[2]	0.75 LSB	−55°C to +125°C	E-28A
AD9002TD[2]	0.50 LSB	−55°C to +125°C	D-28
AD9002TE[2]	0.50 LSB	−55°C to +125°C	E-28A

NOTES
[1]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; J = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]MIL-STD-883 versions.

FUNCTIONAL DESCRIPTION

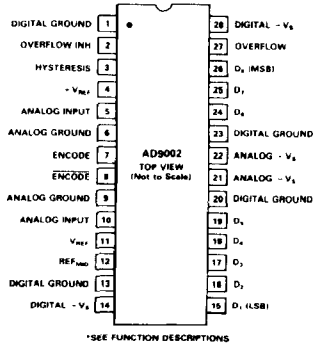
Pin #	Name	Description
1	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
2	OVERFLOW INH	OVERFLOW INHIBIT controls the data output polarity for overvoltage inputs.

ANALOG INPUT	OVERFLOW ENABLED (FLOATING OR −5.2V) OF D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8	OVERFLOW INHIBITED (GND) OF D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
$V_{IN} > +V_{REF}$	1 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1
$V_{IN} \leq +V_{REF}$	0 X X X X X X X X	0 X X X X X X X X

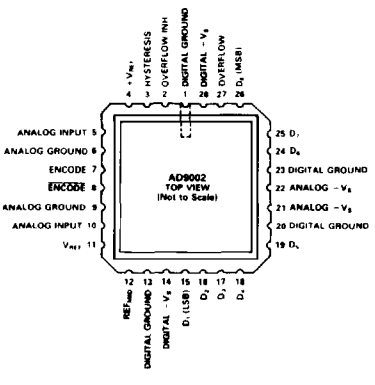
3	HYSTERESIS	The Hysteresis control voltage varies the comparator hysteresis from 0mV to 10mV, for a change from −5.2V to −2.2V at the Hysteresis control pin. Normally connected to −5.2V.
4	$+V_{REF}$	The most positive reference voltage for the internal resistor ladder.
5	ANALOG INPUT	One of two analog input pins. Both analog input pins should be connected together.
6	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
7	ENCODE	Noninverted input of the differential encode input. This pin is driven in conjunction with $\overline{\text{ENCODE}}$. Data is latched on the rising edge of the ENCODE signal.
8	$\overline{\text{ENCODE}}$	Inverted input of the differential encode input. This pin is driven in conjunction with ENCODE.
9	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
10	ANALOG INPUT	One of two analog input pins. Both analog inputs should be connected together.
11	$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
12	REF_{MID}	The midpoint tap on the internal resistor ladder.
13	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
14	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.
15	D1	Digital data output (LSB).
16-19	D2-D5	Digital data output.
20	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
21, 22	ANALOG $-V_S$	One of two negative analog supply pins (nominally −5.2V). Both analog supply pins should be connected together.
23	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
24, 25	D6, D7	Digital data output.
26	D8	Digital data output (MSB).
27	OVERFLOW	Overflow data output. Logic high indicates an input overvoltage ($V_{IN} > +V_{REF}$) if OVERFLOW INHIBIT is enabled (overflow enabled, −5.2V). See OVERFLOW INHIBIT.
28	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.

PIN DESIGNATIONS

DIP



LCC



JLCC