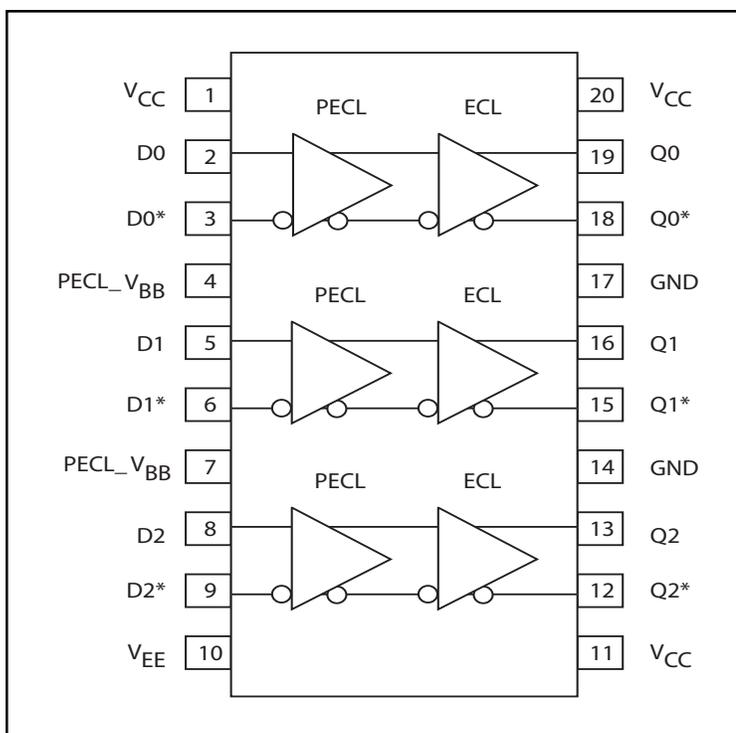


**Description**

The SK100EL91W is a triple PECL to ECL/LVECL and LVPECL to ECL/LVECL translator. It is fully compatible with MC100EL91 and MC100LVEL91. The SK100EL91W provides a  $V_{BB}$  output for single-ended use or DC bias for AC coupling to the device.  $V_{BB}$  is an output pin and should be used as a bias for the EL91W as its current source/sink capability is limited. Whenever used, the  $V_{BB}$  output pin should be bypassed to  $V_{CC}$  via a 0.01  $\mu\text{F}$  capacitor.

To accomplish levels of translation, the EL91W requires three power rails,  $V_{CC}$ ,  $V_{EE}$  and GND. Please refer to the Function Table below for more details.  $V_{CC}$  supply should be connected to the positive supply, and  $V_{EE}$  should be connected to the negative supply.

The GND pins are connected to the system ground plane. Both  $V_{CC}$  and  $V_{EE}$  pins should be bypassed to ground via a 0.01  $\mu\text{F}$  capacitor. Under open input conditions, the  $D^*$  input will be biased at  $V_{CC}/2$ , and the  $D$  input will be pulled to GND. This condition will force the  $Q$  output to low, ensuring stability.

**Functional Block Diagram**

**Features**

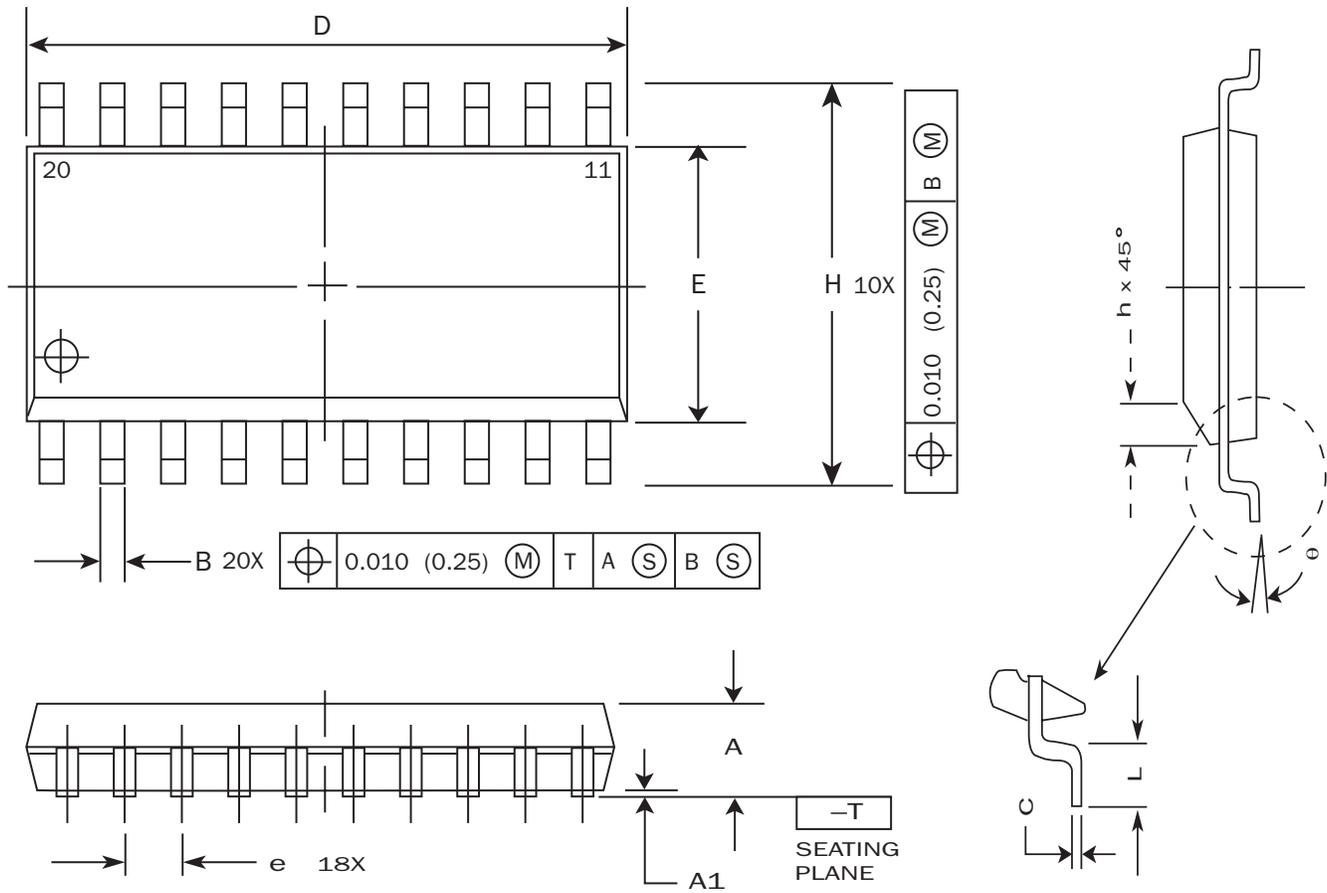
- Extended Supply Voltage Range ( $V_{EE} = -5.5\text{V}$  to  $-3.0\text{V}$  and  $V_{CC} = 3.0\text{V}$  to  $5.5\text{V}$ )
- High Bandwidth Output Transition
- 620 ps Propagation Delay
- $V_{BB}$  Output
- Internal Input Pulldown Resistors
- New Differential Input Common Mode Range
- Fully Compatible with MC100EL91 and MC100LVEL91
- ESD Protection of  $>4000\text{V}$
- Industrial Temperature Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Available in 20 Pin SOIC Package

**Pin Names**

Pin	Function
$D_n, D_n^*$	Differential PECL/LVPECL Inputs
$Q_n, Q_n^*$	Differential ECL/LVECL Outputs
PECL_ $V_{BB}$	PECL/LVPECL Reference Voltage Output

Function	VCC	VEE
LVPECL-to-ECL	3.3V	-5.0V
LVPECL-to-LVECL	3.3V	-3.3V
PECL-to-ECL	+5.0V	-5.0V
PECL-to-LVECL	+5.0V	-3.3V

Function Table

**Package Information**
**20 Pin SOIC Package**


DIM	Millimeters	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
$\theta$	0°	7°

**NOTES:**

1. Dimensions and tolerances per ASME Y14.5M, 1994.
2. Controlling dimension: millimeters.
3. Dimensions D and E do not include mold protrusion.
4. Maximum mold protrusion 0.15 per side.
5. Dimension B does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.13 total in excess of B dimension at maximum material condition.

**DC Characteristics (continued)**
**SK100EL91W PECL/LVPECL Input DC Electrical Characteristics (Notes 1, 5)**

 (V<sub>CC</sub> = 3.0V to 5.5V; V<sub>EE</sub> = -5.5V to -3.0V; V<sub>OUT</sub> loaded 50Ω to GND - 2.0V )

Symbol	Characteristic	TA = - 40 °C		TA = 0 °C		TA = + 25 °C		TA = + 85 °C		Unit	Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
I <sub>IN</sub>	Input Current	-150	150	-150	150	-150	150	-150	150	μA	
V <sub>IH</sub>	Input HIGH Voltage	3835	4120	3835	4120	3835	4120	3835	4120	mV	V <sub>CC</sub> = 5.0V
		2135	2420	2135	2420	2135	2420	2135	2420	mV	V <sub>CC</sub> = 3.3V
V <sub>IL</sub>	Input LOW Voltage	3190	3525	3190	3525	3190	3525	3190	3525	mV	V <sub>CC</sub> = 5.0V
		1490	1825	1490	1825	1490	1825	1490	1825	mV	V <sub>CC</sub> = 3.3V
V <sub>BB</sub>	Reference Output Voltage	3620	3740	3620	3740	3620	3740	3620	3740	mV	V <sub>CC</sub> = 5.0V
		1920	2040	1920	2040	1920	2040	1920	2040	mV	V <sub>CC</sub> = 3.3V
I <sub>CC</sub>	Power Supply Current	3	10	3	10	3	10	3	10	mA	

**SK100EL91W ECL/LVECL Output DC Electrical Characteristics (Note 1)**

 (V<sub>CC</sub> = 3.0V to 5.5V; V<sub>EE</sub> = -5.5V to -3.0V; V<sub>OUT</sub> loaded 50Ω to GND - 2.0V )

Symbol	Characteristic	TA = - 40 °C		TA = 0 °C		TA = + 25 °C		TA = + 85 °C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V <sub>OL</sub>	Output LOW Voltage	-1830	-1555	-1810	-1620	-1810	-1620	-1810	-1620	mV
I <sub>EE</sub>	Power Supply Current	16	36	16	36	16	36	16	36	mA

**AC Characteristics**
**SK100EL91W AC Electrical Characteristics**
 $(V_{CC} = 3.0V \text{ to } 5.5V; V_{EE} = -5.5V \text{ to } -3.0V; V_{OUT} \text{ loaded } 50\Omega \text{ to GND} - 2.0V)$ 

Symbol	Characteristic	TA = - 40 °C		TA = 0 °C		TA = + 25 °C		TA = + 85 °C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>skew</sub>	Output to Output Skew	21	32	21	32	21	32	21	32	ps
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay (Diff) <sup>2</sup>	440	666	460	717	471	742	492	786	ps
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay (SE) <sup>2</sup>	450	713	470	755	480	773	550	808	ps
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Times (20% to 80%)	287	597	287	597	287	597	287	597	ps
V <sub>CMR</sub>	Common Mode Range <sup>4</sup>	GND + 1.2	V <sub>CC</sub>	V						
V <sub>PP</sub>	Minimum Peak-to-Peak Input <sup>3</sup>	150	1000	150	1000	150	1000	150	1000	mV

**Notes:**

- 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
- Duty cycle skew is the difference between T<sub>PLH</sub> and T<sub>PHL</sub> propagation delay through a device.
- Minimum input swing for which parameters are guaranteed.
- CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between V<sub>PP(min)</sub> and 1V. The lower end of the CMR range varies 1:1 with GND and is equal to GND + 1.2V.
- For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
- For ordering description, see TMD Part Ordering Information Data Sheet.

**Ordering Information**

Ordering Code	Package ID
SK100EL91WD	20-SOIC
SK100EL91WDT	20-SOIC
SK100EL91WU	Die

**Application Notes**

- AN1002** - Interfacing Between ECL / LVECL / PECL / LVPECL - to - TTL / LVTTTL / CMOS / LVCMOS
- AN1003** - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices
- AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL
- AN1006** - Designing with 10K and 100K ECL / PECL Devices

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