HM514400A Series — Preliminary

HM514400AL Series Low Power Version

T-46-23-18

HM514400ASL Series Super Low Power Version

1,048,576-Word x 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514400A is a CMOS dynamic RAM organized 1,048,576 word x 4-bit. HM514400A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400A to be packaged in standard 350 mil 20-pin plastic SOJ, standard 300 mil 20-pin plastic SOJ, standard 400 mil 20-pin plastic ZIP, 20-pin plastic TSOP I, 20-pin plastic TSOP I reverse type, 20-pin plastic TSOP II, and 20-pin plastic TSOP II reverse type.

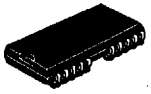
■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....605 mW/550 mW/495 mW/440 mW (max)
  - Standby Mode .....11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles .....(16 ms, 128 ms, 256 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function
- Battery Backup Operation
  - HM514400AL Series (L-Version)
- Data Retention Operation
  - HM514400ASL Series (SL-Version)

■ ORDERING INFORMATION

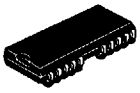
Part No.	Access Time	Package
HM514400AJ/ALJ/ASLJ-6 HM514400AJ/ALJ/ASLJ-7 HM514400AJ/ALJ/ASLJ-8 HM514400AJ/ALJ/ASLJ-10	60 ns 70 ns 80 ns 100 ns	350 mil 20-pin Plastic SOJ (CP-20DA)
HM514400AS/ALS/ASLS-6 HM514400AS/ALS/ASLS-7 HM514400AS/ALS/ASLS-8 HM514400AS/ALS/ASLS-10	60 ns 70 ns 80 ns 100 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM514400AZ/ALZ/ASLZ-6 HM514400AZ/ALZ/ASLZ-7 HM514400AZ/ALZ/ASLZ-8 HM514400AZ/ALZ/ASLZ-10	60 ns 70 ns 80 ns 100 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM514400AT/ALT/ASLT-6 HM514400AT/ALT/ASLT-7 HM514400AT/ALT/ASLT-8 HM514400AT/ALT/ASLT-10	60 ns 70 ns 80 ns 100 ns	20-pin Plastic TSOP I (TFP-20DA)
HM514400AR/ALR/ASLR-6 HM514400AR/ALR/ASLR-7 HM514400AR/ALR/ASLR-8 HM514400AR/ALR/ASLR-10	60 ns 70 ns 80 ns 100 ns	20-pin Plastic TSOP I Reverse Type (TFP-20DAR)
HM514400ATT/ALTT/ASLTT-6 HM514400ATT/ALTT/ASLTT-7 HM514400ATT/ALTT/ASLTT-8 HM514400ATT/ALTT/ASLTT-10	60 ns 70 ns 80 ns 100 ns	20-pin Plastic TSOP II (TTP-20D)
HM514400ARR/ALRR/ASLRR-6 HM514400ARR/ALRR/ASLRR-7 HM514400ARR/ALRR/ASLRR-8 HM514400ARR/ALRR/ASLRR-10	60 ns 70 ns 80 ns 100 ns	20-pin Plastic TSOP II Reverse Type (TTP-20DR)

HM514400AJ/ALJ/ALSJ Series



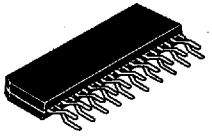
(CP-20DA)

HM514400AS/ALS/ASLS Series



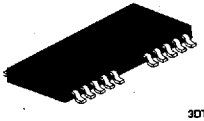
(CP-20D)

HM514400AZ/ALZ/ASLZ Series



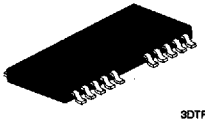
(ZP-20)

HM514400AT/ALT/ASLT Series



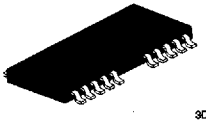
(TFP-20DA)

HM514400AR/ALR/ASLR Series



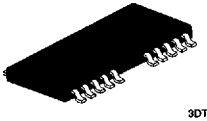
(TFP-20DAR)

HM514400ATT/ALTT/ASLTT Series



(TTP-20D)

HM514400ARR/ALRR/ASLRR Series

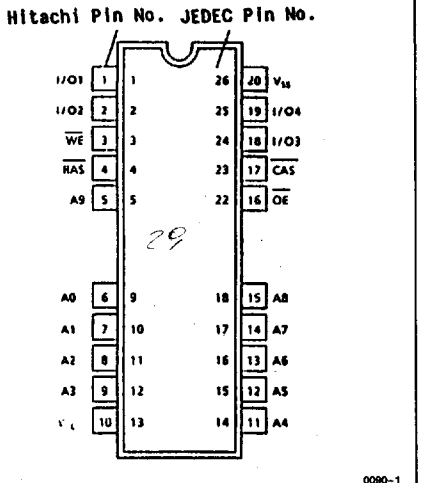


(TTP-20DR)

T-46-23-18

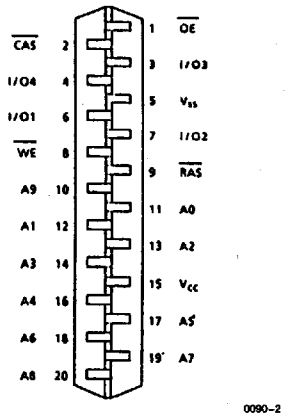
PIN OUT

HM514400AJ/ALJ/ASLJ Series
HM514400CAS/ALS/ASLS Series



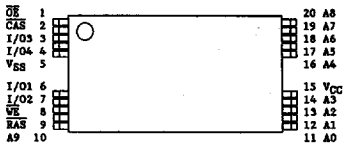
(Top View)

HM514400AZ/ALZ/ASLZ Series



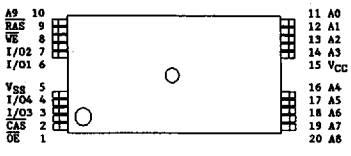
(Bottom View)

HM514400AT/ALT/ASLT Series



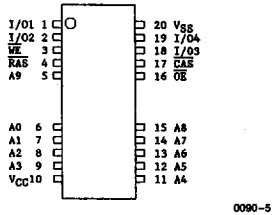
(Top View)

HM514400AR/ALR/ASLR Series



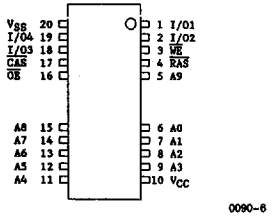
(Top View)

HM514400ATT/ALTT/ASLTT Series



(Top View)

HM514400ARR/ALRR/ASLRR Series



(Top View)

PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
I/O_1–I/O_4	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)
(T_A = 0 to +60°C (SL-Version)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
			4.0	—	5.5	V	1, 2 (SL-Version)
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}.
2. Data retention operation only.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)
(T_A = 0 to +60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version)

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	110	—	100	—	90	—	80	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
[L-Version] Standby Current		—	200	—	200	—	200	—	200	µA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, $\overline{WE}$, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL}, D_{out} = High-Z	4
[SL-Version] Standby Current		—	100	—	100	—	100	—	100	µA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, $\overline{WE}$, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL}, D_{out} = High-Z	4
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	110	—	100	—	90	—	80	mA	t_{RC} = Min	2

T-46-23-18

• **DC Electrical Characteristics** (continued) (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)
(T_A = 0 to +60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version)

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	110	—	100	—	90	—	80	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	110	—	100	—	90	—	80	mA	t_{PC} = Min	1, 3
[L-Version] Battery Backup Operating Current (Standby with CBR Refresh)	I_{CC10}	—	300	—	300	—	300	—	300	µA	t_{RC} = 125 µs, $t_{\overline{RAS}}$ ≤ 1 µs, $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL}, D_{out} = High-Z	4
[SL-Version] Data Retention Current (Equivalent Refresh Time is 256 ms)	I_{CC10}	—	150	—	150	—	150	—	150	µA	t_{RC} = 250 µs, $t_{\overline{RAS}}$ ≤ 200 ns, $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL}, D_{out} = High-Z, 4.0V ≤ V_{CC} ≤ 5.5V	4
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	µA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	µA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V and 0V ≤ V_{IL} ≤ 0.2V.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15, 16]
(T_A = 0 to 60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version))

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	
Refresh Period (L-Version)	t_{REF}	—	128	—	128	—	128	—	128	ms	
Refresh Period (SL-Version)	t_{REF}	—	16	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	3, 4, 13, 17
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 5, 13, 17
Access Time from $\overline{OE}$	t_{OAC}	—	15	—	20	—	20	—	25	ns	3, 17
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	18
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	18
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	20	0	20	0	25	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	20	0	20	0	25	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	20	—	20	—	25	—	ns	

Write Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	150	—	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	65	—	80	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	ns	3, 13, 17
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	55	—	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	80	—	95	—	100	—	110	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

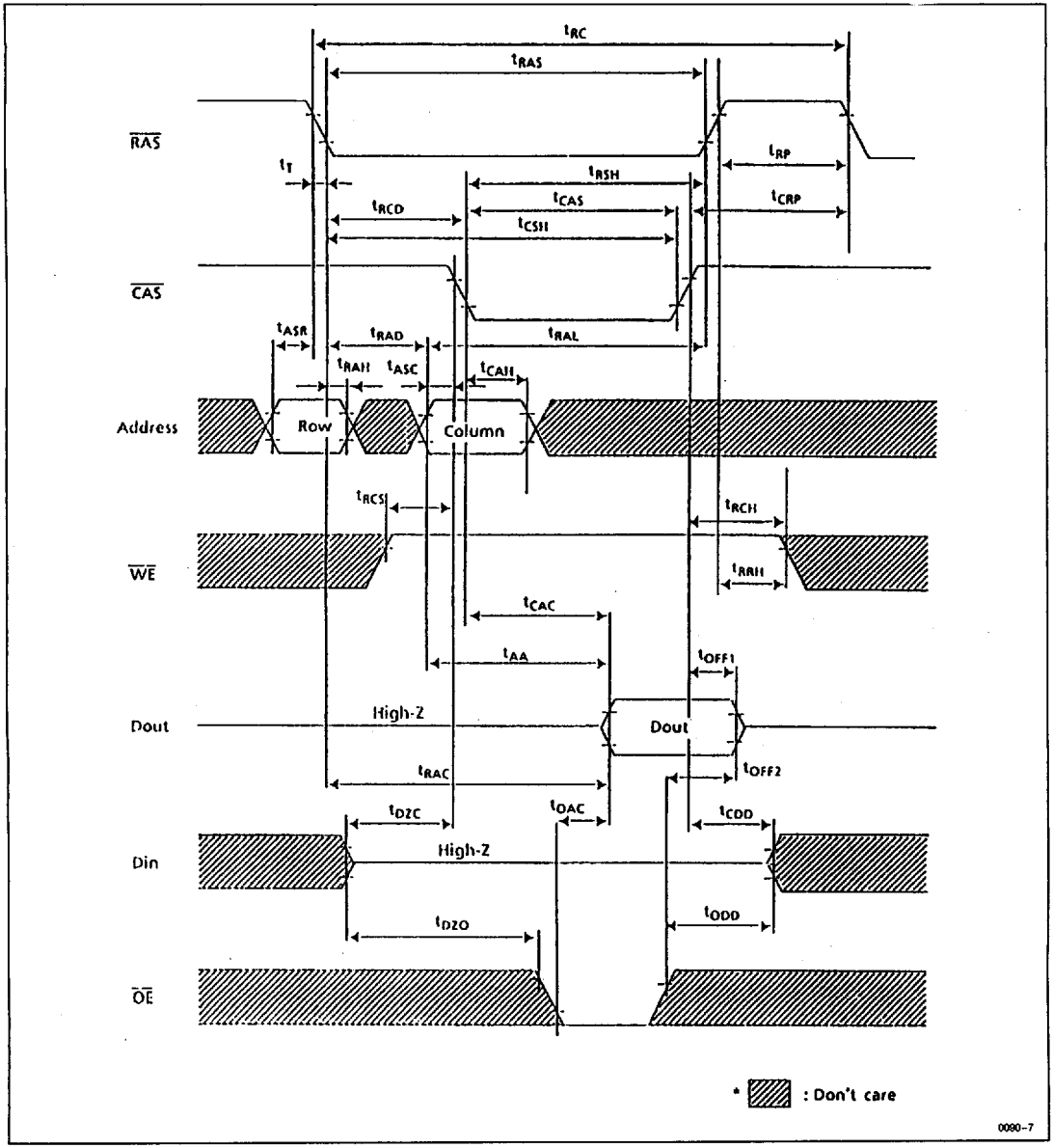
Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	40	—	50	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and t_{RAD} (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits ... CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

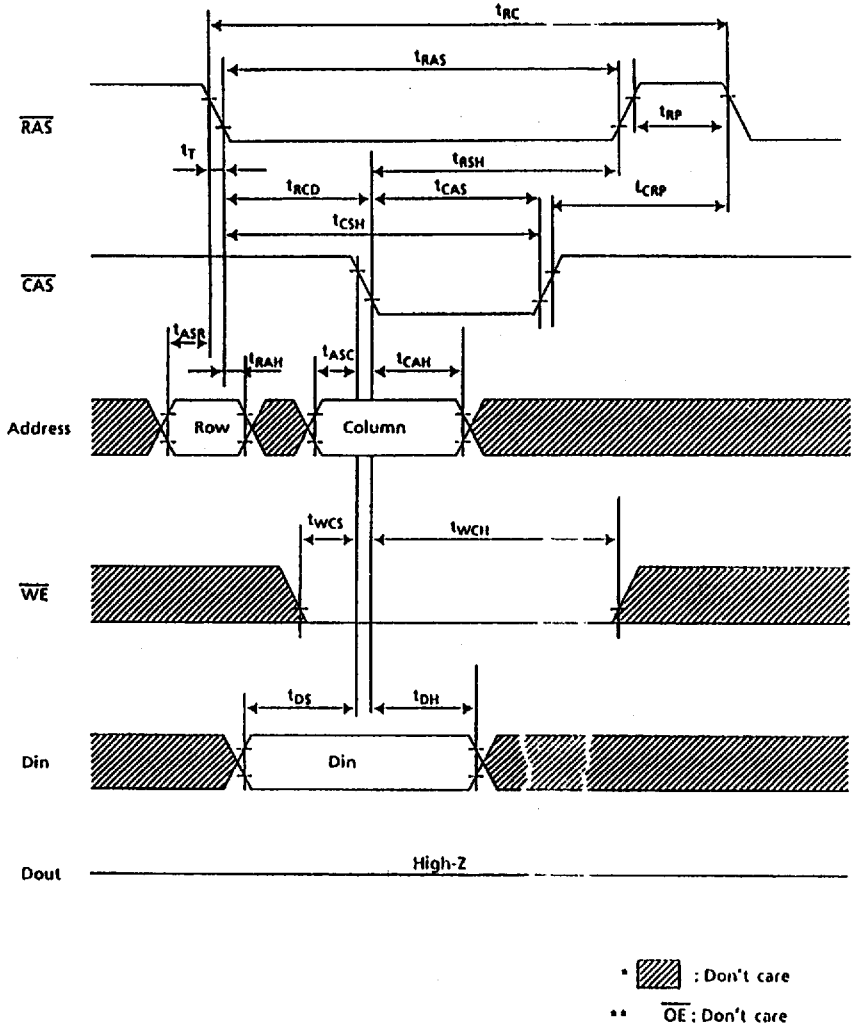
• Read Cycle

T-46-23-18



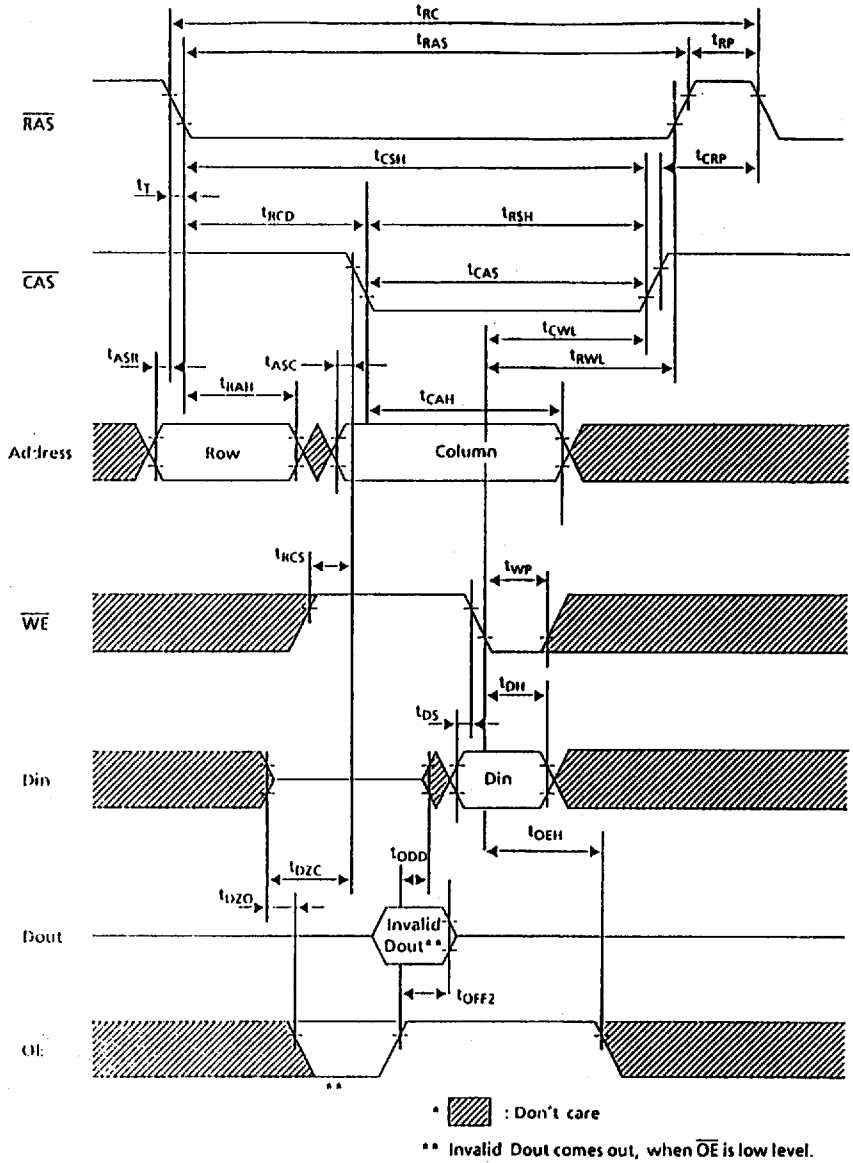
• Early Write Cycle

T-46-23-18



• **Delayed Write Cycle**

T-46-23-18



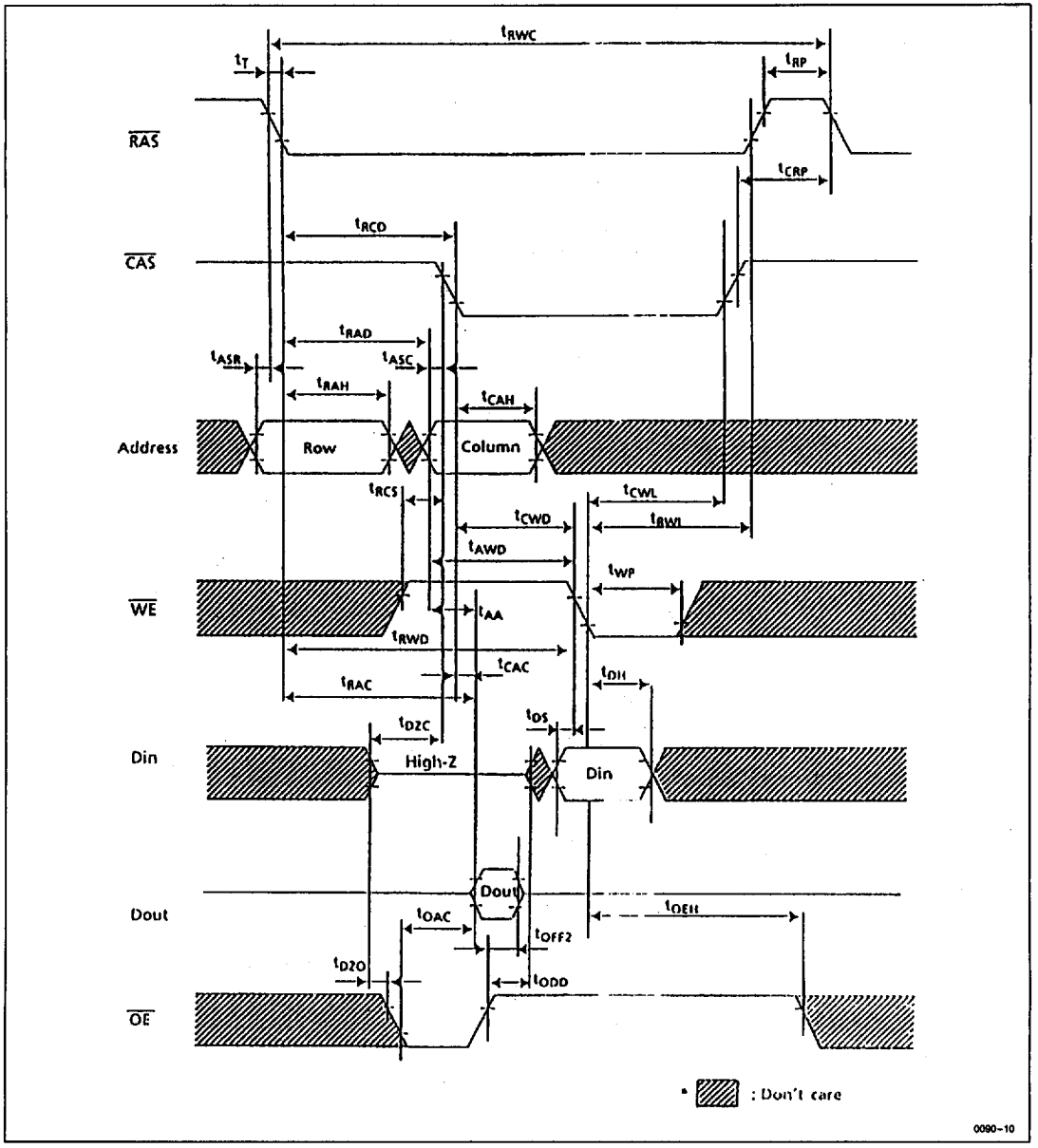
* : Don't care

** Invalid Dout comes out, when $\overline{OE}$ is low level.

0090-9

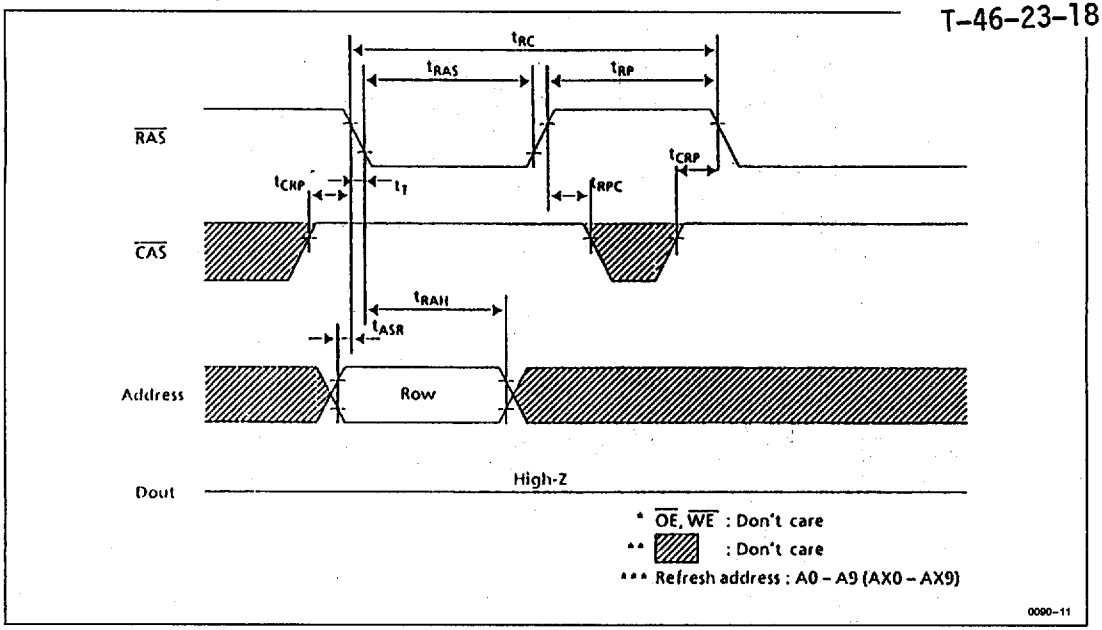
• Read-Modify-Write Cycle

T-46-23-18

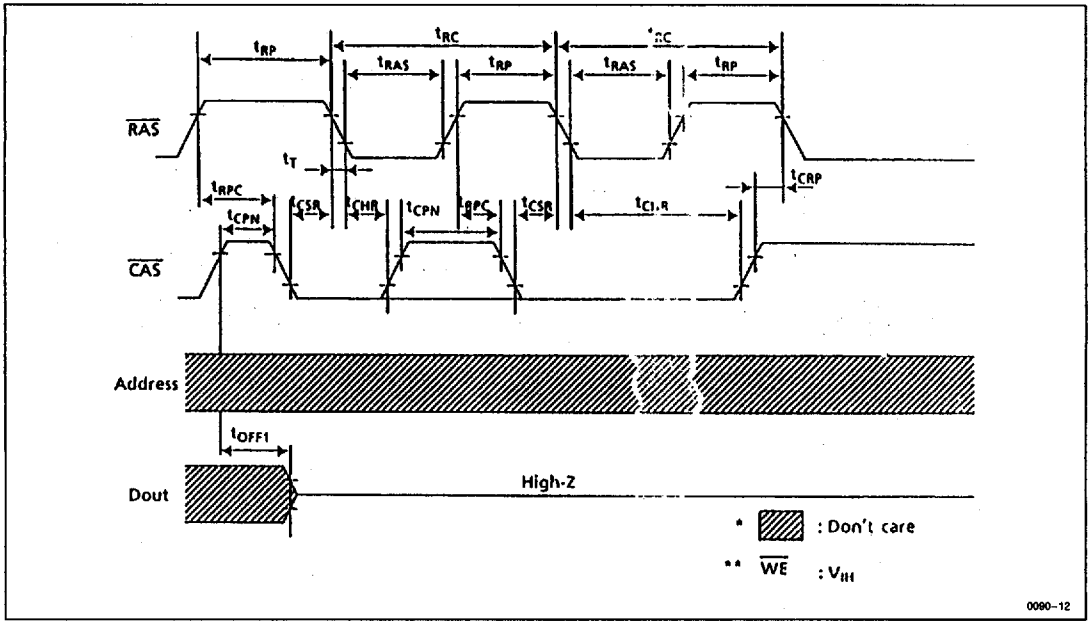


T-46-23-18

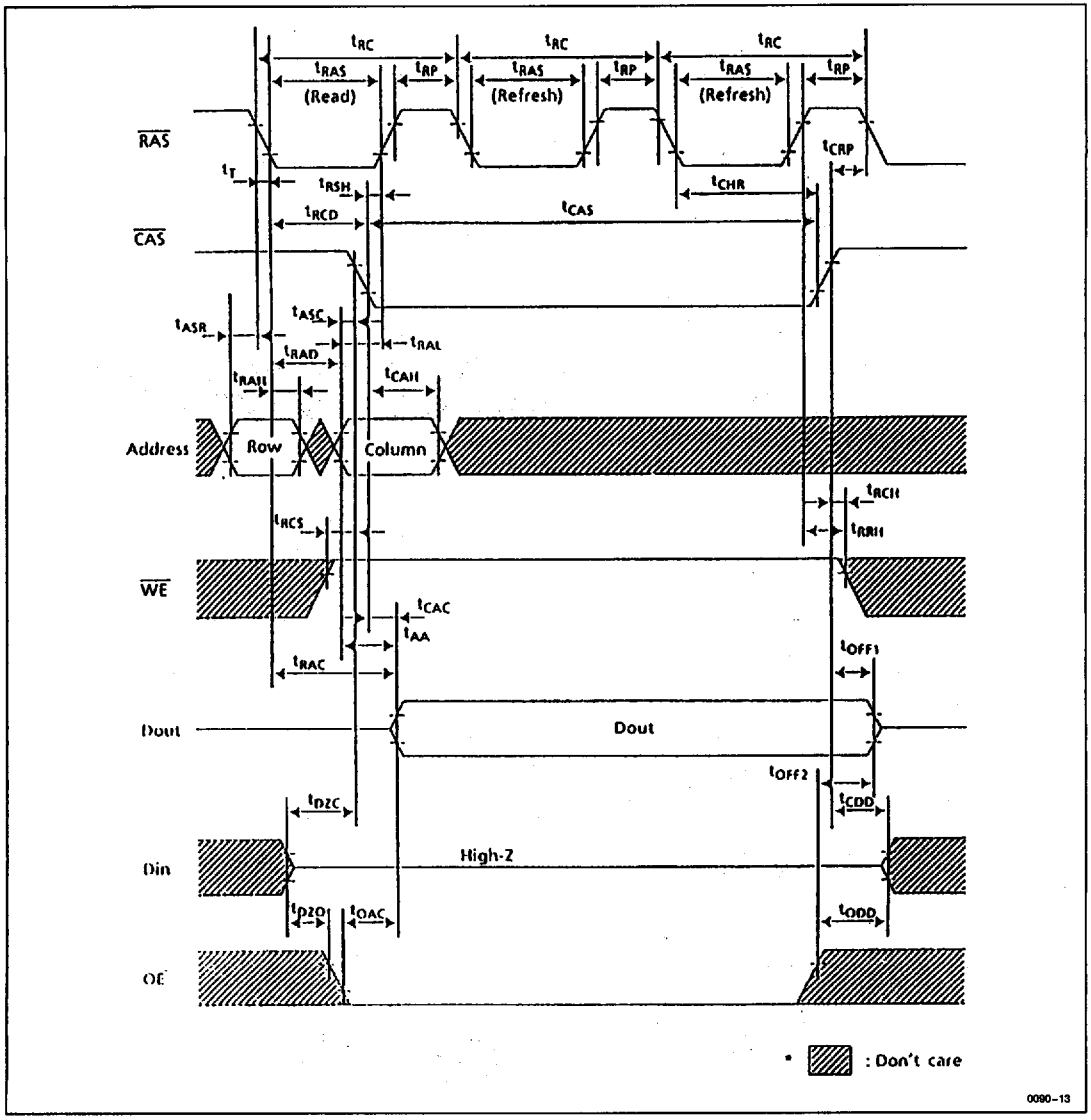
• **$\overline{RAS}$ Only Refresh Cycle**



• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**

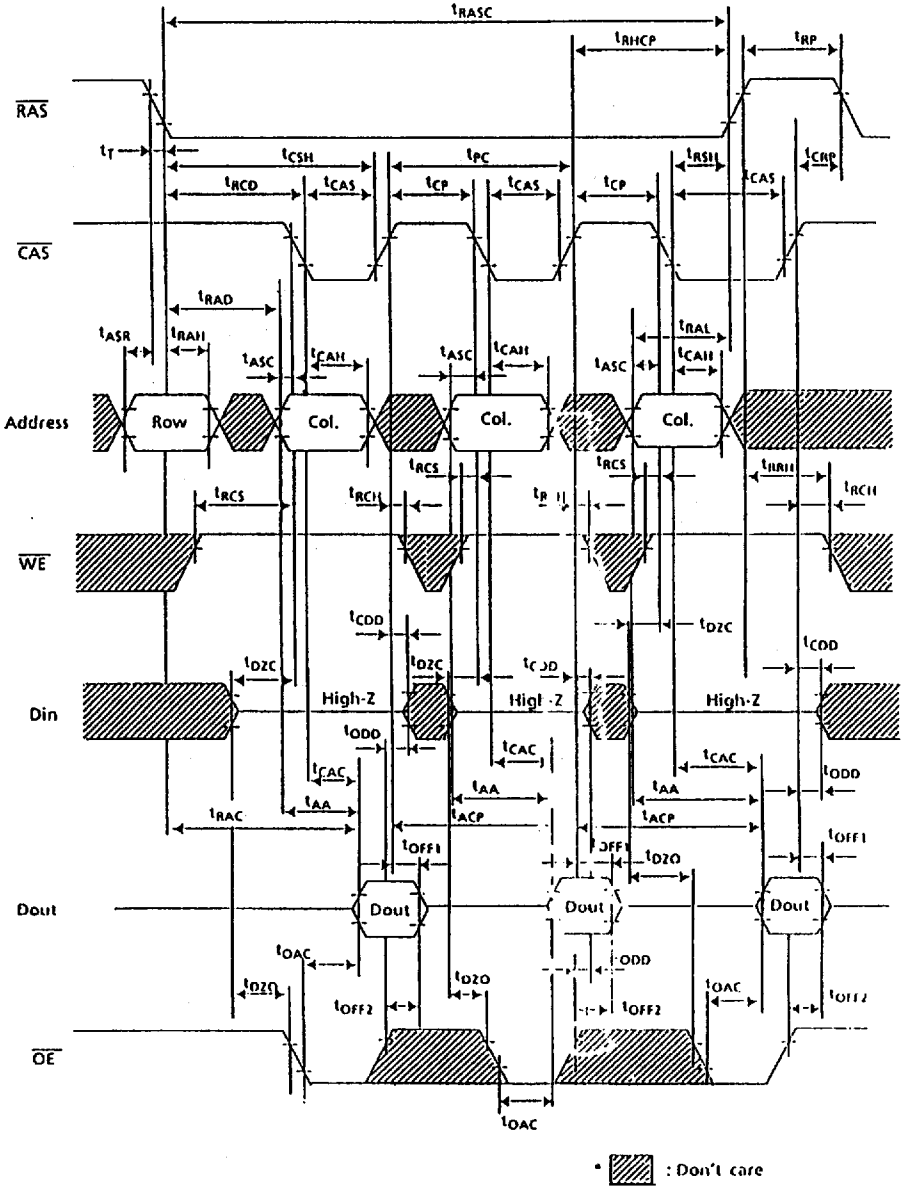


• **Hidden Refresh Cycle**



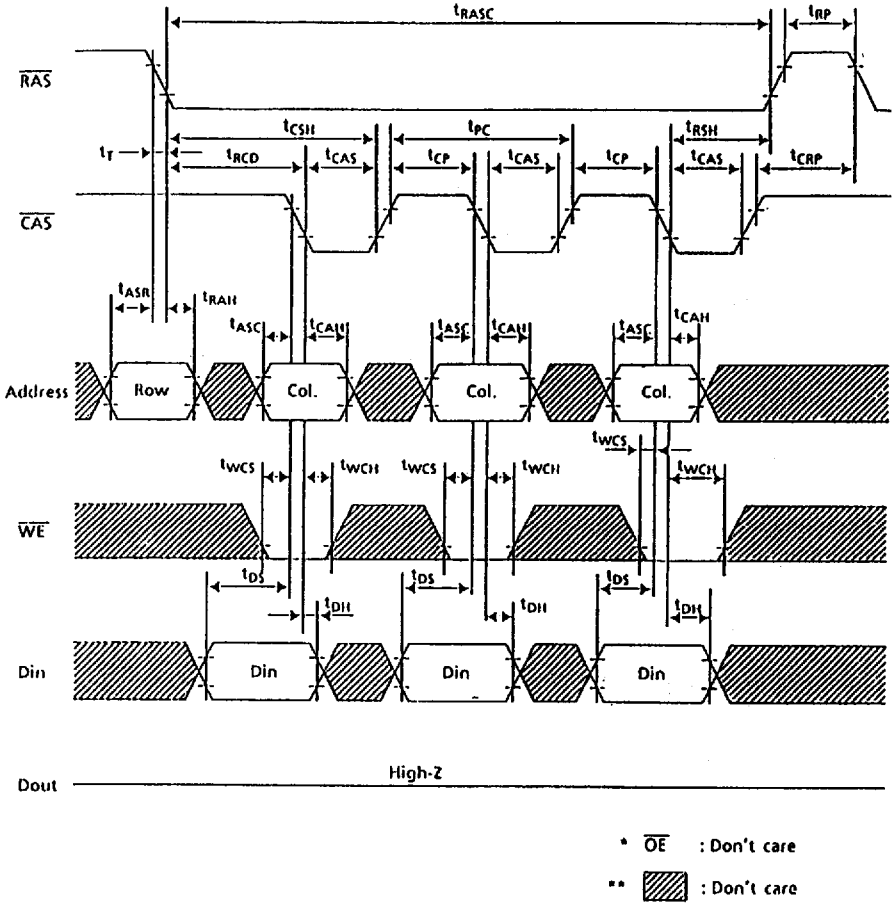
• **Fast Page Mode Read Cycle**

T-46-23-18



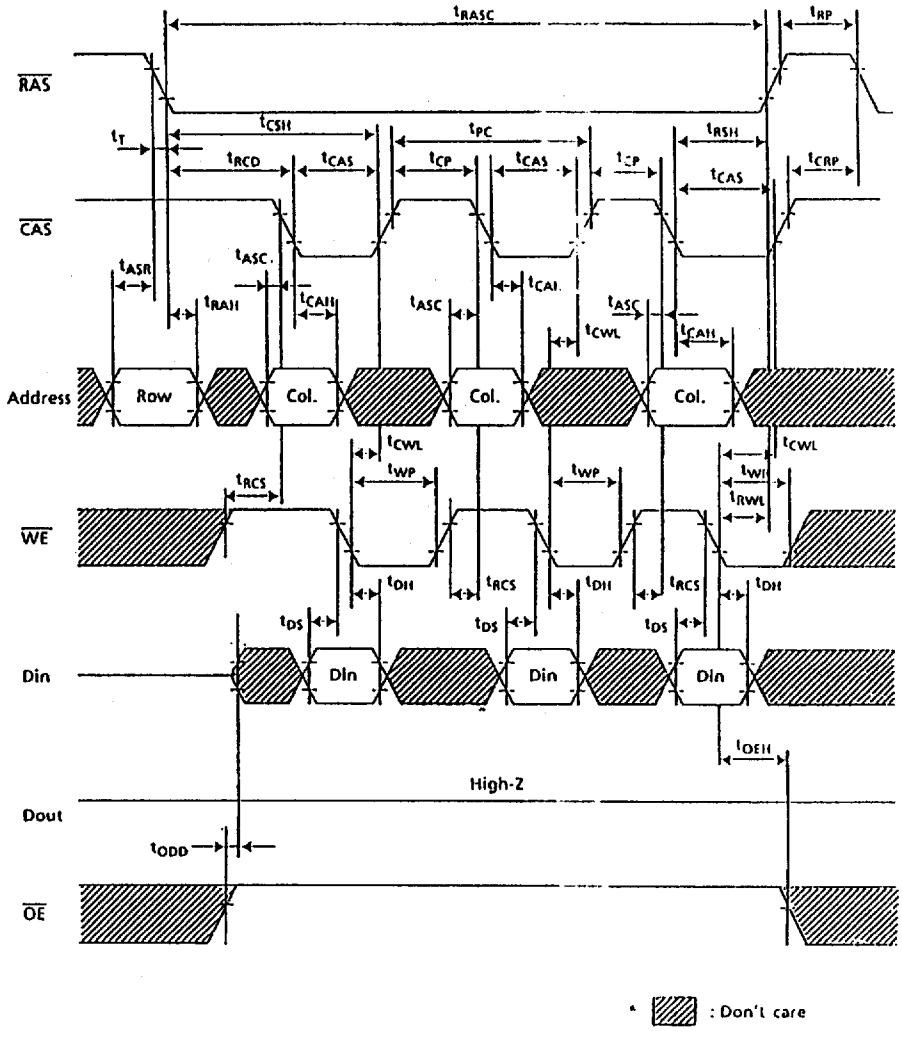
• **Fast Page Mode Early Write Cycle**

T-46-23-18



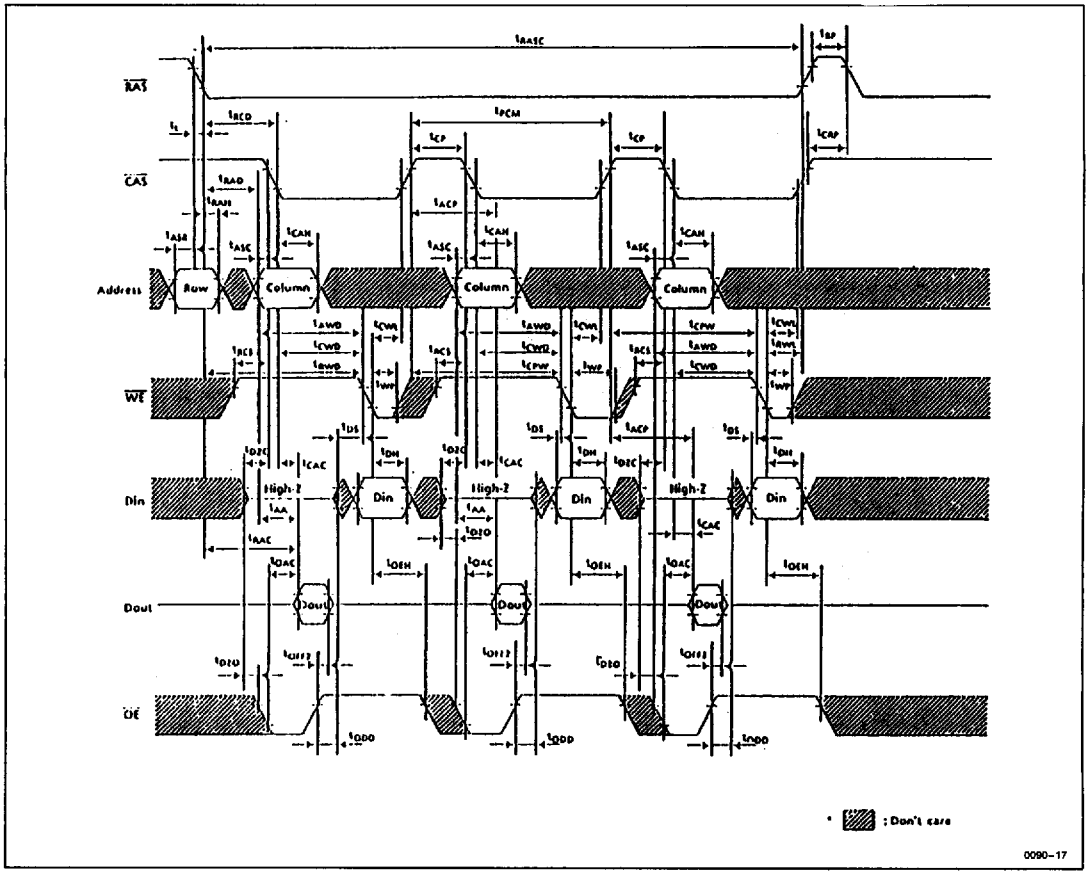
• **Fast Page Mode Delayed Write Cycle**

T-46-23-18



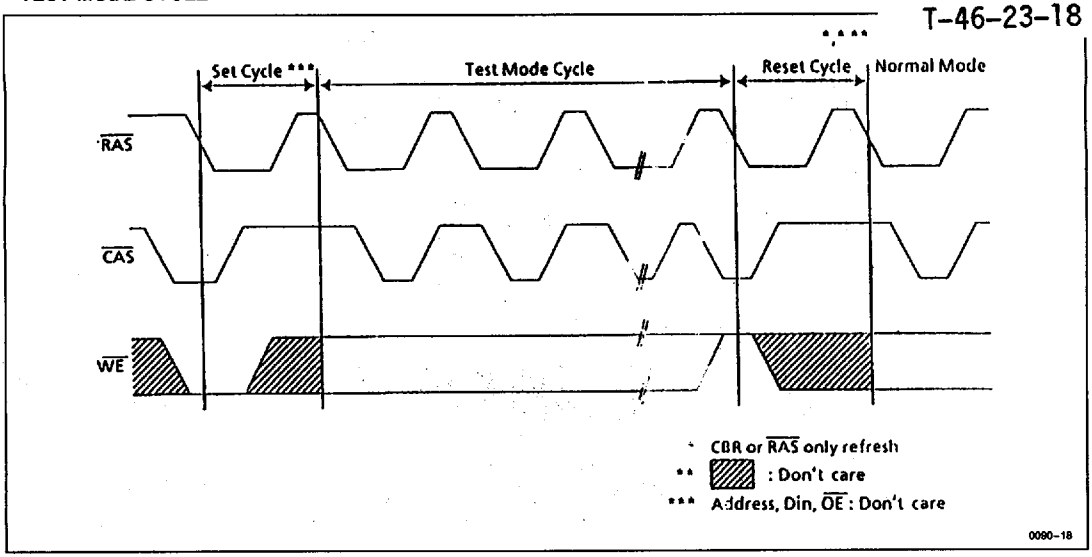
• **Fast Page Mode Read-Modify-Write Cycle**

T-46-23-18

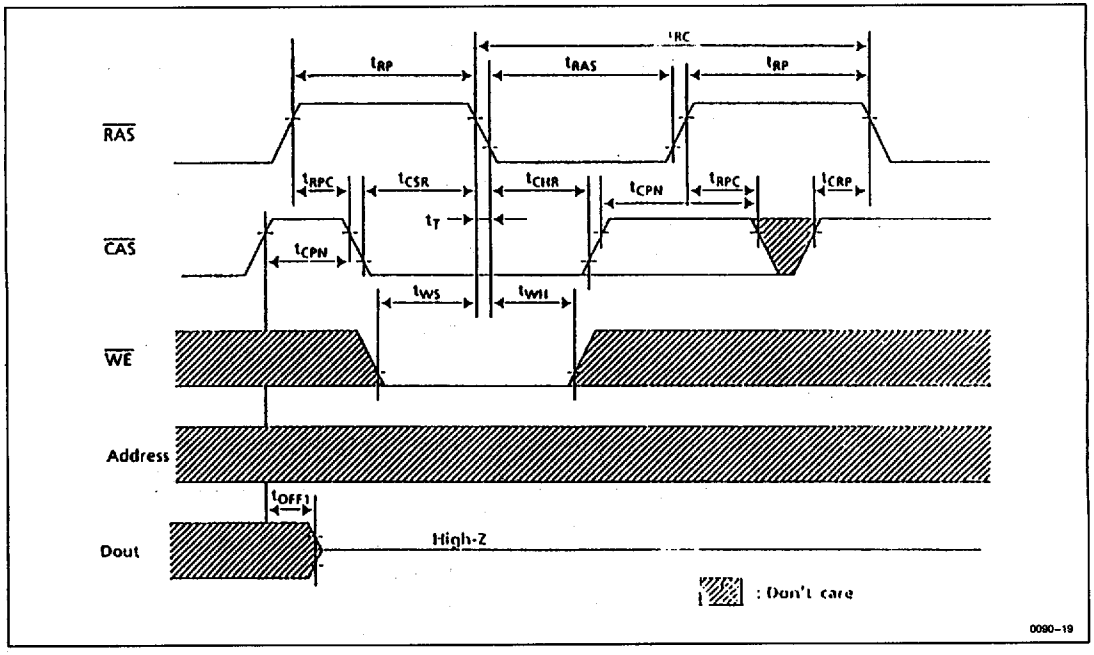


• **TEST MODE CYCLE**

T-46-23-18



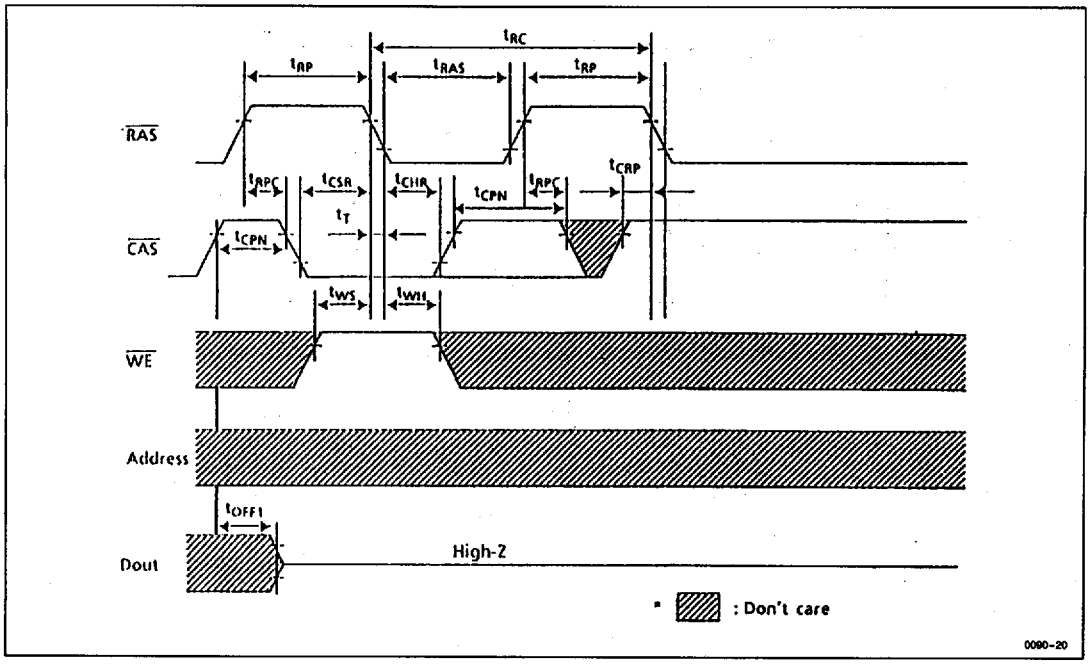
• **Test Mode Set Cycle**
WE And CAS Before RAS Refresh



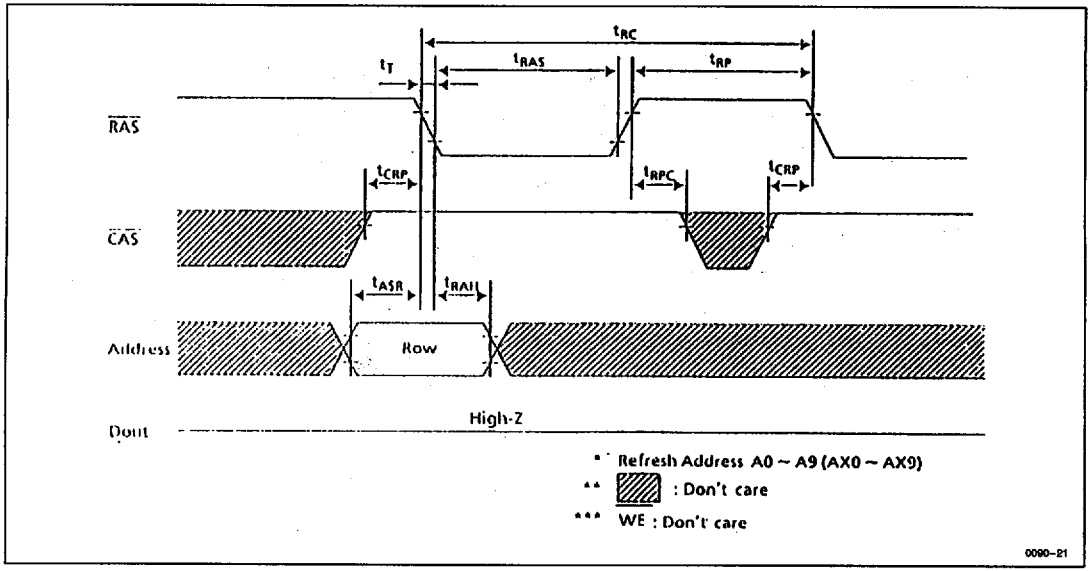
T-46-23-18

- **Test Mode Reset Cycle**

CAS Before RAS Refresh Cycle

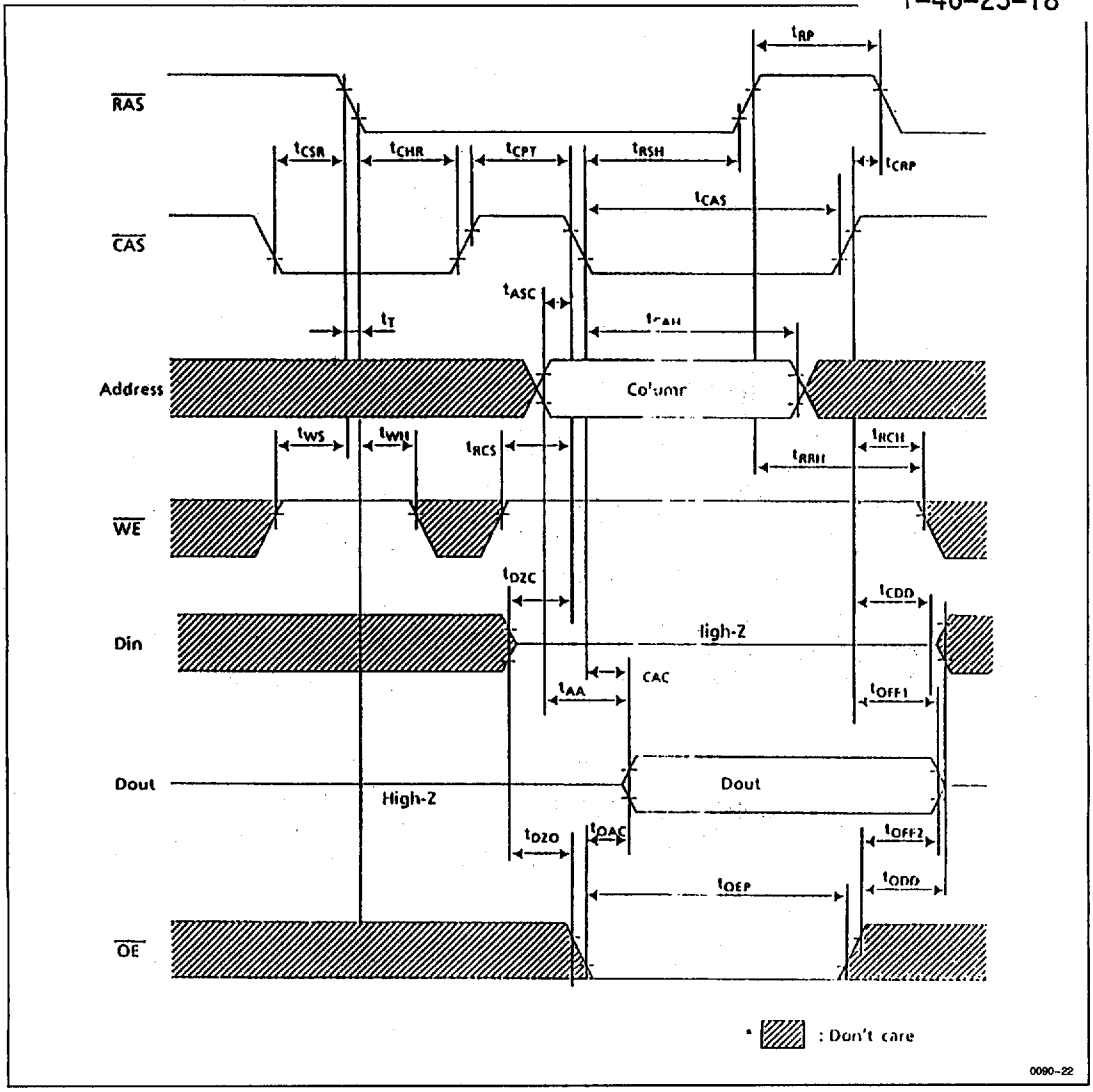


RAS Only Refresh Cycle



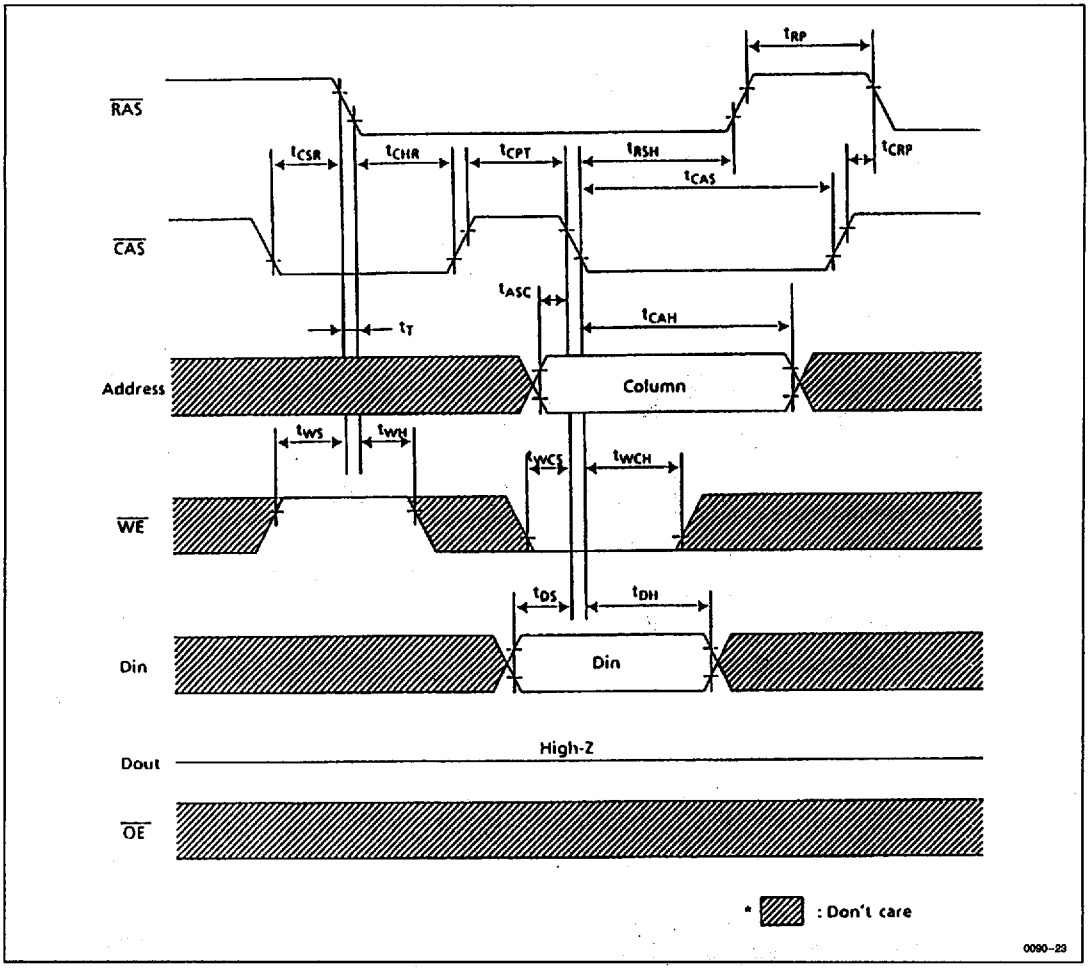
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)

T-46-23-18



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)

T-46-23-18



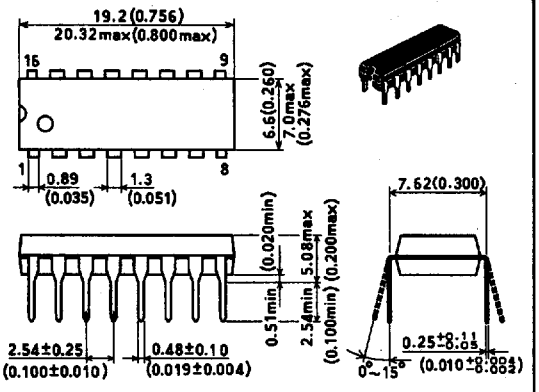
PACKAGE INFORMATION

T-90-20

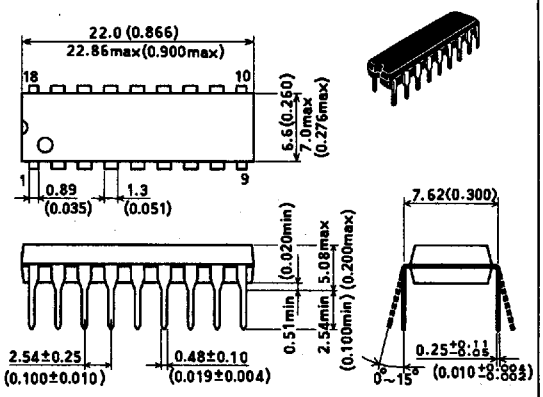
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

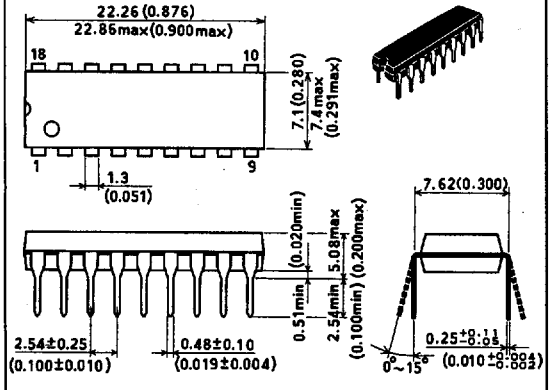
• DP-16B



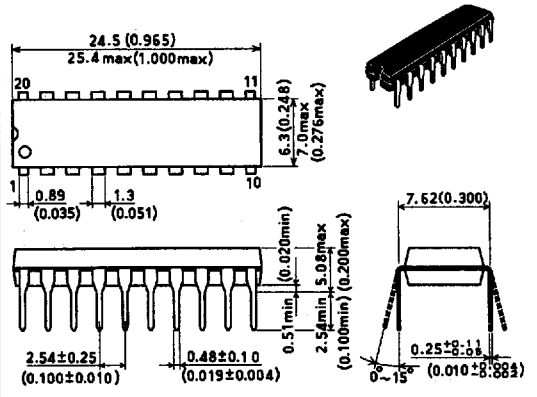
• DP-18B



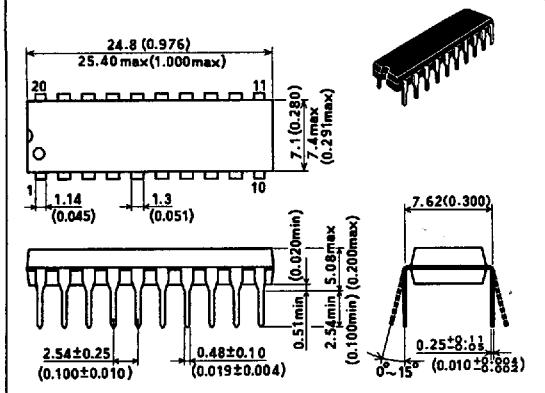
• DP-18C



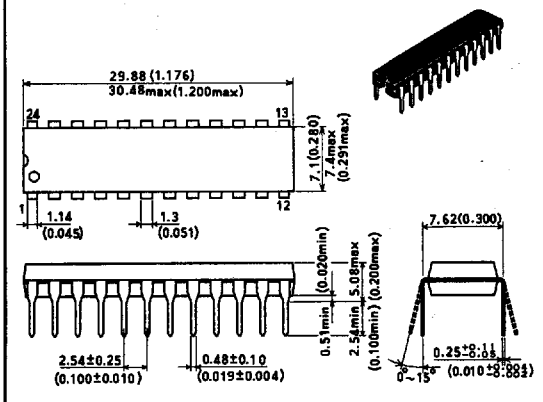
• DP-20N



• DP-20NA



• DP-20NC

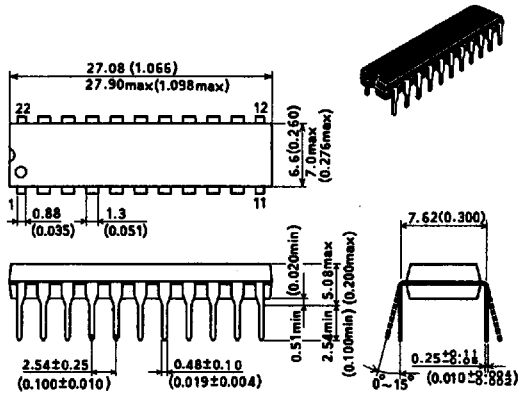


• Dual-in-line Plastic

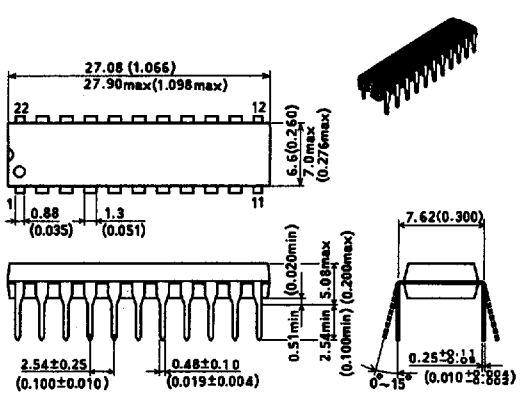
Unit: mm (inch) Scale 3/2

T-90-20

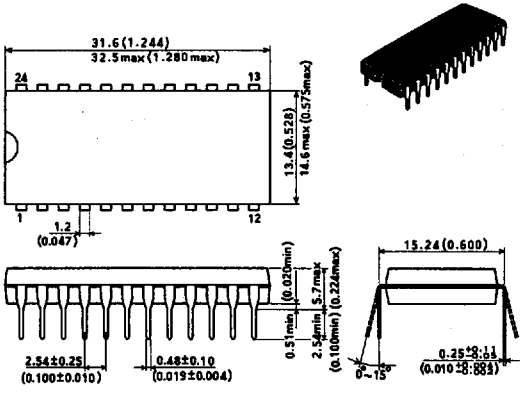
• DP-22N



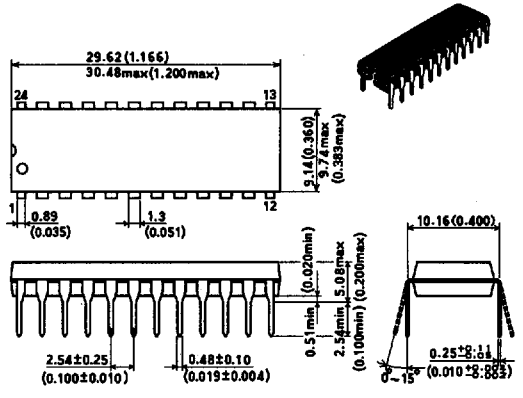
• DP-22NB



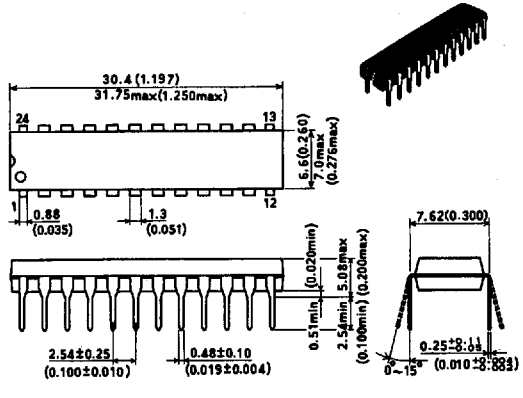
• DP-24



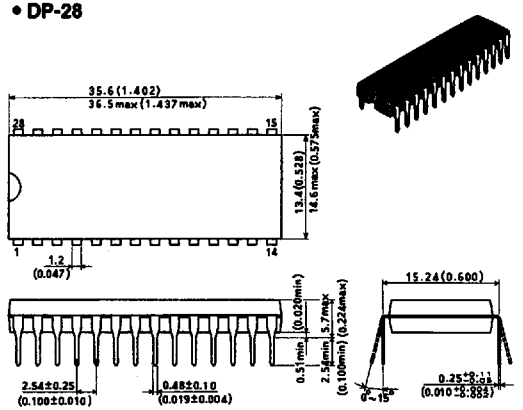
• DP-24A



• DP-24N



• DP-28



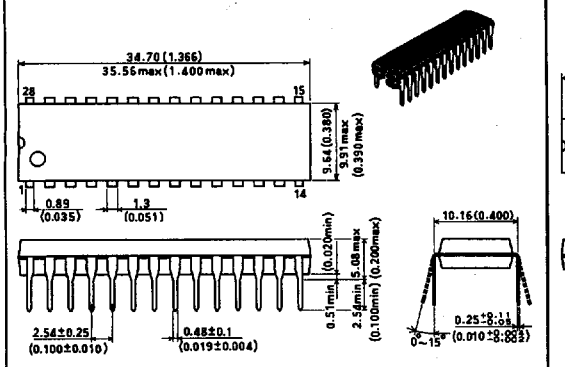
• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

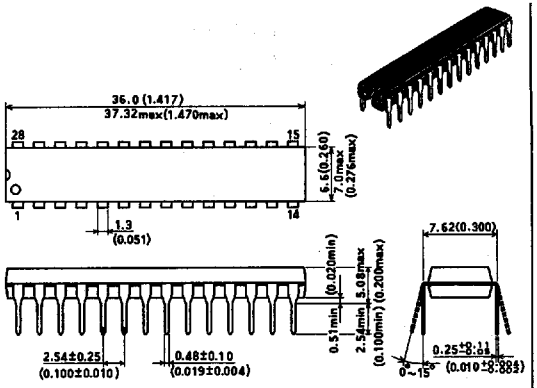
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

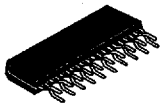


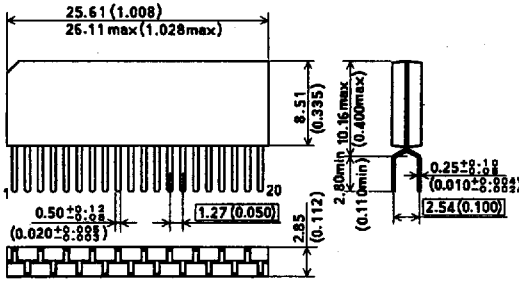
• Zigzag-in-line Plastic HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

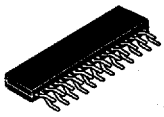
T-90-20

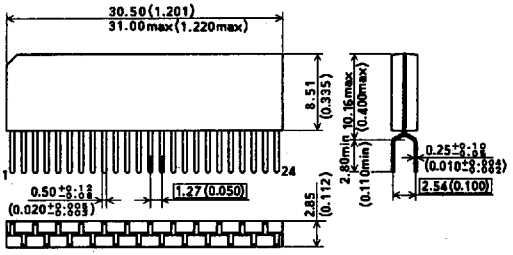
• ZP-20



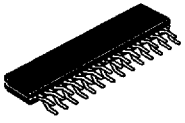


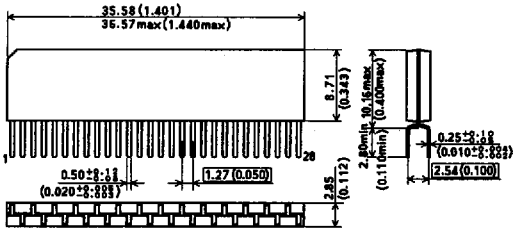
• ZP-24



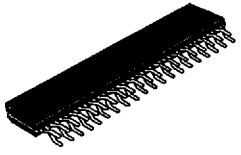


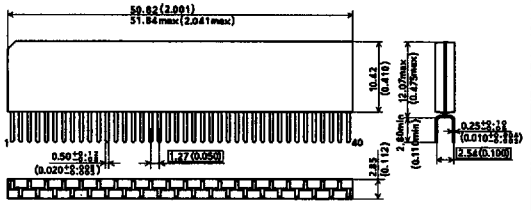
• ZP-28





• ZP-40





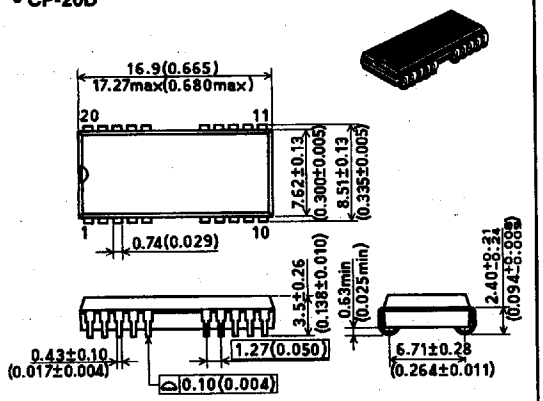
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

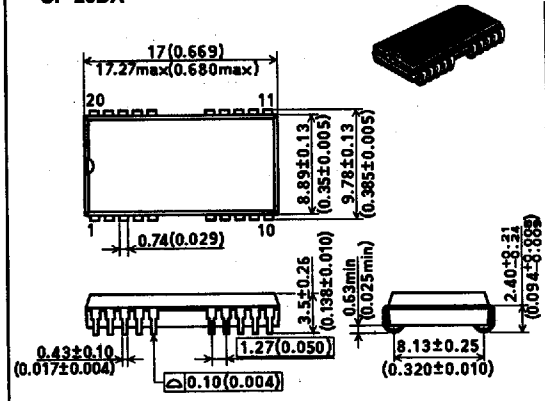
Unit: mm (inch) Scale 3/2

T-90-20

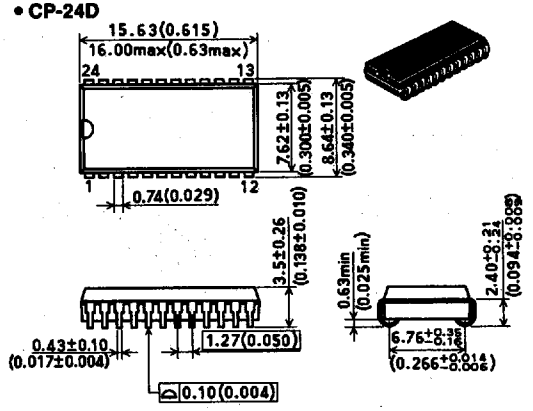
• CP-20D



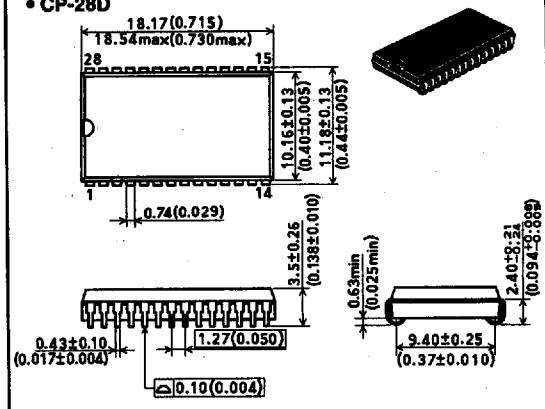
• CP-20DA



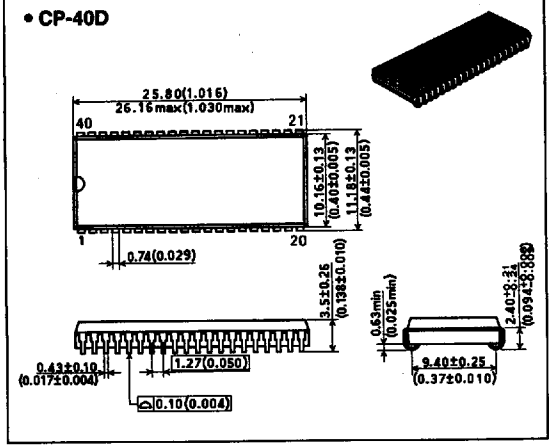
• CP-24D



• CP-28D



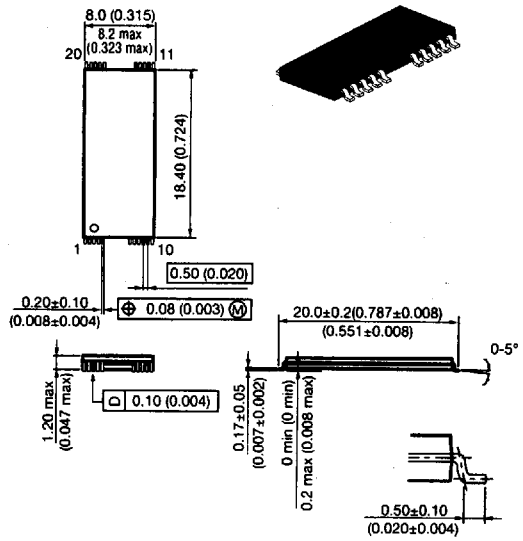
• CP-40D



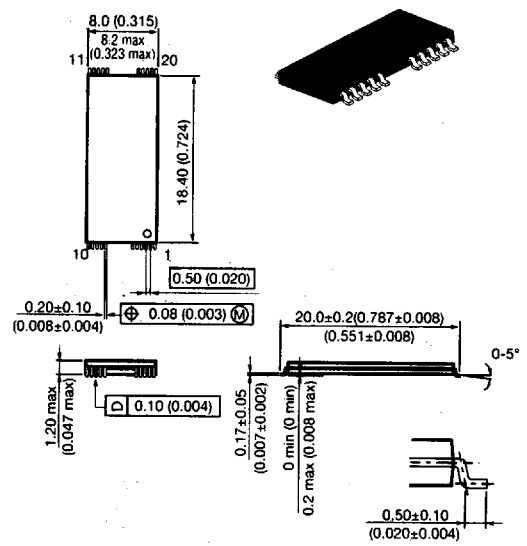
• TSOP (Thin Small Outline Package)

Unit: mm (inch) Scale 3/2

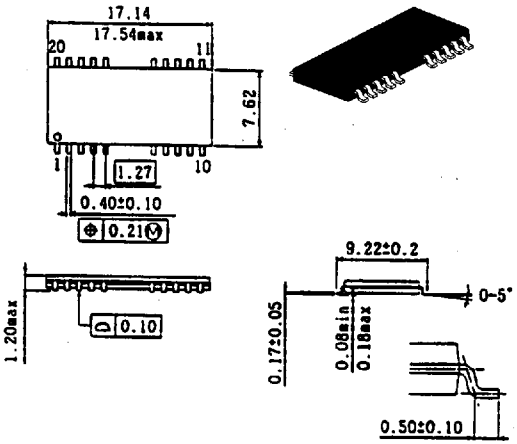
• TFP-20DA



• TFP-20DAR



• TTP-20D



• TTP-20DR