HT82014

ADPCM Synthesizer for External Serial ROM

Features

- Operating voltage: 3.5V~5.0V
- Direct interface with HOLTEK serial ROM
- 12-bit analysis and 3-bit ADPCM coding algorithm
- 16 voice sections/4 key operation
- Auto power control for external power amplifier
- FLAG options:
  - End-pulse output
  - 3Hz flash
  - Busy output
- Programmable voice sampling rate (4K~8K)
- External serial ROM up to 1Mb×8/512Kb×8 in size
- Key debounce time: 33ms
- KEY0 as a stop key
- Key options:
  - Sequential (only for KEY1)
  - Level trigger (only for KEY1)
  - Retriggerable (for KEY2~KEY3)
  - Non-triggerable (for KEY2~KEY3)
  - Level hold (for KEY2~KEY3)
  - One-shot (for KEY2~KEY3)
  - On/off key (for KEY2~KEY3)
  - Play one time and auto stop (for KEY2~KEY3)
  - Non-stop (Repeat) (for KEY1~KEY3)
- 3.58MHz crystal oscillator or RC oscillator for system clock (VDD=5V)
- Voice capacity:
  456 secs—1Mb×8 ROM, 6K sampling rate, 3 bit format

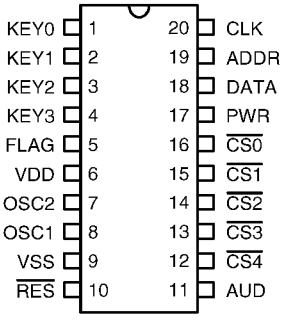
Applications

- Toys
- Alarm clocks
- Public address system
- Alert & warning system
- Sound effect generators
- Products with a voice interface

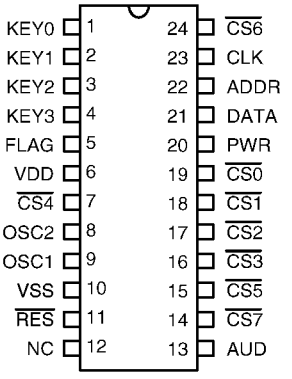
General Description

The HT82014 is a 3-bit ADPCM voice synthesizer LSI implemented in the CMOS technology. It provides an external serial ROM interface circuit and 4 matrix key operation. The size of the voice ROM is decided by the type (512K or 1M) as well as number of the external ROMs (up to 8 at maximum). The customer's voice sources are encoded into a 3-bit format and saved in the external voice ROM by the HOLTEK tools. The instructions of section play-back arrangement for each key are stored in the table ROM. Also the key features are programmable. With such a flexible structure, the HT82014 is excellent for versatile voice applications.

Pin Assignment

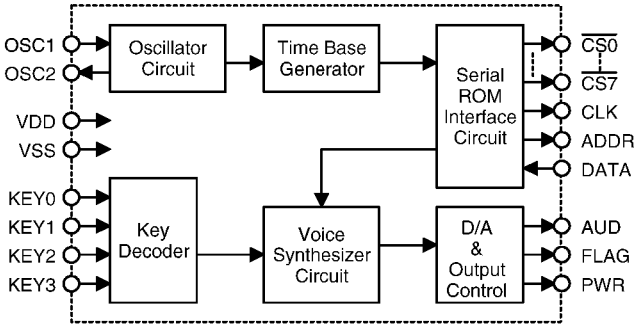


HT82014
– 20 DIP/SOP

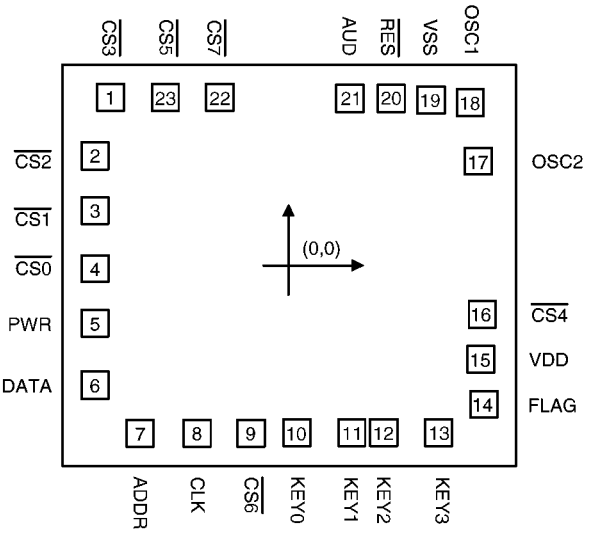


HT82014
– 24 SDIP/SOP

Block Diagram



Pad Coordinates



Chip size: 2620 × 2390 (μm)^2

* The IC substrate should be connected to VSS in the PCB layout artwork.

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1033	974.75	13	870.5	–969.75
2	–1122.5	636.25	14	1132.5	–805.75
3	–1122.5	318.25	15	1117.5	–544.75
4	–1122.5	–18.25	16	1122.5	–283.75
5	–1122.5	–336.25	17	1099.5	605.25
6	–1122.5	–696.25	18	1053.5	946.25
7	–862	–974.75	19	826.5	959.25
8	–531.5	–974.75	20	596.5	969.75
9	–217.5	–974.75	21	356	969.75
10	49.5	–969.75	22	–399.5	974.75
11	367.5	–969.75	23	–715	974.75
12	552.5	–969.75			

Pin Description

24 pin version

Pin No.	Pin Name	I/O	Internal Connection	Descriptions
1~4	KEY0~KEY3	I	Pull-High	Trigger key inputs with a wake-up function
5	FLAG	O	CMOS	End-pulse or 3Hz flash or busy output by code option, active low
6	VDD	—	—	Positive power supply
7	$\overline{CS4}$	O	CMOS	Chip selection for external serial ROMs
8	OSC2	O	—	Oscillator output
9	OSC1	I	—	Oscillator input
10	VSS	—	—	Negative power supply (GND)
11	$\overline{RES}$	I	Pull-High	Input for resetting the chip inside Reset is active at the low-going edge.
12	NC	—	—	No connection
13	AUD	O	PMOS Open Drain	Audio output for an external transistor or amplifier
14	$\overline{CS7}$	O	CMOS	Chip selection for external serial ROMs
15	$\overline{CS5}$	O	CMOS	Chip selection for external serial ROMs
16~19	$\overline{CS3}$~$\overline{CS0}$	O	CMOS	Chip selection for external serial ROMs
20	PWR	O	CMOS	PWR becomes low to make an external amplifier active when the AUD signal is output.
21	DATA	I	CMOS Pull-High	Serial data input from external serial ROMs
22	ADDR	O	CMOS	Serial address output for external serial ROMs
23	CLK	O	CMOS	Serial clock output for external serial ROMs
24	$\overline{CS6}$	O	CMOS	Chip selection for external serial ROMs

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 5.5V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature .....–50°C to 125°C
Operating Temperature .....–25°C to 75°C

Electrical Characteristics

(Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	3.5	—	5	V
I_{DD}	Operating Current	5V	No load, FSYS=3.58MHz	—	1.5	4	mA
I_{STB}	Stand-by Current	5V	No load, Halt mode	—	—	2	μA
V_{IL}	Input Low Voltage	5V	—	0	—	$0.2V_{DD}$	V
V_{IH}	Input High Voltage	5V	—	$0.8V_{DD}$	—	5V	V
I_{OH1}	$\overline{CS0}$~$\overline{CS7}$, CLK, ADDR, FLAG, PWR Source Current	5V	V_{OH1}=4.5V	–1.5	–3	—	mA
I_{OL1}	$\overline{CS0}$~$\overline{CS7}$, CLK, ADDR, FLAG, PWR Sink Current	5V	V_{OL1}=0.5V	4	—	—	mA
I_O	Max. AUD Output Current	5V	V_{OH}=0.6V	–3	–4	—	mA
T_{KEY}	KEY Debounce Time	5V	F_{SYS}=3.58MHz	33	—	—	ms
T_{END}	FLAG End Pulse Width	5V	F_{SYS}=3.58MHz	—	70	—	ms
T_{FLASH}	FLAG Flashing Period	5V	F_{SYS}=3.58MHz	—	333	—	ms
R_{PH}	DATA, $\overline{RES}$, KEY0~KEY3 Pull-High Resistance	5V	V_{IL}=0V	15	—	50	KΩ
F_{SYS}	System Frequency	5V	Crystal or Resonator Oscillator	—	3.58	—	MHz
T_{RES}	Reset Pulse Width	—	V_{DD}=5V	5	—	—	μs

Functional Description

The HT82014 is a 3-bit ADPCM voice synthesizer LSI. It provides 4 keys and an external serial ROM interface. Of the 4 keys (KEY0~KEY3), KEY0 is a stop key, and KEY1 a sequential key. As for the remaining 2 keys (KEY2~KEY3), they are used as direct keys exclusively. The customer's voice data and key definitions are stored in the external serial ROM.

The customer's voice source can be analyzed and coded through the HOLTEK tools. The encoded data are stored in the external HOLTEK serial ROM (HT23CXXX) of 1Mb/512Kb type. The required number of the serial ROMs depends on the customer's voice length, and eight is the maximum number.

Voice Length

Memory Type	Sampling Rate	ADPCM Format	Time
512Kb×8	6K	3-bit	228s
1Mb×8	6K	3-bit	456s

Memory configuration

The HT82014 can interface with HOLTEK's external serial ROMs as the data memory. Following is the memory configuration of the HT82014:

00000H	Memory initial register
00001H : : 00003H	Key option table
00004H : : 00011H	Reserved
00012H : : 00017H	Key starting address
00018H : 0002FH	Reserved
00030H : :	Key group table
: : FFFFFH	Voice ROM

The memory initial register defines the type of serial ROM (1M or 512K), power-on status and FLAG output state. The KEY option table records the various trigger functions of KEY1~KEY3. As for the block of the KEY starting address table, it records the individual address of the 3 keys. The memory allocation of sections included in each group is described in the KEY group table. Finally, the voice ROM stores encoded data. Following is a more detailed description of the memory configuration:

- Memory initial register (00000H)

  The initial register saves the type of the external serial ROM as well as the FLAG output mode. After the power is turned on or the system is reset, the LSI will read-in the register contents to decide the voice ROM type (512K or 1M), LSI power-on status, FLAG output status and voice synthesis sampling rate, as shown below.

Bit	Definition		
D0	Serial ROM type	0	512Kb
		1	1Mb
D1	LSI power on state	0	Enter stand-by
		1	Play KEY1
D2~D3	FLAG output	1X	Flash
		00	End
		01	Busy
D4~D7	Voice sampling rate	See the sampling rate table	

* Serial ROM type

The HT82014 can interface with HOLTEK serial ROM of 512Kb/1Mb (HT23C512/HT23C010) type.

D0=0, 512Kb type

D0=1, 1Mb type

* LSI power on status

The D1 bit defines the LSI power on status. When D1=1, the LSI will play the KEY1 voice once after the power is turned on or the system is reset, and then enters the stand-by state. However, when D1=0, the LSI enters the stand-by state directly after the power is turned on or the system is reset.

* FLAG output

When playing voices, the FLAG pin is active to output one of the following signals through code option:

- Busy output (D2=0, D3=1)

  The FLAG pin is turned low when a sound output occurs. However, FLAG is high when the sound output is terminated.

- End pulse output (D2=0, D3=0)

  The FLAG pin outputs a low pulse when a voice output is completed. The pulse width is 70ms for F_{SYS}=3.58MHz.

- Flash output (D2=1)

  The FLAG pin outputs a flash signal when voices are playing. The FLAG pin is set to high when the voice output is terminated. The flash rate is about 3Hz and the output duty is 50% for F_{SYS}=3.58MHz.

* Voice sampling rate

The sampling rate has to be raised if a better sound quality is required. However, the memory size will be increased with the raise of the sampling rate. Following is a table for the sampling rates to be chosen: (F_{OSC}= 3.58MHz)

D4~D7 --> Define the sampling rate (KHz)

Sampling Rate	D7	D6	D5	D4
4	0	0	0	0
4.5	0	0	0	1
5	0	0	1	0
5.4	0	0	1	1
5.8	0	1	0	0
6	0	1	0	1
6.2	0	1	1	0
6.4	0	1	1	1
6.6	1	0	0	0
6.8	1	0	0	1
7	1	0	1	0
7.2	1	0	1	1
7.4	1	1	0	0
7.6	1	1	0	1
7.8	1	1	1	0
8	1	1	1	1

• Key option table (00001H~00003H)

This table defines the key operating function. Each address of the table registers different functions of a key. For example, the address 00001H defines the KEY1 function, and 00003H defines the KEY3 function. Every address of the option table consists of 8 bits. The bits are defined as follows:

KEY1: Sequential key

D0	Define the key group playing function	0	Level trigger
		1	Repeat
D1~ D7	Reserved		

KEY2 & KEY3: Direct keys

D0	Define the key group playing function	0	One time
		1	Repeat
D1	Define the number of the active keys	0	Normal key
		1	Last key
D2	Define the key to be retriggerable or non-retriggerable	0	Retrigger
		1	Non-retrigger
D3	Define the key's trigger function	0	One shot
		1	Level hold
D4	Define the key on/off function	0	Normal
		1	On/Off key
D5~ D7	Reserved		

* Key group playing function

The D0 bit defines the key group playing function. When D0=1, the corresponding key group is played repeatedly. On the other hand, the according key group is either level triggered (KEY1) or played once (KEY2 and KEY3) and then stops when D0=0.

- Level trigger (D0=0, for KEY1)

  The group after finishing playing will automatically stop if the time to hold KEY1 is less than the group playing time. On the other hand, the group will be played repeatedly when the time to hold KEY1 is greater than the group playing time.

- Repeat function (D0=1)

  In the repeat mode, when one of KEY1~KEY3 is pressed, the corresponding key group is repeatedly played until other triggers occur, and is then changed to the next group. Notice that the sound output is stopped immediately when power is turned off or KEY0 is pressed.

- Play one time function (D0=0)

  In the play-one-time function, when one of KEY2~KEY3 is pressed, the according group is played till it is completely finished. Then, the system enters an idle state. To continue, the corresponding key has to be pressed again, and the according group will come into play, etc.

* The number of the active keys

  The D1 bit defines the number of the active keys. When D1=1 the active key is defined to be the last key. However, the active key is not the last key when D1=0. For example, if the D1 bit of KEY2 (00002H) is "1", it means that KEY1 ~KEY2 are the active keys but KEY3 is not. In addition, the KEY1 sequential cycle begins with KEY1, and stop with the last key.

* Retriggerable/Non-retriggerable definition

  The D2 bit defines the retriggerable or non-retriggerable mode of the key operation.

  - Retriggerable (D2=0)

    A group of KEY2~KEY3 currently playing is stopped immediately when the key corresponding to the playing group is released and a new key trigger is input. The group of the newly triggered key comes into play. However, the newly triggered key is neglected when the original KEY is still held down.

  - Non-retriggerable (D2=1)

    In the non-retriggerable mode,when one of KEY2~KEY3 is pressed, the corresponding group will not start playing till the currently playing group is completed.

* The key trigger function

  The D3 bit defines the key trigger function. KEY2 & KEY3 can be selected as a "one-shot" key or a "level-hold" key.

  - One shot key (D3=0)

    As a "one shot" key, when one of KEY2~KEY3 is pressed, the according group comes into play till it is completed. Then, the system enters an idle state.

  - Level hold key (D3=1)

    As a "level hold" key, when one of KEY2~KEY3 is pressed and held down, the group corresponding to the held key is kept playing till that held key is released.

* The on/off key function

  - Normal (D4=0)

    The key function is decided by the definition of D0, D1, D2 and D3.

  - On/off key (D4=1)

    The according group starts playing when one of KEY2~KEY3 is initially pressed. The playing group will be immediately terminated when the key corresponding to the playing group is re-pressed.

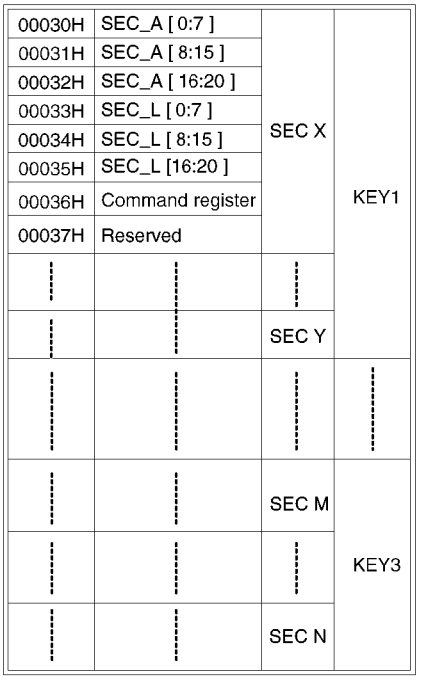
• Key starting address (00012H~00017H)

In the key starting address table, the exact addresses of KEY1~KEY3 are recorded. The recorded address is the starting position of the group table of KEY1~KEY3. Following is a table describing the correspondence between the addresses and KEY1~KEY3.

00012H	KEY1_SA [0:7]	KEY1
00013H	KEY1_SA [8:15]	
00014H	KEY2_SA [0:7]	KEY2
00015H	KEY2_SA [8:15]	
00016H	KEY3_SA [0:7]	KEY3
00017H	KEY3_SA [8:15]	

• KEY group table (00030H~)

The KEY group table records the memory allocation and functions of KEY1~KEY3. For example, the section starting address and section length are defined. In addition, the command register recording the repeating cycle (1 to 16), voice/silence/end sections are registered as well. Following is an illustration of the KEY group table:



SEC_A [0:20] : section starting address
SEC_L [0:20] : section length

* Sections and groups

The total synthesized voice contents can be partitioned into as many number of sections as desired. As for the length of each section, it is decided by the requirements of voice contents.

- Section starting address

The encoded section is saved in the voice ROM. The section starting address is the pointer to the position where the current section is located in the voice ROM.

- Section length

The section length defines the length of the current section included in the voice ROM. The section length can define the end address of the current section. For example:

The starting address: 1000H

The section length: 1F0H

The end address of the 3-bit format in the voice ROM is 1000 + (1F0/8)×3.

- Groups

The HT447L1 plays groups according to the key input. Each group can be made up of one or more sections. When a key is triggered, the corresponding group comes into play. For example, triggering KEY2 plays group 2, and so forth. The same section is allowed to appear in different groups. Each key is comprised by one group only.

* Command register

The command register defines the section repeating number as well as the section type.

D0~D3	Section repeating number
D4~D5	Section type
D6~D7	Reserved

- Section repeating number

The same section can be repeatedly played to save the space of the memory. The repeating cycle can be set as 1 to 16 by D0~D3 bits.

Repeat No.	D0	D1	D2	D3
1	0	0	0	0
2	1	0	0	0
: :	: :	: :	: :	: :
15	0	1	1	1
16	1	1	1	1

– Section type

The bits of D4 and D5 define the section type as a voice section, silence section or end section.

D5	D4	Type
0	0	Voice section
1	0	Silence section
X	1	End section

• Voice ROM algorithm

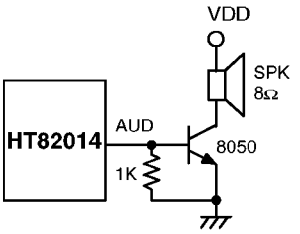
A section when triggered by a key input can be played once, repeated or cascaded with other sections according to the instructions of the key group table. Following is some example of the section division:

group1:	section4+section2
group2:	section1+section3+section5
group3:	section2

Notice that when one of the groups included in the HT82014 is triggered, the section(s) of the triggered group are played in sequence.

AUD

The AUD pin is a PMOS open drain structure. It outputs voice signals to drive the speaker through an external NPN transistor or external power amplifier when the chip is active. However, the AUD pin is floating when the chip is in the stand-by state.

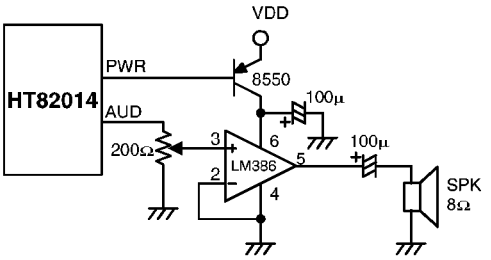


* For transistor

The 8050 type transistor with $h_{FE} \cong 150$ is recommended as an output driver.

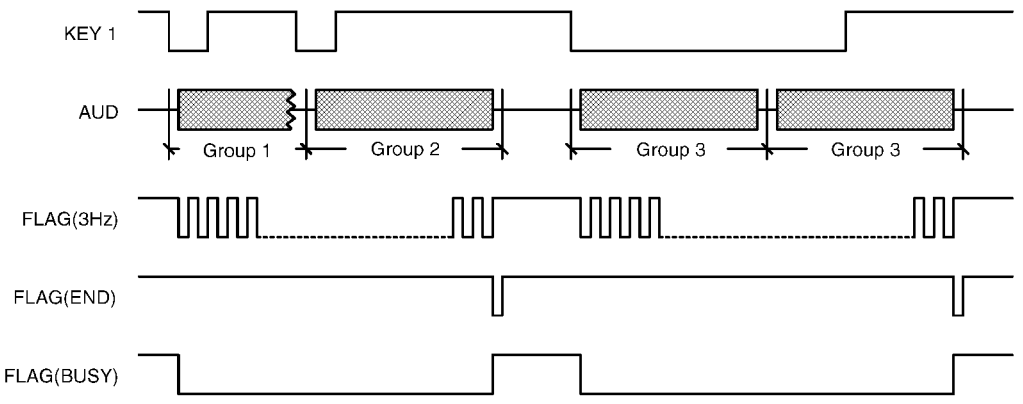
* For power amplifier

For the power amplifier application, the HT82014 provides a PWR pin to control the power consumption in the stand-by state. For better audio frequency response and more power for the speaker output, an external power amplifier is required.

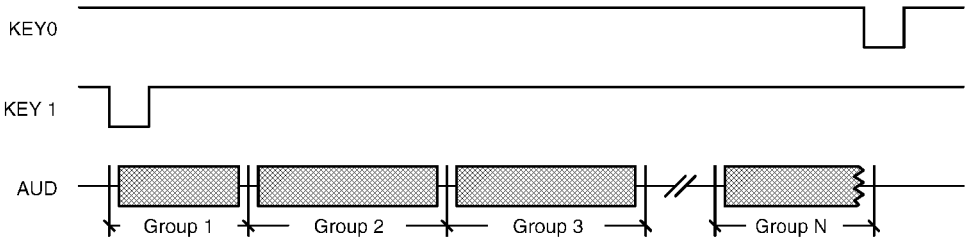


Timing Diagram

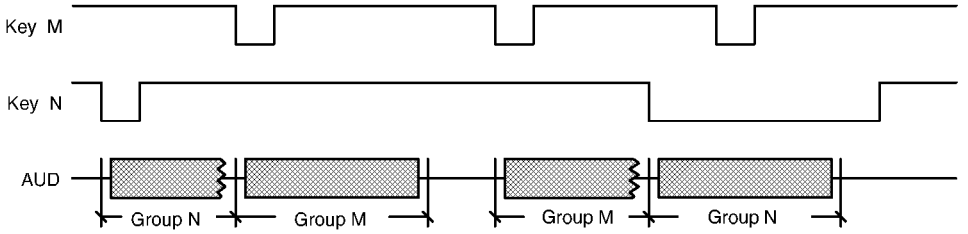
• Sequential & level trigger (KEY1)



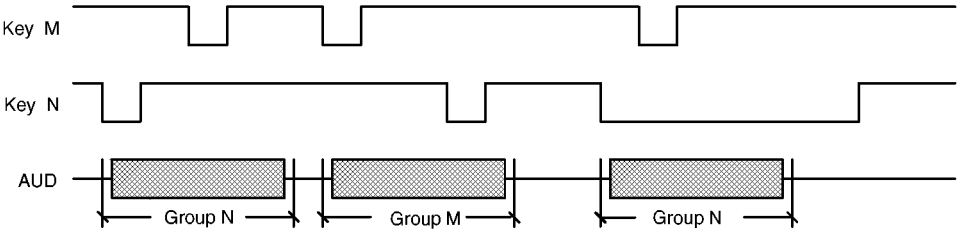
• Sequential & repeat (KEY1)



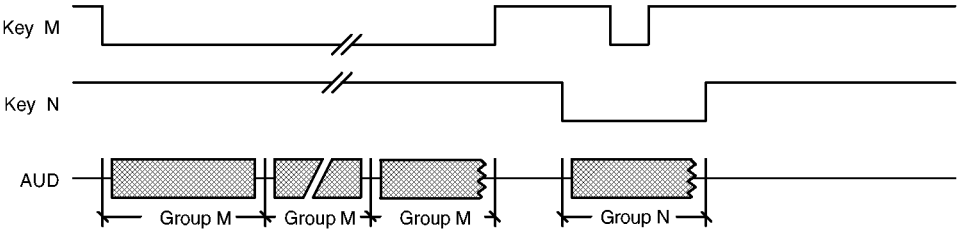
• One shot & retriggerable (KEY2~KEY3)



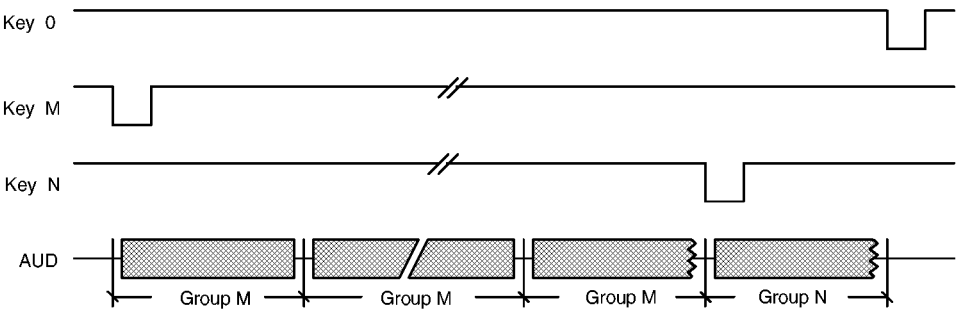
• One shot & non-retriggerable (KEY2~KEY3)



• Level hold (KEY2~KEY3)

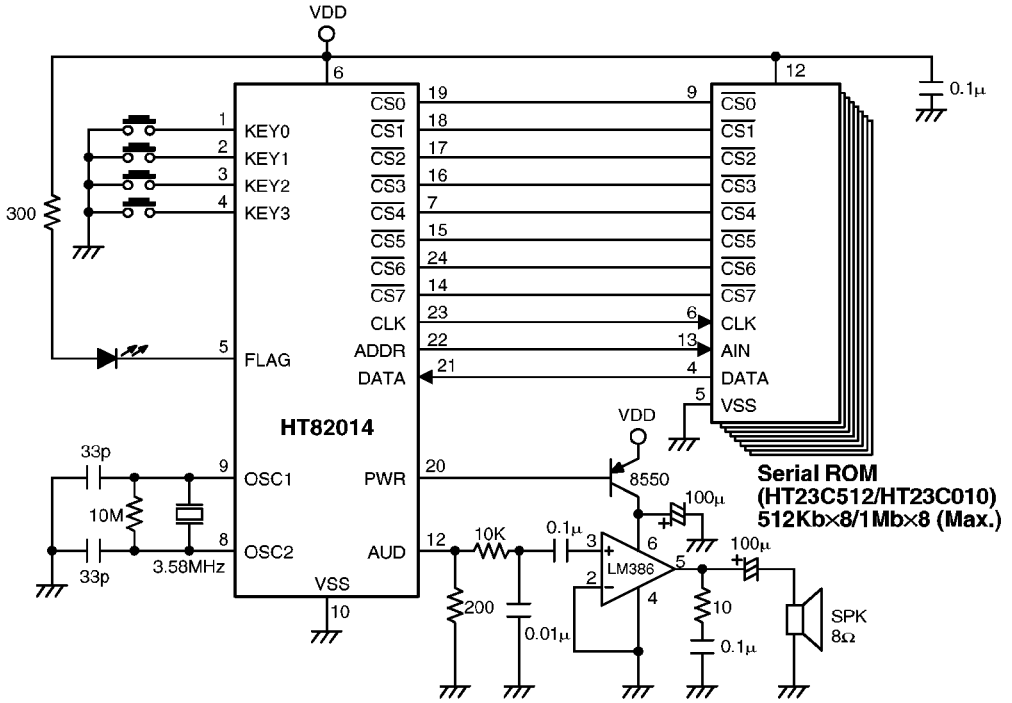


• Repeat & retriggerable (KEY2~KEY3)

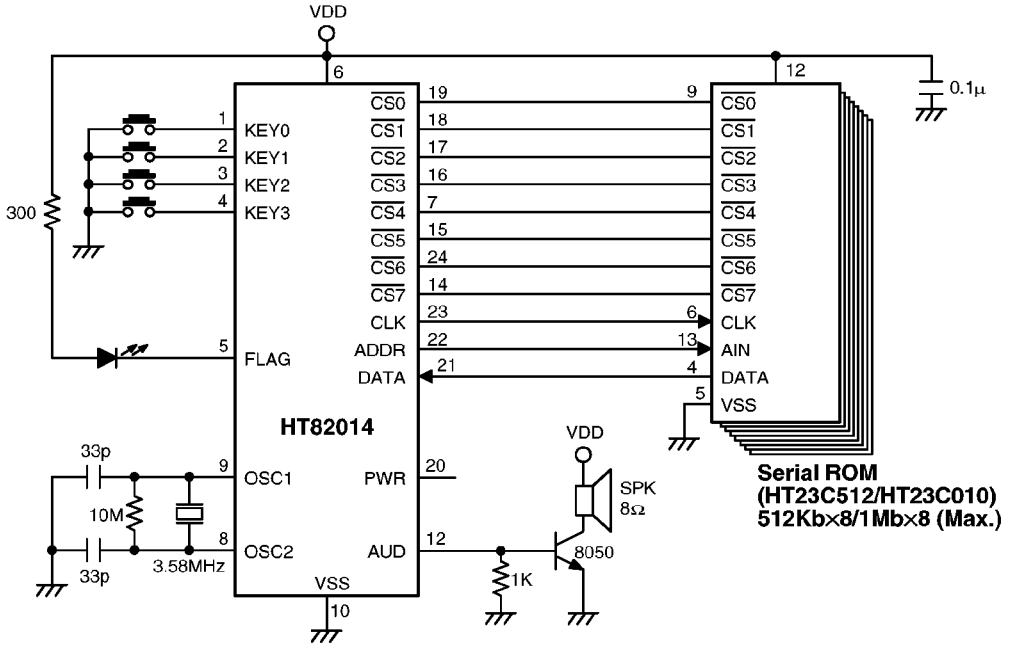


Application Circuit

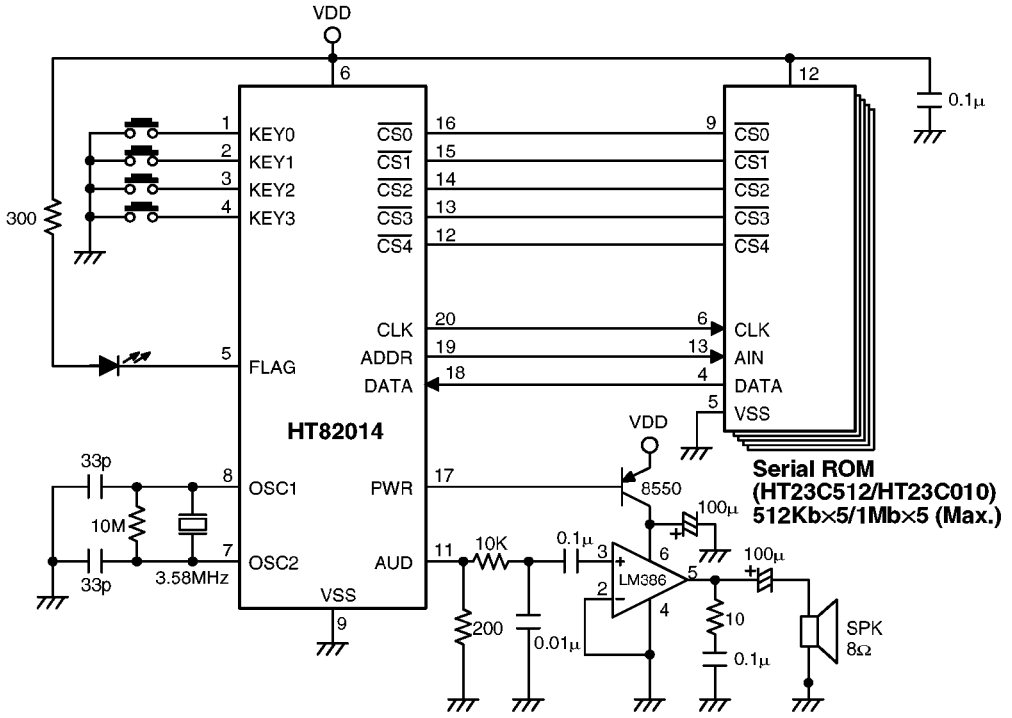
Application with LM386 AMP (24 Pin)



Application with transistor (24 Pin)



Application with LM386 AMP (20 Pin)



Application with transistor (20 pin)