Micro Linear

ML4506

5V Disk Voice Coil Servo Driver

GENERAL DESCRIPTION

The ML4506 is a voice coil power driver intended for use in 5V Hard Disk servo systems. The ML4506 contains all power and control circuitry necessary to drive the voice coils of most small form factor drives. In addition, power fail detection and head retraction functions are provided for orderly shut-down of the drive.

The transconductance is programmed by a logic input at 1/4 A/V and 1/24 A/V respectively, using a 1Ω sense resistor. This allows for greater DAC resolution in digitally controlled servos during track follow without compromising dynamic range during seek.

The retraction circuit, main drive circuit, and control circuits are each powered from their own supplies. This allows maximum flexibility and provides for the lowest forward drop by eliminating the need for a blocking diode.

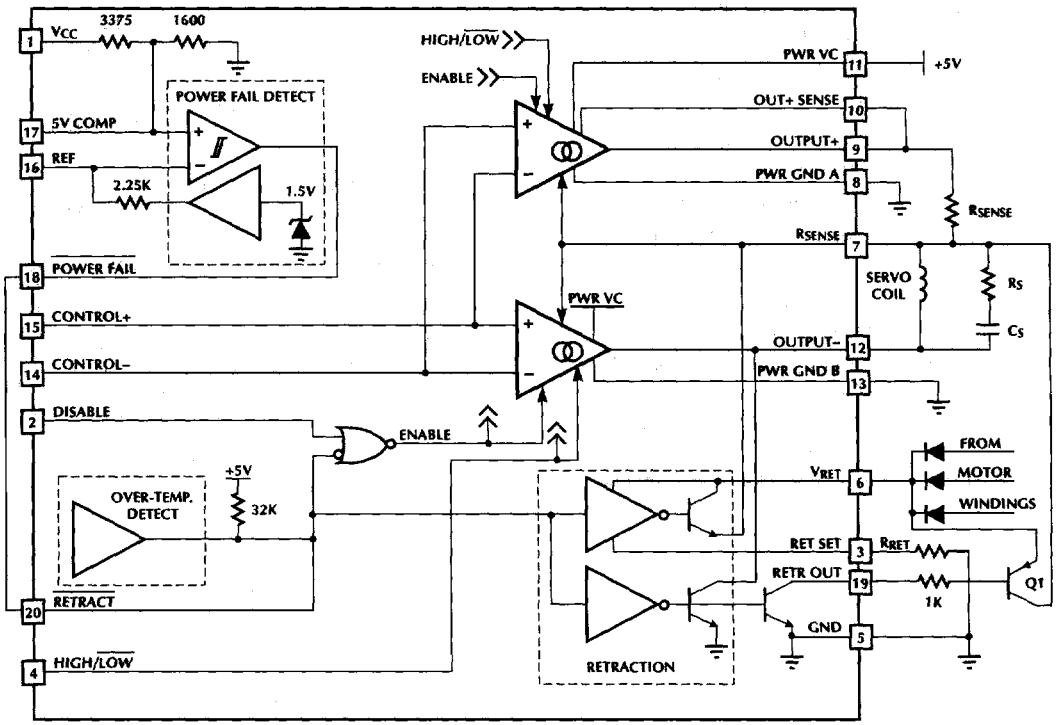
The power fail detection circuit includes a precision 1.5V bandgap reference.

The ML4506 is implemented using Micro Linear's bipolar array technology. This allows for easy customizing of the IC for a user's specific application.

FEATURES

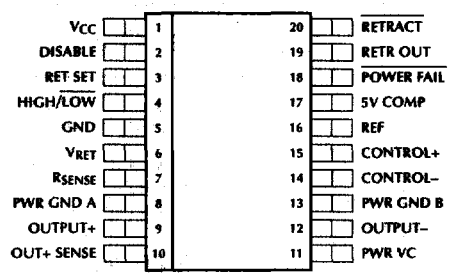
- 500mA power output with 1.3V total forward drop
- Low offsets, cross-over distortion and quiescent current
- Pin-programmable transconductance settings
- Retraction circuitry with programmable retract current, voltage limiting, and separate supply pin.
- On-chip precision power fail detect circuitry
- Over-temperature protection with flag output
- Logic input available for disabling outputs

BLOCK DIAGRAM



PIN CONNECTION

ML4506
20-PIN SOIC (S20W) OR 20-PIN SSOP (R20W)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	V_{CC}	Positive Power supply for the IC. Normally connected to +5V.
2	DISABLE	A logic "1" turns off the main outputs.
3	RET SET	A Current into this sets up the voltage limit for the internal retract sourcing circuit
4	HIGH/$\overline{\text{LOW}}$	A logic "1" sets the transconductance gain to 1/4 while a logic "0" sets the gain to 1/24. Transconductance gain is defined as: $\frac{V_{R_{SENSE}}}{(\text{CONTROL+}) - (\text{CONTROL–})}$
5	GND	Analog Signal Ground
6	V_{RET}	Power supply for the retract circuit.
7	R_{SENSE}	Current sensing resistor terminal.
8	PWR GND A	Ground Terminal for power amplifier A.
9	OUTPUT+	Positive Output terminal for bridge amplifier.
10	OUT+ SENSE	Positive Amplifier Kelvin sense terminal. Tie to OUTPUT+.
11	PWR VC	+5V supply for bridge amplifier
12	OUTPUT–	Negative Output terminal for bridge amplifier.
13	PWR GND B	Ground Terminal for power amplifier.
14	CONTROL–	Negative input for current command.
15	CONTROL+	Positive input for current command.
16	REF	Reference input to the Power Fail comparator. Leave open to use internal 2.5V reference.
17	5V COMP	Input to the Power Fail Comparator. Can be connected to a bypass capacitor for noise immunity.
18	$\overline{\text{POWER FAIL}}$	Open collector output drives low if pin 17 or pin 18 are below pin 16. Normally tied to pin 20.
19	RETR OUT	Open collector output pulls low to drive external PNP for retract if V_{CC} is less than 3.5V and pin 20 is low.
20	$\overline{\text{RETRACT}}$	A logic "0" input causes the main outputs to tri-state and the retraction circuit to activate. This input also functions as a flag output and will go low in the event of an over-temperature condition.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 1,6,11) 7V
Voltage Pins 2,4,18,19,20 ..... –0.3V to +7V
Pins 14, 15 ..... –0.3 to +V_{CC}
Output Current ..... ±750mA
Retraction Current 80mA
Retract set current (pin 3) 3mA

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA})
SOIC Package (S) ..... 55°C/W
SSOP Package (R) ..... 65°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage (pins 1,11) ..... 5V ± 10%
V_{RET} (pin 6) ..... 1V to V_{CC}

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = 5V ± 10%, R_{SENSE} = 1Ω, CONTROL– (pin 15) = 2.5V, R_{SET} (pin 3) = 3.7kΩ, Load = 10Ω.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
AMPLIFIER					
Control Common Mode Range		0.5		V_{CC} – 1	V
Offset				±10	mV
Transconductance Gain	pin 4 = 2V pin 4 = 0.8V	238 39.6	250 41.7	263 43.8	mA/V mA/V
Bandwidth			100		kHz
Sinking saturation	I_{OUT} = 100mA I_{OUT} = 300mA I_{OUT} = 500mA			0.5 0.6 0.8	V V V
Sourcing saturation	I_{OUT} = 100mA I_{OUT} = 300mA I_{OUT} = 500mA			1.1 1.2 1.3	V V V
RETRACTION CIRCUIT V_{PIN20} = 0.8V, V_{RET} = 2.5V					
I_{RET} SET			0.75		V
Turn on time			300		ns
Turn off time			8		µs
Sink current (I_{PIN12})	V_{PIN12} = 0.4V	34	50	150	mA
Source Voltage (V_{PIN7})	I_{PIN7} = –50mA	0.3	0.5	0.7	V
POWER FAIL DETECTION CIRCUIT					
Reference Voltage		1.35	1.50	1.65	V
Reference Source Impedance			2.25		kΩ
5V Threshold Hysteresis		4.40	4.575 30	4.75	V mV
LOGIC INPUTS					
Voltage High (V_{IH})		2	1.4		V
Voltage Low (V_{IL})			1.4	0.8	V
Current High (I_{IH})	V_{IN} = 5V			±10	mA
Current Low (I_{IL})	V_{IN} = 0V, except pin 20 V_{IN} = 0V, pin 20 only	–40 –250	–10 –160		mA mA
CURRENT CONSUMPTION					
Pin 1 + Pin 11	V_{PIN14} = V_{PIN15} = 2.5V		10	15	mA
Pin 6	V_{PIN14} = 2.5V		2.5	5.0	mA

FUNCTIONAL DESCRIPTION

POWER AMPLIFIER

The ML4506 power amplifier circuit is set up as a Howland Current source with a fixed gain of 1/4 or 1/24 (set by driving pin 4 high or low respectively). This architecture yields minimal cross-over distortion while maintaining low output cross conduction currents.

The gain figure refers to the ratio of input voltage to the output voltage seen across R_{SENSE}. For example, at a 1/4 gain setting, with V(–) input at 2.5V and the V(+) input at 3.5V, +500mA would flow through the coil using a 0.5Ω sense resistor. Under the same conditions with pin 4 low, the current would be 83mA. The ability to change from low to high gain allows more complete utilization of DAC resolution when in the track follow mode.

The output stage (figure 2) is designed to provide minimal saturation losses and employs a "composite PNP" for the sourcing drive and a saturable NPN to sink current. Sourcing saturation drop is typically 0.9V while sinking saturation drop is typically 0.4V.

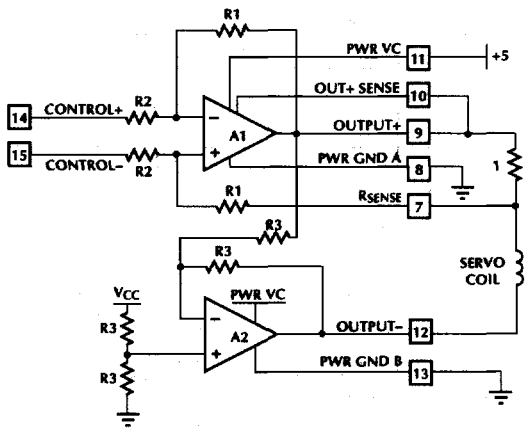


Figure 1. Power Amplifier Topology.

POWER FAIL DETECT

The ML4506 power fail detection circuit consists of a precision trimmed reference, resistor dividers, and a comparator with an effective hysteresis of 30mV. The output at pin 18 is open-collector and is normally tied to pin 1 which is internally pulled-up to 5V.

RETRACT

The retract circuit features provision for very low voltage operation as well as voltage limiting when a "live" retract with 5V on V_{RET} is performed. When pin 20 goes low, the internal NPN transistor will saturate, pulling SINK B (pin 11) low. A RETR OUT signal (open collector) saturates to drive an external PNP source transistor when pin 20 is low and when V_{RET} (pin 6) is below 3.5V. This portion of the circuit will function with less than 1V on V_{RET}.

An internal voltage limited pull-up circuit is provided which sources current on pin 7 to the VCM. This limit is set by an external resistor (see fig. 7) This circuit will operated reliably down to a V_{RET} voltage of around 2.5V. Pin 20 (Retract input) also serves as a flag to indicate an over-temperature condition on the die and goes low when the die temperature exceeds a safe operating limit (about 160°C).

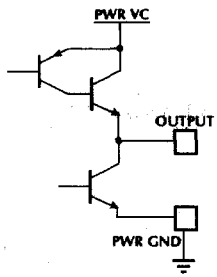


Figure 2. Power Output Stage.

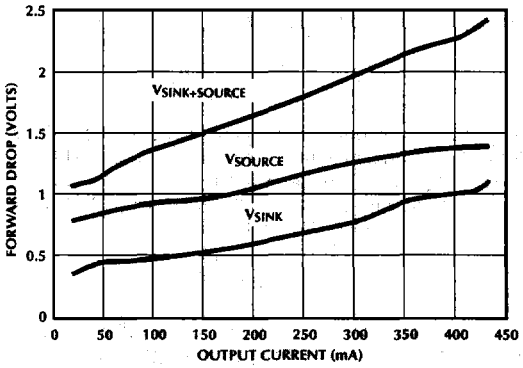


Figure 3. Output Saturation Voltage vs. Output Current. (V_{CC} = PWR VC = 5V)

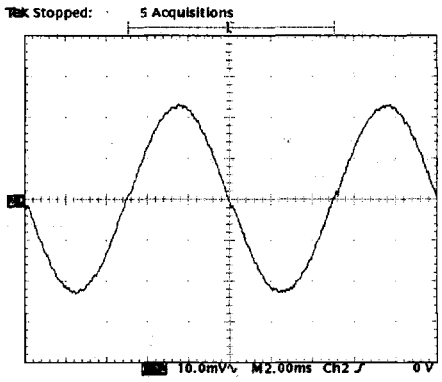


Figure 4. Output Current: V_{IN} = 100Hz Sine Wave, 100mA$_{P-P}$ Low Gain Mode ($V_{PIN\,5}$ = 0), R_{SENSE} = 0.5Ω, R_L = 10Ω.

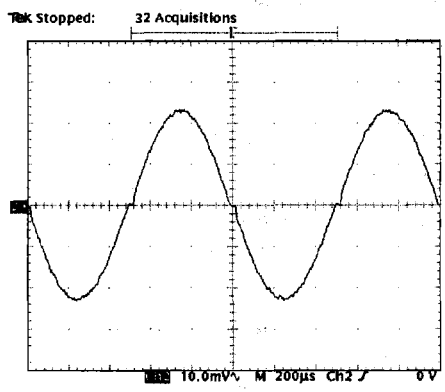


Figure 5. Output Current: V_{IN} = 1kHz Sine Wave, 100mA$_{P-P}$ Low Gain Mode ($V_{PIN\,5}$ = 0), R_{SENSE} = 0.5Ω, R_L = 10Ω.

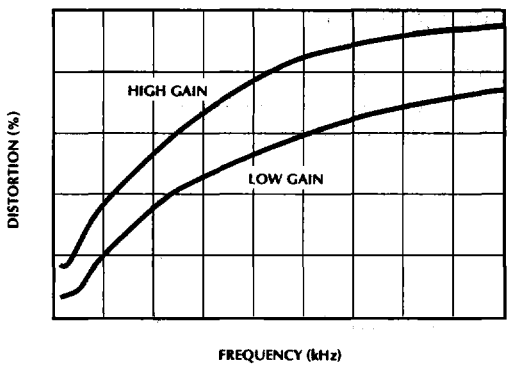


Figure 6. Total Harmonic Distortion vs. Frequency. Low Gain Setting (V_{PIN5} = 0), R_{SENSE} = 1Ω, V_{IN} = 2.4V$_{P-P}$ High Gain Setting (V_{PIN5} = 0), R_{SENSE} = 1Ω, V_{IN} = 0.4V$_{P-P}$

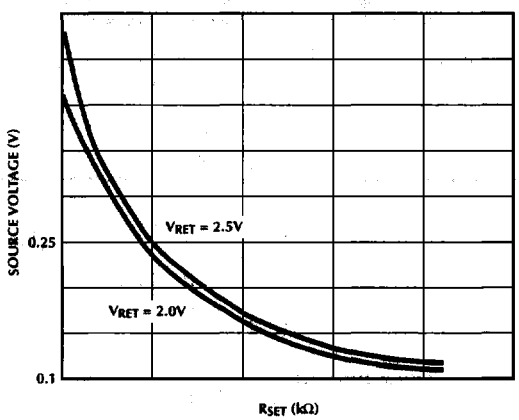


Figure 7. R_{SET} vs. Retract Source Voltage Limit.

APPLICATIONS

COMPENSATION

Figure 8 shows the equivalent AC circuit for the transconductance amplifier.

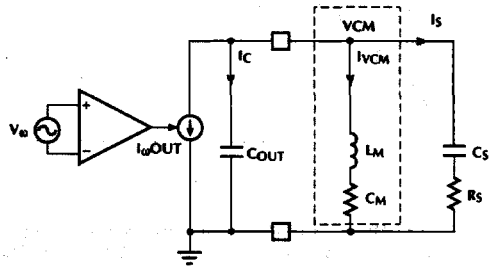


Figure 8. AC Equivalent Circuit for Current Amplifier, Voice Coil Motor (VCM) and Snubber.

The amplifier's current bandwidth is limited by C_{OUT} which varies with the value chosen for R_{SENSE}

$$C_{OUT} = \frac{25nF}{R_{SENSE}}$$

With no snubber (RS and CS) the bandwidth is limited to:

$$F_{-3dB} = \frac{1}{2\pi}\sqrt{\frac{2.414}{L(M)\,C(OUT)}}$$

Since this is a second order system with L(M) and C(OUT) forming a resonant circuit, some damping is desirable to reduce ringing in the step response. This is accomplished with resistive snubber. The optimum value of R(S) occurs when the following condition is met:

$$R(S) = \sqrt{\frac{L(VCM)}{C(OUT)}}$$

For a given C(S), setting R(S) to this value will minimize the ringing in the transient response. Larger values of R(S) will result in more ringing and more bandwidth. Smaller values of R(S) will result in more ringing and less bandwidth. R(S) should not exceed 300Ω.

C(S) (snubber capacitor) values of between 200nF and 1µF are usually necessary to acheive the desired reduction of ringing in the step response. At optimum value of R(S) larger values of C(S) further reduce the ringing but do not affect the bandwidth.

Tuning the current loop response can be best done simulating the network in figure 8 with a computer simulator (such as SPICE).

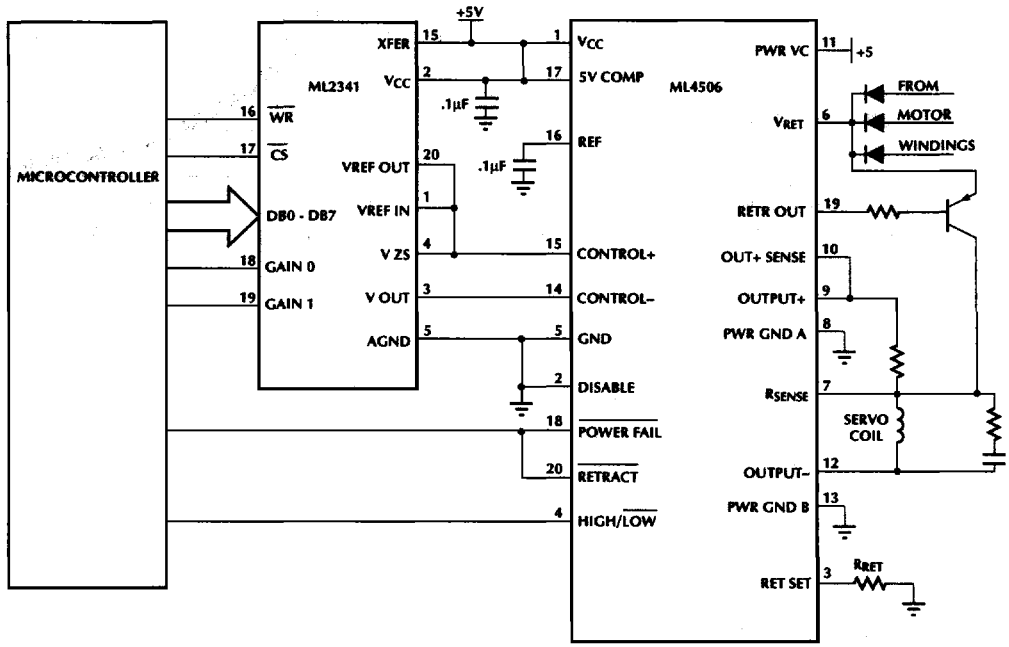


Figure 9. Typical Application: ML4506 used with ML2341 8-bit DAC provides up to 12-bit effective resolution.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4506CS	0°C to 70°C	20-Pin SOIC (S20W)
ML4506CR	0°C to 70°C	20-Pin SSOP (R20)