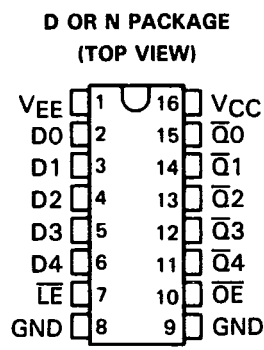


10K ECL-TO-TTL LEVEL TRANSLATOR WITH LATCH

T-52-11

D3058, NOVEMBER 1987—REVISED DECEMBER 1988

- ECL Control Inputs
- 3-State Outputs
- 10K ECL Input Compatible
- Package Options Include Plastic "Small Outline" Package and Standard Plastic 300-mil DIPs
- Direct Replacement for National Semiconductor DP8480



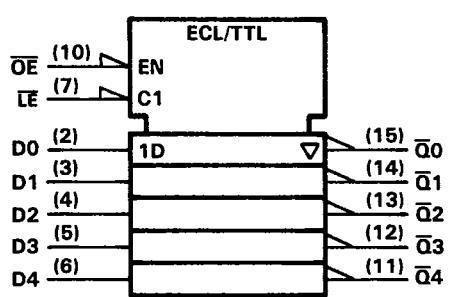
description

This circuit translates ECL input levels to TTL output levels and provides an inverting transparent latch. The 3-state outputs are designed to drive highly capacitive loads. All inputs operate at ECL levels.

If Latch Enable (\overline{LE}) is low, the latches are transparent and the \overline{Q} outputs follow the complement of the D inputs. If \overline{LE} is high, the outputs are latched. If output enable (\overline{OE}) is high, the outputs are in the high-impedance state, as they are during power up and power down.

The DP8480 is characterized for operation from 0°C to 75°C.

logic symbol†

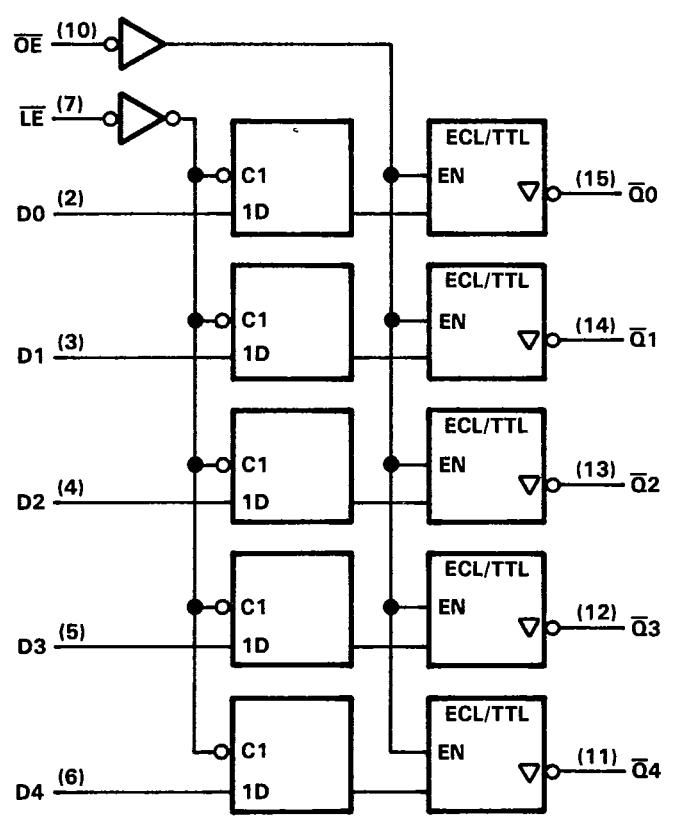


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH LATCH/TRANSLATOR)

\overline{OE}	\overline{LE}	D	\overline{Q}
H	X	X	Z
L	L	L	H
L	L	H	L
L	H	X	Q_0

logic diagram



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DP8480

10K ECL-TO-TTL LEVEL TRANSLATOR WITH LATCH

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T-52-11

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Supply voltage, V_{EE}	-8 V
Input voltage, V_I	0 V to V_{EE}
Output voltage, V_O	5.5 V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 75°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 75^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	570 mW
N	1150 mW	9.2 mW/°C	690 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{EE}	-4.68	-5.20	-5.72	V
High-level input voltage, V_{IH} (see Note 1)	$T_A = 0^\circ\text{C}$		-840	mV
	$T_A = 25^\circ\text{C}$		-810	
	$T_A = 75^\circ\text{C}$		-720	
Low-level input voltage, V_{IL} (see Note 1)	$T_A = 0^\circ\text{C}$		-1490	mV
	$T_A = 25^\circ\text{C}$		-1475	
	$T_A = 75^\circ\text{C}$		-1450	
Pulse duration, \overline{LE} low, t_w		5		ns
Setup time, data before $\overline{LE}1$, t_{su}		3		ns
Hold time, data after $\overline{LE}1$, t_h		3		ns
Operating free-air temperature, T_A		0	75	°C

NOTE 1: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH} High-level output voltage	$I_{OH} = -10\text{ mA}$	$V_{CC} - 2$			V
V_{OL} Low-level output voltage	$I_{OL} = 12\text{ mA}$		0.2	0.5	V
I_{IH} High level input current	$V_{IH} = V_{IH\text{ max}}$		75	350	μA
I_{IL} Low-level input current	$V_{IL} = V_{IL\text{ min}}$		50	85	μA
I_{OHS} High-state short-circuit output current	$V_{OHS} = 0$, See Note 2	-70	-150		mA
I_{OLS} Low-state short-circuit output current	$V_{OLS} = 2.5\text{ V}$, See Note 2	70	150		mA
I_{OZ} High-impedance state output current	$V_O = 0$ to 5 V		± 1	± 50	μA
I_{CC} Supply current from V_{CC}	Outputs open, Inputs = V_{IL}		16	35	mA
I_{EE} Supply current from V_{EE}	Outputs open, Inputs = V_{IL}		-30	-50	mA

†Typical values are at $V_{CC} = 5\text{ V}$, $V_{EE} = -5.2\text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 2: During testing of I_{OHS} or I_{OLS} , only one output should be tested at a time and the current should be limited to a maximum of $\pm 120\text{ mA}$.

10K ECL-TO-TTL LEVEL TRANSLATOR WITH LATCH

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high-level output from \overline{LE} input	C _L = 50 pF, See Figure 1	4	10	15	ns
t _{PHL} Propagation delay time, high-to-low-level output from \overline{LE} input		4	11	15	ns
t _{PLH} Propagation delay time, low-to-high-level output from D input		3.5	10	15	ns
t _{PHL} Propagation delay time, high-to-low-level output from D input		3.5	11	15	ns
t _{en} Output enable time from \overline{OE} input		6	12	25	ns
t _{dis} Output disable time from \overline{OE} input		4.5	8	22	ns

†Typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C, and with all channels switched simultaneously.

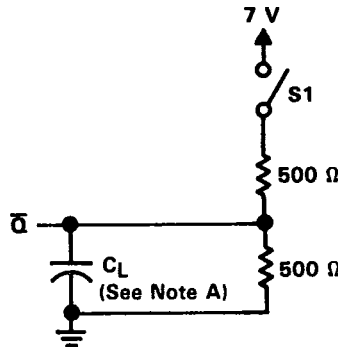
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10K ECL-TO-TTL LEVEL TRANSLATOR WITH LATCH

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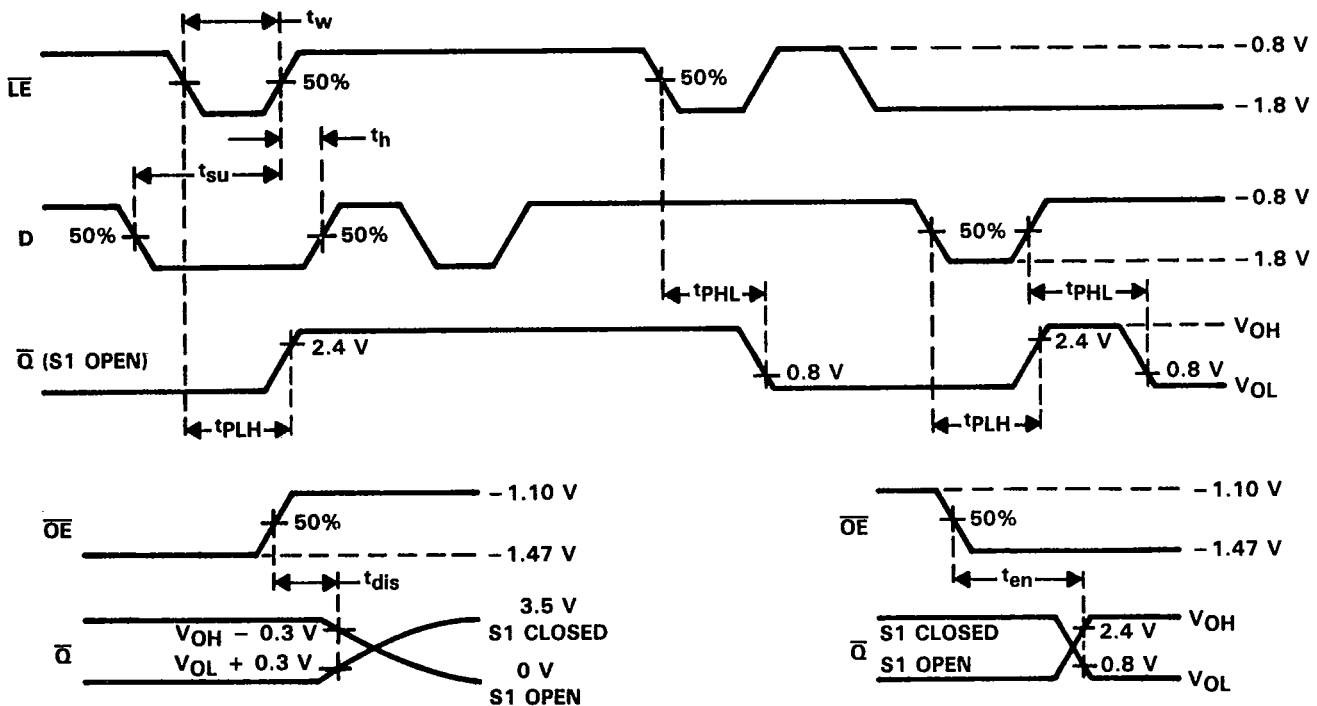
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PARAMETER MEASUREMENT INFORMATION



OUTPUT LOAD CIRCUIT

NOTE A: C_L includes probe and jig capacitance.



NOTE B: ECL input rise times and fall time are $2\text{ ns} \pm 0.2\text{ ns}$ from 20% to 80%.

FIGURE 1. SWITCHING CHARACTERISTICS