**THNCFxxxMAA Series

CompactFlash™ Card

OUTLINE

The THNCF***MAA series CompactFlash™ card is a flash technology based with ATA interface flash memory card. It is constructed with flash disk controller chip and NAND-type（Toshiba）flash memory device. The CompactFlash™ card operates in both 5-Volt and 3.3-Volt power supplies. It comes in capacity of 8, 16, 32, 48, 64, 96, 128, 160, 192, 256, 320, 384 and up to 512 MB unformatted for type-I card. Emulating IDE hard disk drives and being certified in accordance with the CompactFlash™ Certification Plan it is a perfect choice of solid-state mass-storage cards for battery backup handheld devices such as Digital Camera, Audio Player, PDA, or the applications which require high environment tolerance with high performance sustained write speed.

FEATURES

CompactFlash™ Compatibility

Certified in accordance with the CompactFlash™ Certification Plan
Substantially compatible with PC Card standard and PC Card ATA
Support for CIS implemented with 256 bytes of attribute memory

ATA/IDE interface

ATA command set compatible
Support for 8- or 16-bit host transfers
Programmable and auto-wait-state generation for compatibility with any host speed using IORDY

High performance

Fast ATA host-to-buffer burst transfer rates up to 20 Mbytes/second
Supports PIO mode 4, both at 16.6 Mbytes/second
Buffer transfer rates to and from flash memory up to 12.5 Mbytes/second
Sustained write : up to 1.5 Mbytes/second (8MB~48MB), 3.2 Mbytes/second(64MB~512MB)
Sustained read : up to 5.6Mbytes/second
Card capacity of 8, 16, 32, 48, 64, 96, 128, 160, 192, 256, 320, 384 and up to 512 MB Mbytes available
Single +5 Volt or 3.3 Volt power supply and very low power consumption with automatic power management.

NOTES

CompactFlash™ is a trademark of SanDisk Corporation and is licensed royalty-free to the CFA, which in turn will license it royal-free to CFA members.
CFA: CompactFlash™ Association.

Products Models

unformatted	Cylinder	Head	Sector	Model No.
8MB	244	2	32	THNCF008MAA
16MB	244	4	32	THNCF016MAA
32MB	488	4	32	THNCF032MAA
48MB	732	4	32	THNCF048MAA
64MB	976	4	32	THNCF064MAA
96MB	732	8	32	THNCF096MAA
128MB	976	8	32	THNCF128MAA
160MB	610	16	32	THNCF160MAA
192MB	732	16	32	THNCF192MAA
256MB	976	16	32	THNCF256MAA
320MB	814	16	48	THNCF320MAA
384MB	977	16	48	THNCF384MAA
512MB	993	16	63	THNCF512MAA

Product Specifications

Dimensions:

Type I card: 36.4mm(L) x 42.8mm (W) x 3.3mm (H)
Weight: 14.2 g or 0.5 oz

Storage Capacities:

8,16, 32, 48, 64, 96, 128, 160, 192, 256, 320, 384 and up to 512 MB Mbytes (unformatted)

System Compatibility:

Please refer to the compatibility list.

Performance:

Data Transfer Rates:	up to 4.1Mbyte/s in ATA PIO mode 4
To/from Flash memory:	up to 12.5 Mbytes/s
To/from host:	up to 20Mbytes/s
Sustained write:	up to 2.98Mbyte/s in ATA PIO mode 4
Sustained read:	up to 5.62Mbyte/s in ATA PIO mode 4
Command to DREQ:	<4ms
Idle to Read	<1 µs
Idle to Write	<1 µs
SRAM data buffer	6 KBytes SRAM

Operating Voltage: 3.3V / 5V +/- 10%

Power consumption:

Read mode	30 mA (typ)
Write mode	30 mA (typ)
Sleep mode	100uA (typ)

Environment conditions:

Operating temperature	0℃ to 60℃
Storage temperature	-20℃ to 65℃
Relative humidity	95%(Max)

Electrical Specification

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
Vcc	Power Supply Voltage	−0.3 to 7	V
Vin	Input Voltage	−0.3 to 7	V
Tstg	Storage Temperature	−20 to 65	℃
Topr	Operating Temperature	0 to 60	℃

DC RECOMMENDED OPERATING CONDITIONS

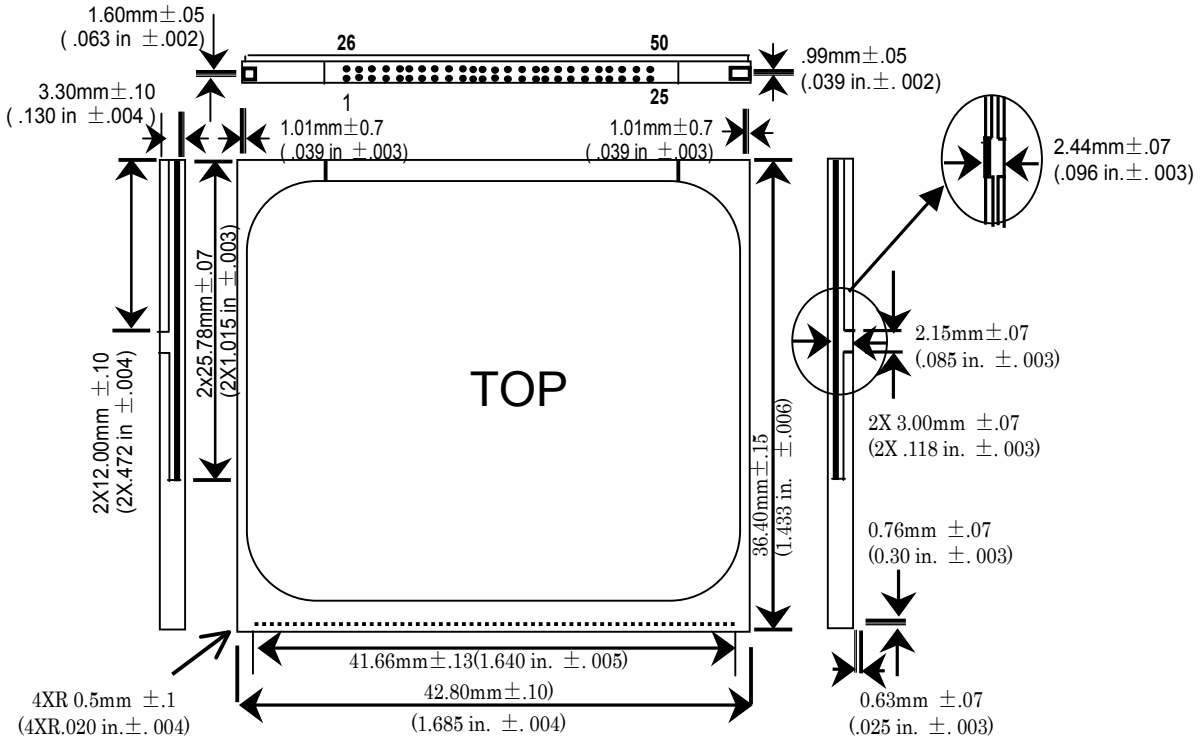
SYMBOL	PARAMETER	MIN	MAX	UNIT
Vcc	Power Supply Voltage	3.0	5.5	V
ViH	High Level Input Voltage	2.2	Vcc+0.3	V
ViL	Low Level Input Voltage	−0.3 *	0.8	V

Note: * 0.8V (Pulse width <= 10nS)

DC CHARACTERISTICS (Ta = 0℃ to 65℃, Vcc = 3.15V to 5.5V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Icco	Operating Current		26	50	mA
Iccs	Sleep Mode Current		75	200	uA
VoH	High Level Output Voltage	2.4			V
VoL	Low Level Output Voltage			0.4	V

Physical Specifications



Note: The optional notched configuration was shown in the CF Specification Rev.1.0. In Specification Rev. 1.2. the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

Type I CompactFlash Storage Card and CF+ Card Dimensions

Electrical Interface

Physical Description

The host is connected to the CompactFlash Storage Card or CF+ Card using a standard 50-pin connector. The connector in the host consists of two rows of 25 male contacts each on 50 mil (1.27 mm) centers.

Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 4. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Section 4.3 defines the DC characteristics for all input and output type structures.

Electrical Description

The CompactFlash Storage Card functions in three basic modes: 1) PC Card ATA using I/O Mode, 2) PC Card ATA using Memory Mode and 3) True IDE Mode, which is compatible with most disk drives. CompactFlash Storage Cards are required to support all three modes. The CF Cards normally function in the first and second modes, however they can optionally function in True IDE mode. The configuration of the CompactFlash Card will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the storage card.or for True IDE Mode, pin 9 being grounded. The configuration of the CF Card will be controlled using configuration registers. The configuration registers are starting at the address defined in the Configuration Tuple (CISTPL_CONFIG) in the Attribute Memory space of the CF Card. Signals whose source is the host are designated as inputs while signals that the CompactFlash Storage Card sources are outputs. The CompactFlash Storage Card logic levels conform to those specified in the PCMCIA Release 2.1 specification. Each signal has three possible operating modes:

1) PC Card Memory mode
2) PC Card I/O mode
3) True IDE mode

True IDE mode is required for CompactFlash Storage cards. All outputs from the card are totem pole except the data bus signals that are bi-directional tri-state.

Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin Num.	Signal Name	Pin Type	In,Out Type	Pin Num.	Signal Name	Pin Type	In,Out Type	Pin Num.	Signal Name	Pin Type	In,Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09[2]	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08[2]	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07[2]	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC	I	Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06[2]	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05[2]	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04[2]	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03[2]	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3
23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3
28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3
29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3
30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3
31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3
32	-CE2[1]	I	I3U	32	-CE2[1]	I	I3U	32	-CS[1]	I	I1Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD	I	I3U	34	-IORD	I	I3U	34	-IORD	I	I3Z
35	-IOWR	I	I3U	35	-IOWR	I	I3U	35	-IOWR	I	I3Z
36	-WE	I	I3U	36	-WE	I	I3U	36	-WE[3]	I	I3U

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin Num.	Signal Name	Pin Type	In,Out Type	Pin Num.	Signal Name	Pin Type	In,Out Type	Pin Num.	Signal Name	Pin Type	In,Out Type
37	RDY/BSY	O	OT1	37	IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		POWER	38	VCC		Power	38	VCC		Power
39	-CSEL	I	I2Z	39	-CSEL	I	I2Z	39	-CSEL	I	I2U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	-RESET	I	I2Z
42	-WAIT	O	OT1	42	-WAIT	O	OT1	42	IORDY	O	ON1
43	-INPACK	O	OT1	43	-INPACK	O	OT1	43	-INPACK	O	OZ1
44	-REG	I	I3U	44	-REG	I	I3U	44	-REG[3]	I	I3U
45	BVD2	I/O	I1U, OT1	45	-SPKR	I/O	I1U,OT1	45	-DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U, OT1	46	-STSCHG	I/O	I1U,OT1	46	-PDIAG	I/O	I1U,ON1
47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z,OZ3	47	D08[1]	I/O	I1Z,OZ3
48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z,OZ3	48	D09[1]	I/O	I1Z,OZ3
49	D10[1]	I/O	I1Z, OZ3	49	D10[1]	I/O	I1Z,OZ3	49	D10[1]	I/O	I1Z,OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

Note: 1. These signals are required only for 16bit access and not required when installed in 8-bit systems. Devices should allow for 3-state signals not to consume current.

2. Should be grounded by the host.

3. Should be tied to VCC by the host.

4. Optional for CF+Cards, required for CompactFlash Storage Cards.

Signal Description

Signal Name	Dir.	Pin	Description
A10 - A0 (PC Card Memory Mode)	I	8,10,11,12 14,15,16,17, 18,19,20	These address lines along with the –REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+Card, a byte in the card's information structure and its configuration control and status registers.
A10 – A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 – A0 (True IDE Mode)	I	18,19,20	In True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+Card. They are used by the host to determine that the CompactFlash Storage Card or CF+Card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word, -CE1accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Tables 4-11, 4-12, 4-15, 4-16 and 4-17.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.

Signal Name	Dir.	Pin	Description
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 – D00 (PC Card Memory Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2,23, 22,21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 – D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15 – D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00–D07 while all data transfers are 16bit using D00–D15.
GND (PC Card Memory Mode)	-	1, 50	Ground
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
-INPACK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+Card and the CPU.
-INPACK (True IDE Mode)			In True IDE mode this output signal is not used and should not be connected at the host.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF+Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Strage Card or CF+Card controller registers when the CompactFlash Storage Card or CF+Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal(trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Signal Name	Dir.	Pin	Description
-OE (PC Card Memory Mode) -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Strage Card or CF+Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this Input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode) -IREQ (PC Card I/O Mode) INTRQ (True IDE Mode)	O	37	In Memory Mode this signal is set high when the CompactFlash Storage Card or CF+Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low(busy) until the CompactFlash Storage Card or CF+Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+Card during this time. The RDY/-BSY signal is held high(disabled from being busy) whenever the following condition is true: The CompactFlash Storage Card or CF+Card has been powered up with +RESET continuously disconnected or asserted. I/O Operation –After the CompactFlash Storage Card or CF+Card has been configured for I/O operation, this signal is used as –Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select -REG (PC Card I/O Mode) -REG (True IDE Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus. In True IDE Mode this input signal is not used and should be connected to VCC by the host.
RESET (PC Card Memory Mode) RESET (PC Card I/O Mode) -RESET (True IDE Mode)	I	41	When the pin is high, this signal Resets the CompactFlash Storage Card or CF+Card. The CompactFlash Storage Card or CF+Card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card or CF+Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode)	-	13,38	+5V, +3.3V power This signal is the same for all modes. This signal is the same for all modes.

Signal Name	Dir.	Pin	Description
-VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode)	O	33 40	Voltage Sense Signals. –VS1 is grounded so that the CompactFlash Storage Card or CF+Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode) -WAIT (PC Card I/O Mode) IORDY (True IDE Mode)	O	42	The –WAIT signal is driven low by the CompactFlash Storage Card or CF+Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode this output signal may be used as IORDY.
-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card Storage Card or CF+Card when the card is configured in the memory interfacce mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O Mode) -IOIS 16 (True IDE Mode)	O	24	Memory Mode – The CompactFlash Storage Card or CF+Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation – When the CompactFlash Storage Card or CF+Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16Bit Port (-IOIS16) function. A Low signal indicates that a 16bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

Access Specifications

1. Attribute access specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of –REG="L" as follows. That region can be accessed by Byte/World/Old-byte modes, which are defined by PC card standard specifications.

Attribute Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	High-Z	High-Z
Byte access(8-bit)	L	H	L	L	L	H	High-Z	even byte
	L	H	L	H	L	H	High-Z	invalid
Word access(16-bit)	L	L	L	x	L	H	invalid	even byte
Odd byte access(8-bit)	L	L	H	x	L	H	invalid	High-Z

Note: x: L or H

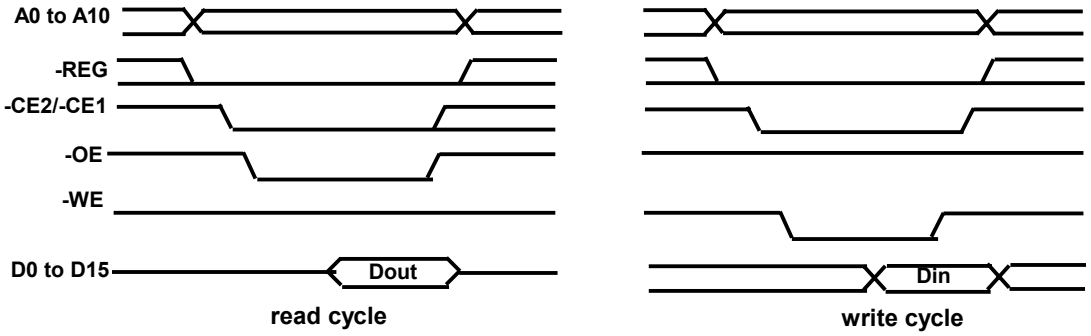
Attribute Write Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	Don't care	Don't care
Byte access(8-bit)	L	H	L	L	H	L	Don't care	even byte
	L	H	L	H	H	L	Don't care	Don't care
Word access(16-bit)	L	L	L	x	H	L	Don't care	even byte
Odd byte access(8-bit)	L	L	H	x	H	L	Don't care	Don't care

Note: x: L or H

Note: write CIS-ROM region is invalid.

Attribute Access Timing Example



Task File register access specifications

There are two cases of Task File register mapping, one is mapped I/O address area, the other is mapped Memory address area. Each case of Task File registers read and write operations is executed under the condition as follows. That area can be accessed by Byte/World/Odd Byte modes, which are defined by PC card standard specifications.

(1) I/O address map

Task File Register Read Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	x	x	High-Z	High-Z
Byte access(8-bit)	L	H	L	L	L	H	H	H	High-Z	even byte
	L	H	L	H	L	H	H	H	High-Z	odd byte
Word access(16-bit)	L	L	L	x	L	H	H	H	odd byte	even byte
Odd byte access(8-bit)	L	L	H	x	L	H	H	H	odd byte	High-Z

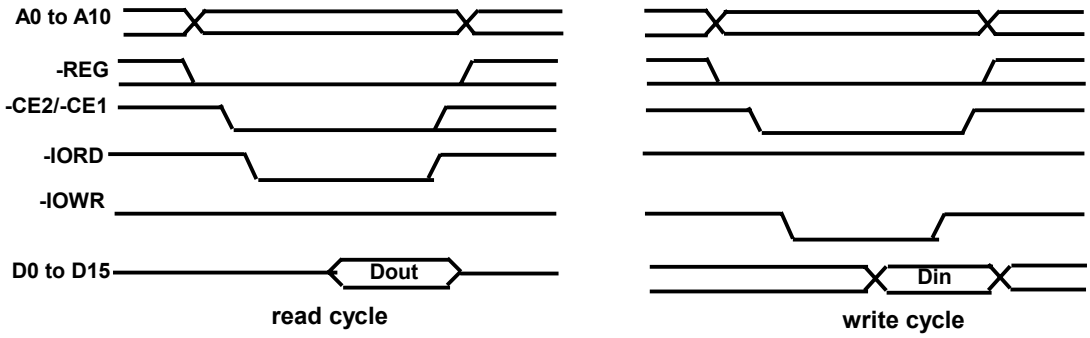
Note: x: L or H

Task File Register Write Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	x	x	Don't care	Don't care
Byte access(8-bit)	L	H	L	L	H	L	H	H	Don't care	even byte
	L	H	L	H	H	L	H	H	Don't care	odd byte
Word access(16-bit)	L	L	L	x	H	L	H	H	odd byte	even byte
Odd byte access(8-bit)	L	L	H	x	H	L	H	H	odd byte	Don't care

Note: x: L or H

Task File Register Access Timing Example (1)



Memory address map

Task File Register Read Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	x	x	High-Z	High-Z
Byte access(8-bit)	H	H	L	L	L	H	H	H	High-Z	even byte
	H	H	L	H	L	H	H	H	High-Z	odd byte
Word access(16-bit)	H	L	L	x	L	H	H	H	odd byte	even byte
Odd byte access(8-bit)	H	L	H	x	L	H	H	H	odd byte	High-Z

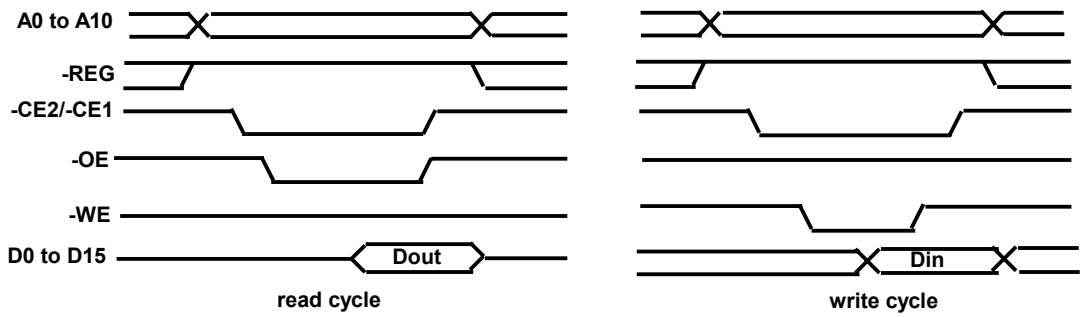
Note: x: L or H

Task File Register Write Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	x	x	Don't care	Don't care
Byte access(8-bit)	H	H	L	L	H	L	H	H	Don't care	even byte
	H	H	L	H	H	L	H	H	Don't care	odd byte
Word access(16-bit)	H	L	L	x	H	L	H	H	odd byte	even byte
Odd byte access(8-bit)	H	L	H	x	H	L	H	H	odd byte	Don't care

Note: x: L or H

Task File Register Access Timing Example (2)



True IDE Mode

The card can be configured in a True IDE This card is configured in this mode only when the-OE input signal is asserted GND by the host. In this True IDE mode Attribute Registers are not accessible from the host. Only I/O operation to the task file and data register is allowed. If this card is configured during power on sequence, data register is accessed in word (16-bit). The card permits 8-bit accessed if the user issues a Set Feature Command to put the device in 8-bit mode.

True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-OWR	D8 to D15	D0 to D7
Invalid mode	L	L	x	x	x	High-Z	High-Z
Standby mode	H	H	x	x	x	High-Z	High-Z
Data register access	H	L	0	L	H	odd byte	even byte
Alternate status access	L	H	6H	L	H	High-Z	status out
Other task file access	H	L	1-7H	L	H	High-Z	data

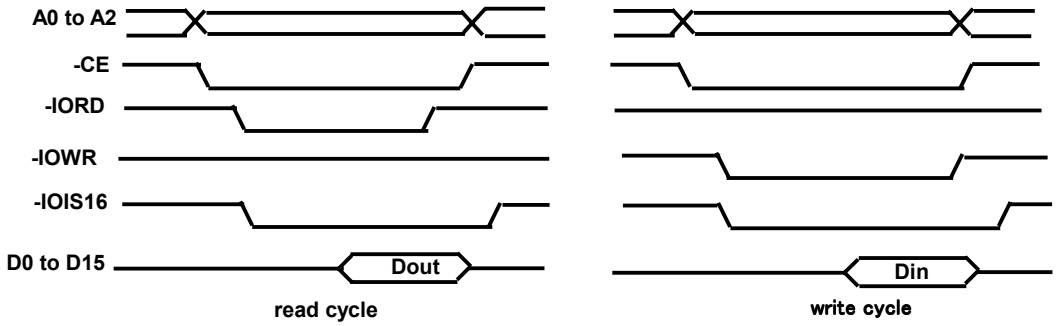
Note: x: L or H

True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-OWR	D8 to D15	D0 to D7
Invalid mode	L	L	x	x	x	don't care	don't care
Standby mode	H	H	x	x	x	don't care	don't care
Data register access	H	L	0	H	L	odd byte	even byte
Control register access	L	H	6H	H	L	don't care	control in
Other task file access	H	L	1-7H	H	L	don't care	data

Note: x: L or H

True IDE Mode I/O Access Timing Example



Configuration register specifications

This card supports four Configuration registers for the purpose of the configuration and observation of this card. These registers can be used in memory card mode and I/O card mode. In True IDE mode, these registers can not be used.

1. Configuration Option register(Address 200H)

This register is used for the configuration of the card configuration status and for the issuing soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRESET	LevlREQ	INDEX					

Note: initial value: 00H

Name	R/W	Function
SRESET	R/W	Setting this bit to "1", places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit set to "0", places the card in the reset state of Hard Reset (This bit is set to "0" by Hard Reset). Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.
LevlREQ (HOST->)	R/W	This bit sets to "0" when pulse mode interrupt is selected, and "1" when level mode interrupt is selected.
INDEX (HOST->)	R/W	This bits is used for select operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is "000000" for the purpose of Memory card interface recognition.

INDEX bit assignment

INDEX bit								
5	4	3	2	1	0	Card mode	Task File register address	Mapping mode
0	0	0	0	0	0	Memory card	0H to FH, 400H to 7FFH	Memory mapped
0	0	0	0	0	1	I/O card	xx0H to xxFH	contiguous I/O mapped
0	0	0	0	1	0	I/O card	1F0H to 1F7H,3F6H to 3F7H	primary I/O mapped
0	0	0	0	1	1	I/O card	1F0H to 177H,376H to 3F7H	Secondary I/O mapped

2. Configuration and Status register (Address 202H)

This register is used for observing the state of the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0

Note: initial value: 00H

Name	R/W	Function
CHGED (CARD->)	R	This bit indicates that CRDY/-BSY bit on Pin Replacement register is set to "1". When CHGED bit is set to "1", -STSCHG pin is held "L" at the condition of SIGCHG bit set to "1" and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal (-STSCHG pin). When the card is configured I/O card interface and this bit is set "1", -STSCHG pin is controlled by CHGED bit. If this bit is set to "0", -STSCHG pin is kept "H".
IOIS8 (HOST->)	R/W	The host sets this field to "1" when it can provide I/O cycles only with on 8 bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to "1", the card enters sleep state (Power Down mode). When this bit is reset to "0", the card transfers to idle state (active mode). RRDY/BSY bit on Pin Replacement Register becomes BUSY when this bit is changed. RRDY/BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle and powers back up when it receives a command.
INTR (CARD->)	R	This bit indicates the internal state of the interrupt request. This bit state is available whether I/O card interface has been configured or not. This signal remains true until the condition, which caused the interrupt request, has been serviced. If the –IEN bit in the Device Control Register disables interrupts, this bit is a zero.

3. Pin Replacement register (Address 204H)

This register is used for providing the state of –IREQ signal when the card configured I/O card interface.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	CRDY/–BSY	0	1	1	RRDY/–BSY	0

Note: initial value: 0CH

Name	R/W	Function
CRDY/–BSY (HOST–>)	R/W	This bit is set to "1" when the RRDY/–BSY bit changes state. The host may also write this bit.
RRDY/–BSY (HOST–>)	R	When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/–BSY bit masking.

4. Socket and Copy register (Address 206H)

This register is used for identification of the card from the other cards. Host can read and write this register. Host should set this register before this card's Configuration Option register set.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	DRV#	0	0	0	0

Note: initial value: 00H

Name	R/W	Function
DRV# (HOST–>)	R	These fields are used for the configuration of the plural cards. When host configures the plural cards, written the card's copy number in this field. In this way, host can perform the card's master/slave organization.

CIS information

CIS information of CompactFlash card is defined as follows.

Address	Data	Description of contents	CIS function
000H	01h	CISTPL_DEVICE	Tuple code
002H	03h	TPL_LINK	Tuple link
004H	d9h	Device information	Tuple data
006H	01h	Device information	Tuple data
008H	ffh	END MARKER	End of Tuple
00AH	1ch	CISTPL_DEVICE_OC	Tuple code
00CH	04h	TPL_LINK	Tuple link
00EH	03h	Conditions information	Tuple data
010H	d9h	Device information	Tuple data
012H	01h	Device information	Tuple data
014H	ffh	END MARKER	End of Tuple
016H	18h	CISTPL_JEDEC_C	Tuple code
018H	02h	TPL_LINK	Tuple link
01AH	dfh	PCMCIA's manufacture's JEDEC ID code	Tuple data
01CH	01h	PCMCIA's JEDEC device code	Tuple data
01EH	20h	CISTPL_MANFID	Tuple code
020H	04h	TPL_LINK	Tuple link
022H	00h	Low byte of manufacturer's ID code	Tuple data
024H	00h	High byte of manufacturer's ID code	Tuple data
026H	00h	Low byte of product code	Tuple data
028H	00h	High byte of product code	Tuple data
02AH	15h	CISTPL_VERS_1	Tuple code
02CH	20h	TPL_LINK	Tuple link
02EH	04h	TPLLV1_MAJOR	Tuple data
030H	01h	TPLLV1_MINOR	Tuple data
032H	xxh	' ' (Vender Specific Strings)	Tuple data
034H	xxh	' ' (Vender Specific Strings)	Tuple data
036H	xxh	' ' (Vender Specific Strings)	Tuple data
038H	xxh	' ' (Vender Specific Strings)	Tuple data
03AH	xxh	' ' (Vender Specific Strings)	Tuple data
03CH	xxh	' ' (Vender Specific Strings)	Tuple data
03EH	xxh	' ' (Vender Specific Strings)	Tuple data
040H	xxh	' ' (Vender Specific Strings)	Tuple data
042H	xxh	' ' (Vender Specific Strings)	Tuple data
044H	xxh	' ' (Vender Specific Strings)	Tuple data
046H	xxh	' ' (Vender Specific Strings)	Tuple data
048H	xxh	' ' (Vender Specific Strings)	Tuple data
04AH	xxh	' ' (Vender Specific Strings)	Tuple data
04CH	xxh	' ' (Vender Specific Strings)	Tuple data

04EH	xxh	' ' (Vender Specific Strings)	Tuple data
050H	xxh	' ' (Vender Specific Strings)	Tuple data
052H	xxh	' ' (Vender Specific Strings)	Tuple data
054H	xxh	' ' (Vender Specific Strings)	Tuple data
056H	xxh	' ' (Vender Specific Strings)	Tuple data
058H	00h	Null terminator	Tuple data
05AH	xxh	' ' (Vender Specific Strings)	Tuple data
05CH	xxh	' ' (Vender Specific Strings)	Tuple data
05EH	xxh	' ' (Vender Specific Strings)	Tuple data
060H	xxh	' ' (Vender Specific Strings)	Tuple data
062H	xxh	' ' (Vender Specific Strings)	Tuple data
064H	xxh	' ' (Vender Specific Strings)	Tuple data
066H	xxh	' ' (Vender Specific Strings)	Tuple data
068H	xxh	' ' (Vender Specific Strings)	Tuple data
06AH	00h	Null terminator	Tuple data
06CH	ffh	END MARKER	End of Tuple
06EH	21h	CISTPL_FUNCID	Tuple code
070H	02h	TPL_LINK	Tuple link
072H	04h	IC Card function code	Tuple data
074H	01h	System initialization bit mask	Tuple data
076H	22h	CISTPL_FUNCE	Tuple code
078H	02h	TPL_LINK	Tuple link
07AH	01h	Type of extended data	Tuple data
07CH	01h	Function information	Tuple data
07EH	22h	CISTPL_FUNCE	Tuple code
080H	03h	TPL_LINK	Tuple link
082H	02h	Type of extended data	Tuple data
084H	0ch	Function information	Tuple data
086H	0fh	Function information	Tuple data
088H	1ah	CISTPL_CONFIG	Tuple code
08AH	05h	TPL_LINK	Tuple link
08CH	01h	Size field	Tuple data
08EH	03h	Index number of last entry	Tuple data
090H	00h	Configuration register base address (Low)	Tuple data
092H	02h	Configuration register base address (High)	Tuple data
094H	0fh	Configuration register present mask	Tuple data
096H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
098H	08h	TPL_LINK	Tuple link
09AH	c0h	Configuration Index Byte	Tuple data
09CH	c0h	Interface Descriptor	Tuple data
09EH	a1h	Feature Select	Tuple data
0A0H	01h	Vcc Selection Byte	Tuple data
0A2H	55h	Nom V Paramete	Tuple data
0A4H	08h	Memory length (256 byte pages)	Tuple data

0A6H	00h	Memory length (256 byte pages)	Tuple data
0A8H	20h	Misc features	Tuple data
0AAH	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
0ACH	06h	TPL_LINK	Tuple link
0AEH	00h	Configuration Index Byte	Tuple data
0B0H	01h	Feature Select	Tuple data
0B2H	21h	Vcc Selection Byte	Tuple data
0B4H	b5h	Nom V Parameter	Tuple data
0B6H	1eh	Nom V Parameter	Tuple data
0B8H	4dh	Peak I Parameter	Tuple data
0BAH	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
0BCH	0ah	TPL_LINK	Tuple link
0BEH	c1h	Configuration Index Byte	Tuple data
0C0H	41h	Interface Descriptor	Tuple data
0C2H	99h	Feature Select	Tuple data
0C4H	01h	Vcc Selection Byte	Tuple data
0C6H	55h	Nom V Parameter	Tuple data
0C8H	64h	I/O param	Tuple data
0CAH	f0h	IRQ parameter	Tuple data
0CCH	ffh	IRQ request mask	Tuple date
0CEH	ffh	IRQ request mask	Tuple data
0D0H	20h	Misc features	Tuple data
0D2H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
0D4H	06h	TPL_LINK	Tuple link
0D6H	01h	Configuration Index Byte	Tuple data
0D8H	01h	Feature Select	Tuple data
0DAH	21h	Vcc Selection Byte	Tuple data
0DCH	b5h	Nom V Parameter	Tuple data
0DEH	1eh	Nom V Parameter	Tuple data
0E0H	4dh	Peak I Parameter	Tuple data
0E2H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
0E4H	0fh	TPL_LINK	Tuple link
0E6H	c2h	Configuration Index Byte	Tuple data
0E8H	41h	Interface Descriptor	Tuple data
0EAH	99h	Feature Select	Tuple data
0ECH	01h	Vcc Selection Byte	Tuple data
0EEH	55h	Nom V Parameter	Tuple data
0F0H	eah	I/O param	Tuple data
0F2H	61h	I/O range length and size	Tuple data
0F4H	f0h	Base address	Tuple data
0F6H	01h	Base address	Tuple data
0F8H	07h	Address length	Tuple data
0FAH	f6h	Base address	Tuple data
0FCH	03h	Base address	Tuple data

0FEH	01h	Address length	Tuple data
100H	eeh	IRQ parameter	Tuple data
102H	20h	Misc features	Tuple data
104H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
106H	06h	TPL_LINK	Tuple link
108H	02h	Configuration Index Byte	Tuple data
10AH	01h	Feature Select	Tuple data
10CH	21h	Vcc Selection Byte	Tuple data
10EH	b5h	Nom V Parameter	Tuple data
110H	1eh	Nom V Parameter	Tuple data
112H	4dh	Peak I Parameter	Tuple data
114H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
116H	0fh	TPL_LINK	Tuple link
118H	c3h	Configuration Index Byte	Tuple data
11AH	41h	Interface Descriptor	Tuple data
11CH	99h	Feature Select	Tuple data
11EH	01h	Vcc Selection Byte	Tuple data
120H	55h	Nom V Parameter	Tuple data
122H	eah	I/O param	Tuple data
124H	61h	I/O range length and size	Tuple data
126H	70h	Base address	Tuple data
128H	01h	Base address	Tuple data
12AH	07h	Address length	Tuple data
12CH	76h	Base address	Tuple data
12EH	03h	Base address	Tuple data
130H	01h	Address length	Tuple data
132H	eeh	IRQ parameter	Tuple data
134H	20h	Misc features	Tuple data
136H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
138H	06h	TPL_LINK	Tuple link
13AH	03h	Configuration Index Byte	Tuple data
13CH	01h	Feature Select	Tuple data
13EH	21h	Vcc Selection Byte	Tuple data
140H	b5h	Nom V Parameter	Tuple data
142H	1eh	Nom V Parameter	Tuple data
144H	4dh	Peak I Parameter	Tuple data
146H	14h	CISTPL_NO_LINK	Tuple code
148H	00h	TPL_LINK	Tuple link
14AH	ffh	CISTPL_END	End of Tuple

Task File register specification

These registers are used for reading and writing the storage data in this card. These registers are mapped five types by the configuration of INDEX in Configuration Option register. The decoded addresses are shown as follows.

Memory map (INDEX=0)

-REG	A10	A9 to A4	A3	A2	A1	A0	Offset	-OE=L	-WE=L
1	0	x	0	0	0	0	0H	Data register	Data register
1	0	x	0	0	0	1	1H	Error register	Feature register
1	0	x	0	0	1	0	2H	Sector count register	Sector count register
1	0	x	0	0	1	1	3H	Sector number register	Sector number register
1	0	x	0	1	0	0	4H	Cylinder low register	Cylinder low register
1	0	x	0	1	0	1	5H	Cylinder high register	Cylinder high register
1	0	x	0	1	1	0	6H	Drive head register	Drive head register
1	0	x	0	1	1	1	7H	Status register	Command register
1	0	x	1	0	0	0	8H	Dup. even data register	Dup. even data register
1	0	x	1	0	0	1	9H	Dup. odd data register	Dup. odd data register
1	0	x	1	1	0	1	DH	Dup. error register	Dup. feature register
1	0	x	1	1	1	0	EH	Alt. status register	Device control register
1	0	x	1	1	1	1	FH	Drive address register	Reserved
1	1	x	x	x	x	0	8H	Even data register	Even data register
1	1	x	x	x	x	1	9H	Odd data register	Odd data register

Contiguous I/O map (INDEX=1)

-REG	A10 to A4	A3	A2	A1	A0	Offset	-IORD=L	-IOWR=L
0	x	0	0	0	0	0H	Data register	Data register
0	x	0	0	0	1	1H	Error register	Feature register
0	x	0	0	1	0	2H	Sector count register	Sector count register
0	x	0	0	1	1	3H	Sector number register	Sector number register
0	x	0	1	0	0	4H	Cylinder low register	Cylinder low register
0	x	0	1	0	1	5H	Cylinder high register	Cylinder high register
0	x	0	1	1	0	6H	Drive head register	Drive head register
0	x	0	1	1	1	7H	Status register	Command register
0	x	1	0	0	0	8H	Dup. even data register	Dup. even data register
0	x	1	0	0	1	9H	Dup. odd data register	Dup. odd data register
0	x	1	1	0	1	DH	Dup. error register	Dup. feature register
0	x	1	1	1	0	EH	Alt. status register	Device control register
0	x	1	1	1	1	FH	Drive address register	Reserved

Primary I/O map (INDEX=2)

-REG	A10	A9 to A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0	x	1FH	0	0	0	0	Data register	Data register
0	x	1FH	0	0	0	1	Error register	Feature register
0	x	1FH	0	0	1	0	Sector count register	Sector count register
0	x	1FH	0	0	1	1	Sector number register	Sector number register
0	x	1FH	0	1	0	0	Cylinder low register	Cylinder low register
0	x	1FH	0	1	0	1	Cylinder high register	Cylinder high register
0	x	1FH	0	1	1	0	Drive head register	Drive head register
0	x	1FH	0	1	1	1	Status register	Command register
0	x	3FH	0	1	1	0	Alt. status register	Device control register
0	x	3FH	0	1	1	1	Drive address register	Reserved

Secondary I/O map (INDEX=3)

-REG	A10	A9 to A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0	x	17FH	0	0	0	0	Data register	Data register
0	x	17FH	0	0	0	1	Error register	Feature register
0	x	17FH	0	0	1	0	Sector count register	Sector count register
0	x	17FH	0	0	1	1	Sector number register	Sector number register
0	x	17FH	0	1	0	0	Cylinder low register	Cylinder low register
0	x	17FH	0	1	0	1	Cylinder high register	Cylinder high register
0	x	17FH	0	1	1	0	Drive head register	Drive head register
0	x	17FH	0	1	1	1	Status register	Command register
0	x	37FH	0	1	1	0	Alt. status register	Device control register
0	x	37FH	0	1	1	1	Drive address register	Reserved

True IDE Mode I/O map

-CE2	-CE1	A2	A1	A0	-IORD=L	-IOWR=L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder low register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Drive head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. status register	Device control register
0	1	1	1	1	Drive address register	Reserved

1.Data register: This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

2.Error register: This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to "0"(Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	"0"	IDNF	"0"	ABRT	"0"	AMNF

bit	Name	Function
7	BBK(Bad Block detected)	This bit is set when a Bad Block is detected in requester ID field.
6	UNC(Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF(ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT(ABoRTed command)	This bit is set if the command has been aborted because of the card status condition.(Not ready, Write fault, Invalid command, etc.)
0	AMNF(Address Mark Not Found)	This bit is set in case of a general error.

3.Feature register: This register is write-only register, and provides information regarding features of the drive that the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature byte							

5. **Sector count register:** This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete, the request.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

5.Sector number register: This register contains the starting sector number, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number byte							

6.Cylinder low register: This register contains the low 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low byte							

7.Cylinder high register: This register contains the high 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high byte							

8.Drive head register: This register is used for selecting the Drive number and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	LBA	1	DRV	Head number			

bit	Name	Function
7	1	This bit is set to "1".
6	LBA	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA =0, CHS mode is selected. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07-LBA00 : Sector Number Register D7-D0. LBA15-LBA08 : Cylinder Low Register D7-D0. LBA23-LBA16 : Cylinder High Register D7-D0. LBA27-LBA24 : Drive / Head Register bits HS3-HS0.
5	1	This bit is set to "1".
4	DRV(DriVe select)	This bit is used for selecting the Master (Card 0)and Slave(Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.
3	Head number	This bit is used for selecting the Head number for the following command. Bit 3 is MSB.

9.Status register: This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX=1,2,3) and level interrupt mode, –IREQ is negated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY(BuSY)	This bit is set when the card internal operation is executing. When this bit is set to "1", other bits in this register are invalid.
6	DRVY(Drive ReaDY)	If this bit and DSC bit are set to "1", the card is capable of receiving the read or write or seek requests. If this bit is set to "0", the card prohibits these requests.
5	DWF(Drive Write Fault)	This bit is set if this card indicates the write fault status.
4	DSC(Drive Seek Complete)	This bit is set when the drive seeks complete.
3	DRQ(Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR(CORRected data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX(InDeX)	This bit is always set to "0".
0	ERR(ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in this error register or other Status registers. This bit is cleared by the next command.

10.Alternate status register: This register is the same as Status register in physically, so the bit assignment refers to previous item of Status register. But this register is different from Status register that –IREQ is not negated when data read.

11.Command register: This register is write only register, and it is used for writing the command to execute the requested operation. The command codes is written in the command register, after the parameter is written in the Task File when the card is in Ready state.

		Used parameter						
Command	**Command code**	**FR**	**SC**	**SN**	**CY**	**DR**	**HD**	**LBA**
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
Erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1H or 95H	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40H or 41H	N	Y	Y	Y	Y	Y	Y
Recalibrate	1XH	N	N	N	N	Y	N	N
Request sense	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Set sleep mode	E6H or 99H	N	N	N	N	Y	N	N
Stand by	E2H or 96H	N	N	N	N	Y	N	N
Stand by immediate	E0H or 94H	N	N	N	N	Y	N	N
Translate sector	87H	N	Y	Y	Y	Y	Y	Y
Wear level	F5H	N	N	N	N	Y	Y	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32H or 33H	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

Note: FR: Feature register
SC: Sector Count register
SN: Sector Number register
CY: Cylinder register
DR: DRV bit of Drive Head register
HD: Head Number of Drive Head register
LBA: Logical Block Address Mode Supported
Y: The register contains a valid parameter for this command
N: The register does not contain a valid parameter for this command

12. Device control register: This register is write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	x	1	SRST	nIEN	0

bit	Name	Function
7to 4	X	don't care
3	1	This bit is set to "1".
2	SRST(Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0".
1	nIEN(Interrupt Enable)	This bit is used for enabling –IREQ. When this bit is set to "0", –IREQ is enabled. When this bit is set to "1", –IREQ is disabled.
0	0	This bit is set to "0".

13.Drive Address register: This register is read only register, and it is used for confirming the drive status. This register is provides for compatibility with the AT disk drive interface. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on bit7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

bit	Name	Function
7	X	This bit is unknown.
6	nWTG(WriTing Gate)	This bit is unknown.
5 to 2	nHS3-0(Head Select3-0)	These bits is the negative value of Head Select bits(bit 3 to 0)in Drive/Head register.
1	nDS1(Idrive Select1)	This bit is unknown.
0	nDS0(Idrive Select0)	This bit is unknown.

ATA Command specifications

This table summarizes the ATA command set with the paragraphs. Following shows the supported commands and command codes, which are written in command registers.

ATA Command Set

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LSB
1	Check power mode	E5H or 98H	—	—	—	—	Y	—	—
2	Execute drive diagnostic	90H	—	—	—	—	Y	—	—
3	Erase sector(s)	C0H	—	Y	Y	Y	Y	Y	Y
4	Format track	50H	—	Y	—	Y	Y	Y	Y
5	Identify Drive	ECH	—	—	—	—	Y	—	—
6	Idle	E3H or 97H	—	Y	—	—	Y	—	—
7	Idle immediate	E1H or 95H	—	—	—	—	Y	—	—
8	Initialize drive parameters	91H	—	Y	—	—	Y	Y	—
9	Read buffer	E4H	—	—	—	—	Y	—	—
10	Read multiple	C4H	—	Y	Y	Y	Y	Y	Y
11	Read long sector	22H,23H	—	—	Y	Y	Y	Y	Y
12	Read sector(s)	20H,21H	—	Y	Y	Y	Y	Y	Y
13	Read verify sector(s)	40H, 41H	—	Y	Y	Y	Y	Y	Y
14	Recalibrate	1XH	—	—	—	—	Y	—	—
15	Request sense	03H	—	—	—	—	Y	—	—
16	Seek	7XH	—	—	Y	Y	Y	Y	Y
17	Set features	EFH	Y	—	—	—	Y	—	—
18	Set multiple mode	C6H	—	Y	—	—	Y	—	—
19	Set sleep mode	E6H or 99H	—	—	—	—	Y	—	—
20	Stand by	E2H or 96H	—	—	—	—	Y	—	—
21	Stand by immediate	E0H or 94H	—	—	—	—	Y	—	—
22	Translate sector	87H	—	Y	Y	Y	Y	Y	Y
23	Wear level	F5H	—	—	—	—	Y	Y	—
24	Write buffer	E8H	—	—	—	—	Y	—	—
25	Write long sector	32H or 33H	—	—	Y	Y	Y	Y	Y
26	Write multiple	C5H	—	Y	Y	Y	Y	Y	Y
27	Write multiple w/o erase	CDH	—	Y	Y	Y	Y	Y	Y
28	Write sector	30H or 31H	—	Y	Y	Y	Y	Y	Y
29	Write sector w/o erase	38H	—	Y	Y	Y	Y	Y	Y
30	Write verify	3CH	—	Y	Y	Y	Y	Y	Y

Note: FR: Feature Register
SC: Sector Count register (00H to FFH)
SN: Sector Number register (01H to 20H)
CY: Cylinder Low/High register
DR: Drive bit of Drive/Head register
HD: Head No.(0 to 3) of Drive/Head register
Y: Set up
－: Not set up

1. Check Power Mode (code: E5H or 98H): This command checks the power mode.
2. Execute Drive Diagnostic (code: 90H): This command performs the internal diagnostic tests implemented by the Card.
3. Erase Sector(s)(code: C0H): This command is used to erase data sectors.
4. Format Track (code: 50H): This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFH or 00H). To remain host backward compatible, the card expects one sector (512Bytes) of data from the host to follow the command with same protocol as the Write Sector Command.
5. Identify Drive (code: ECH): This command enables the host to receive parameter information from the Card.

Identify Drive Information

Word address	Default value	Total bytes	Data field type information
0	848AH	2	General configuration bit-significant information
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	XXXX	2	Number of unformatted bytes per sector
6	XXXX	2	Default number of sectors per track
7 to 8	XXXX	4	Number of sectors per card(Word7=MSW,Words=LSW)
9	0000H	2	Reserved
10 to 19	XXXX	20	Serial number in ASCII
20	0001H	2	Buffer type(single ported)
21	0004H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23 to 46	XXXX	48	Firmware revision in ASCII etc.
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0200H	2	Capabilities: DMA NOT Supported(bit 8), LBA supported
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	DMA data transfer cycle timing mode not Supported
53 to 58	XXXX	12	Reserved
59	0101H	2	Multiple sector setting is valid
60 to 61	XXXX	4	Total number of sectors addressable in LBA Mode
62 to 255	0000H	388	Reserved

6.Idle (code: E3H or 97H): This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

7.Idle Immediate (code: E1H or 95H): This command causes the Card to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

8.Initialize Drive Parameters (code: 91H): This command enables the host to set the number of sectors per track and the number of heads per cylinder.

9.Read Buffer (code: E4H): This command enables the host to read the current contents of the card's sector buffer.

10. Read Multiple (code: C4H): This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
11. Read Long Sector (code 22H or 23H): This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.
12. Read Sector(s) (code 20H, 21H): This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.
13. Read Verify Sector(s) (code: 40H or 41H): This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.
14. Recalibrate (code: 1XH): This command is effectively a NOP command to the Card and is provided for compatibility purposes.
15. Request Sense (code: 03H): This command requests an extended error code after command ends with an error.
16. Seek (code: 7XH): This command is effectively a NOP command to the Card although it does perform a range check.
17. Set Features (code: EFH): This command is used by the host to establish or select certain features.

Feature	Operation
01H	Enable 8-bit data transfers.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
81H	Disable 8-bit data transfers.
BBH	4 bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

18. Set Multiple Mode (code: C6H): This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands.
19. Set Sleep Mode (code: E6H or 99H): This command causes the Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.
20. Stand By (code: E2H or 96H): This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
21. Stand By Immediate (code: E0H or 94H): This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
22. Translate Sector (code: 87H): This command allows the host a method of determining the exact number of times a use sector has been erased and programmed.

23. Wear Level (code: F5H): This command effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 00H indicating Wear Level is not needed.

24. Write Buffer (code: E8H): This command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired.

25. Write Long Sector (code: 32H or 33H): This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.

26. Write Multiple (code: C5H): This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

27. Write Multiple without Erase (code: CDH): This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed.

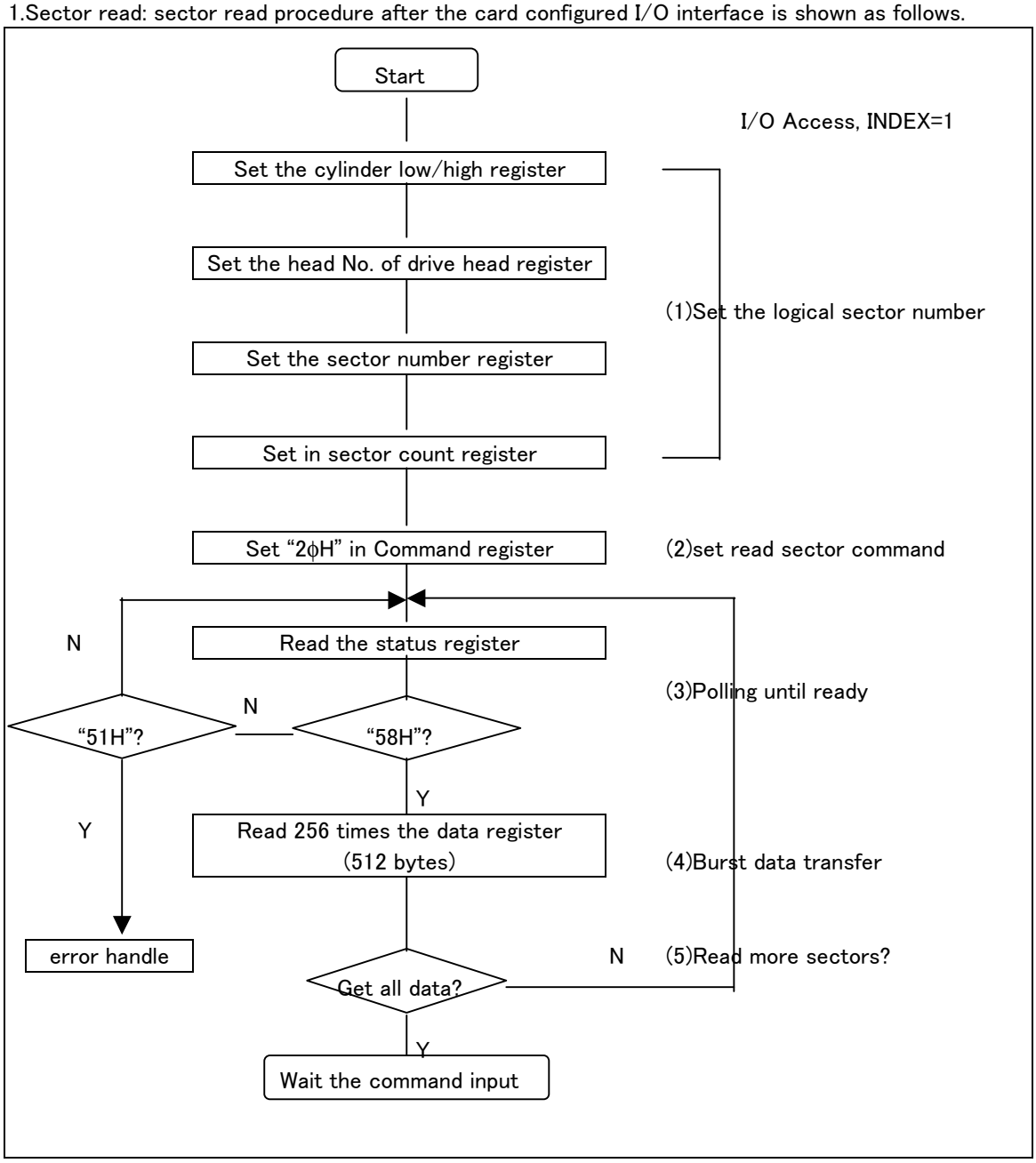
28. Write Sector(s): (code: 30H or 31H): This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

29. Write Sector(s) without Erase (code: 38H): This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.

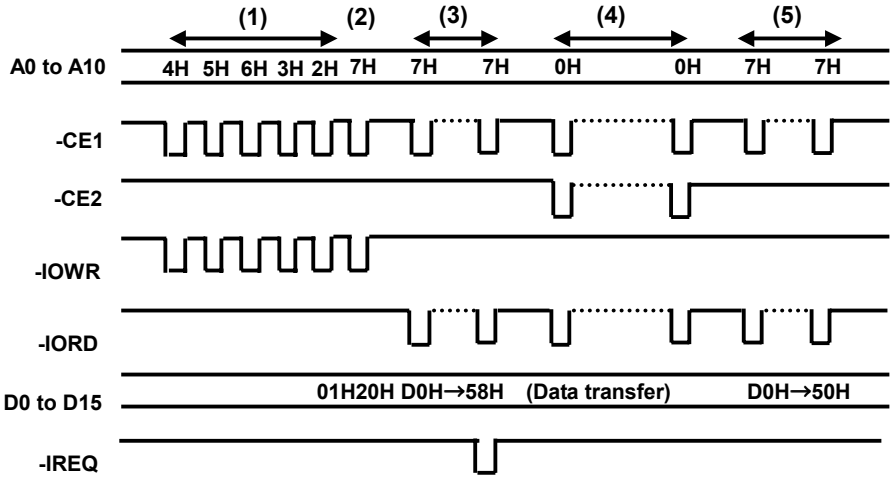
30. Write Verify (code: 3CH): This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

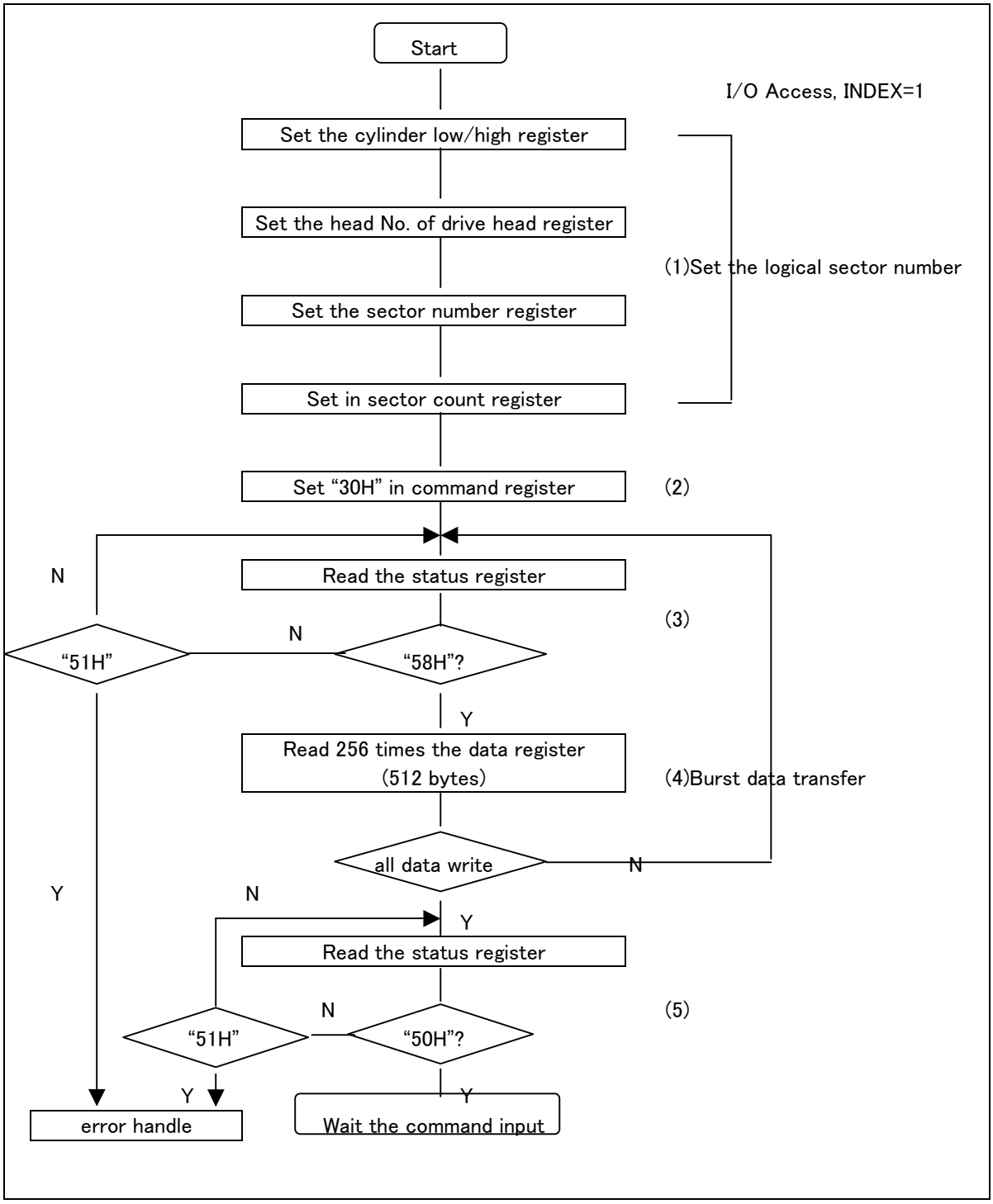
Sector Transfer Protocol

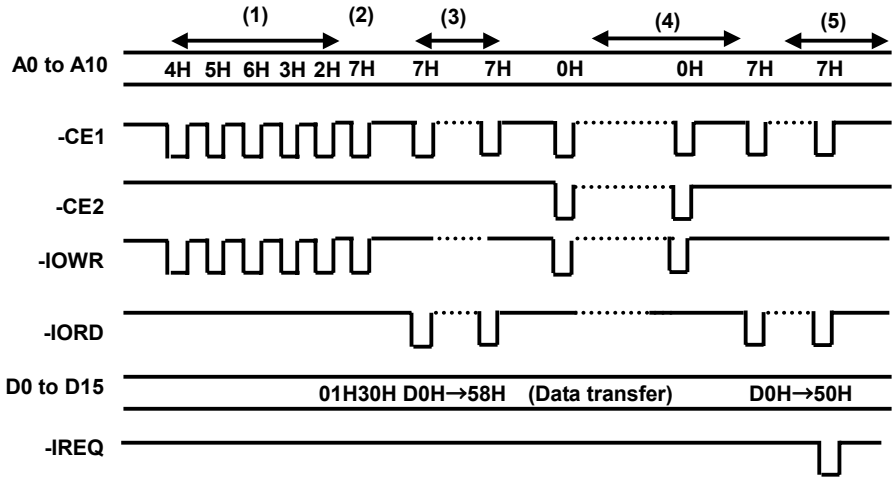
1.Sector read: sector read procedure after the card configured I/O interface is shown as follows.



2.Sector write: write sector procedure after the card configured I/O interface is shown as follows.




Start
I/O Access, INDEX=1
Set the cylinder low/high register
Set the head No. of drive head register
(1)Set the logical sector number
Set the sector number register
Set in sector count register
Set "30H" in command register
(2)
Read the status register
N
(3)
"51H"
N
"58H"?
Y
Read 256 times the data register
(512 bytes)
(4)Burst data transfer
all data write
N
Y
N
Y
Read the status register
N
(5)
"51H"
"50H"?
Y
Y
error handle
Wait the command input



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
All input/output voltages	Vin, Vout	−0.3 to V_{CC} +0.3	V	1
V_{CC} voltage	V_{CC}	−0.3 to +6.7	V	
Operation temperature range	Topr	0 to +85	°C	
Storage temperature range	Tstg	−55 to +125	°C	

Note: 1. Vin, Vout min=−2.0 V for pulse width ≦20ns.

Recommended Operation Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operation temperature	Ta	0	25	60	°C
V_{CC} voltage	V_{CC}	4.5	5.0	5.5	V
		3.15	3.3	3.45	V

Capacitance (Ta=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	15	pF	Vin=0V	1
Output capacitance	Count	—	—	15	pF	Vout=0V	1

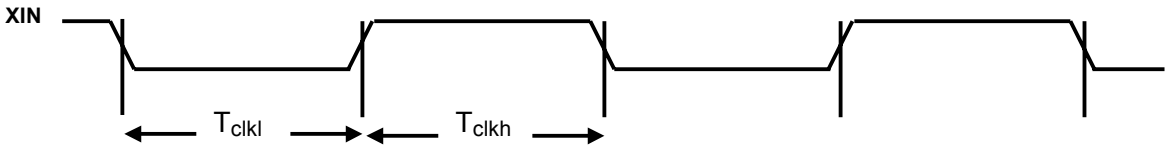
Note: 1. This parameter is sampled and not 100% tested.

Card System performance

Item	Performance
Set up times (Reset to ready)	500 ms (max)
Set up times (Sleep to idle)	100 μs (max)
Set up times (Deep power down to idle)	4 ms (max)
Data transfer rate to/from host	16 Mbyte/s burst (max), theoretically
Sustained read transfer rate	5.4Mbyte/s (max), actually
Sustained write transfer rate	3.2Mbyte/s (max), actually
Controller overhead (Command to DRQ)	4 ms (max)
Data transfer cycle end to ready(Sector write)	500 μs (typ), 50 ms (max)

DC Characteristics-1 (Ta=0 to +70° C, V_{CC} = 3.3V±5%, 5V±10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage	V_{IH}	2.0	—	V_{CC}+0.3	V	—
	V_{IL}	−0.3	—	0.6	V	
Schmitt circuit	V_{T+}	—	2.1	—	V	V_{CC}=3.3V
	V_{T-}	—	1.2	—	V	
Output voltage (4mA)	V_{OH}	2.4	—	—	V	I_{OH}=−4mA
	V_{OL}	—	—	0.4	V	I_{OL}=4mA
Input leakage current	I_{LI}	—	—	1	μA	—
Output leakage current	I_{LO}	—	—	1	μA	V_{OUT}=high impedance
Pull-up current (Resistivity)	$-I_{PU}$	20/(165)	45/(73)	72/(45)	μA(kΩ)	V_{Force}=3.3V
Pull-down current (Resistivity)	$-I_{PD}$	−20/(1800)	−48/(206)	−72/(85)	μA(kΩ)	V_{Force}=0V
Sleep/standby current	I_{SP1}	—	(0.2)	(0.5)	MA	CMOS level (control signal=V_{CC}−0.2)
Sector read current	I_{CCR}(DC)	—	(25)	(50)	MA	CMOS level (control signal=V_{CC}−0.2)
	I_{CCR}(Peak)	—	(50)	(80)	MA	
Sector write current	I_{CCW}(DC)	—	(25)	(50)	MA	CMOS level (control signal=V_{CC}−0.2)
	I_{CCW}(Peak)	—	(50)	(80)	MA	



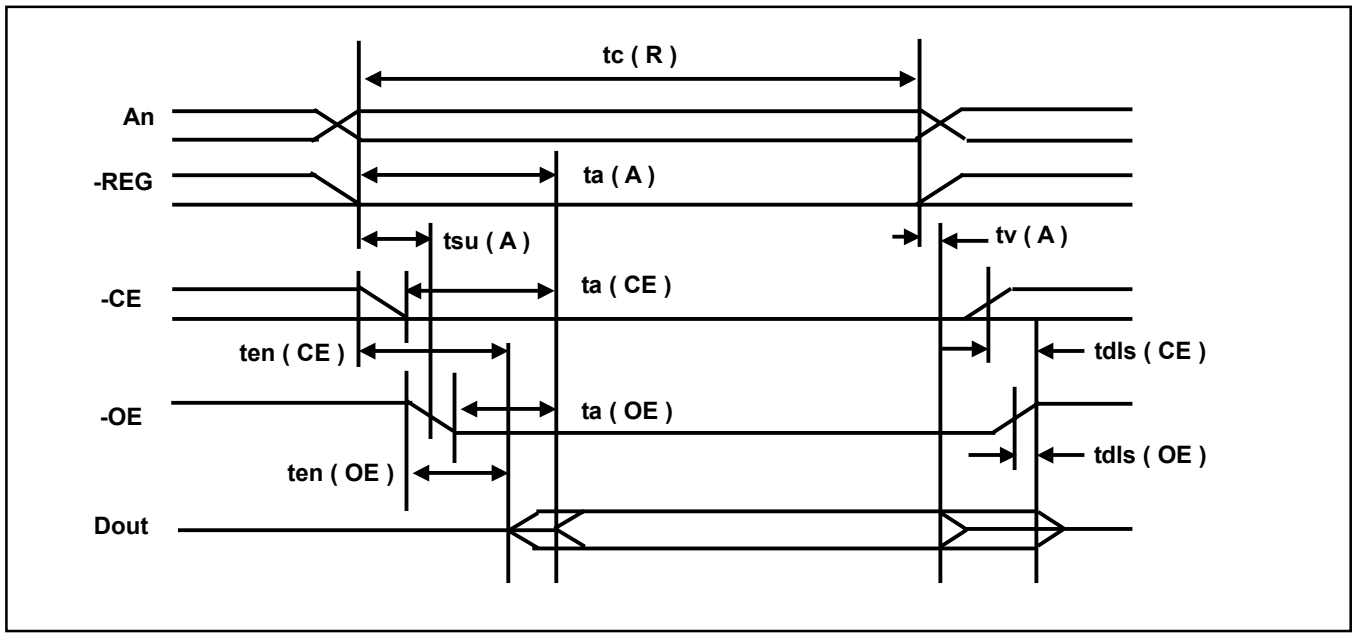
Symbol	Parameter	Min	Max
Tclkl	clock LOW time	20	
Tclkh	clock HIGH time	20	

AC Characteristics (Ta=0 to +60°C, V_{CC} = 5V±10%, V_{CC} = 3.3V±5%)

Attribute Memory Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	Tcr	100	—	—	ns
Address access time	ta(A)	—	—	100	ns
−CE access time	ta(CE)	—	—	100	ns
−OE access time	ta(OE)	—	—	50	ns
Output disable time(−CE)	tdis(CE)	—	—	40	ns
Output disable time(−OE)	tdis(OE)	—	—	40	ns
Output enable time(−CE)	ten(CE)	5	—	—	ns
Output enable time(−OE)	ten(OE)	5	—	—	ns
Data valid time(A)	tv(A)	0	—	—	ns
Address setup time	tsu(A)	30	—	—	ns

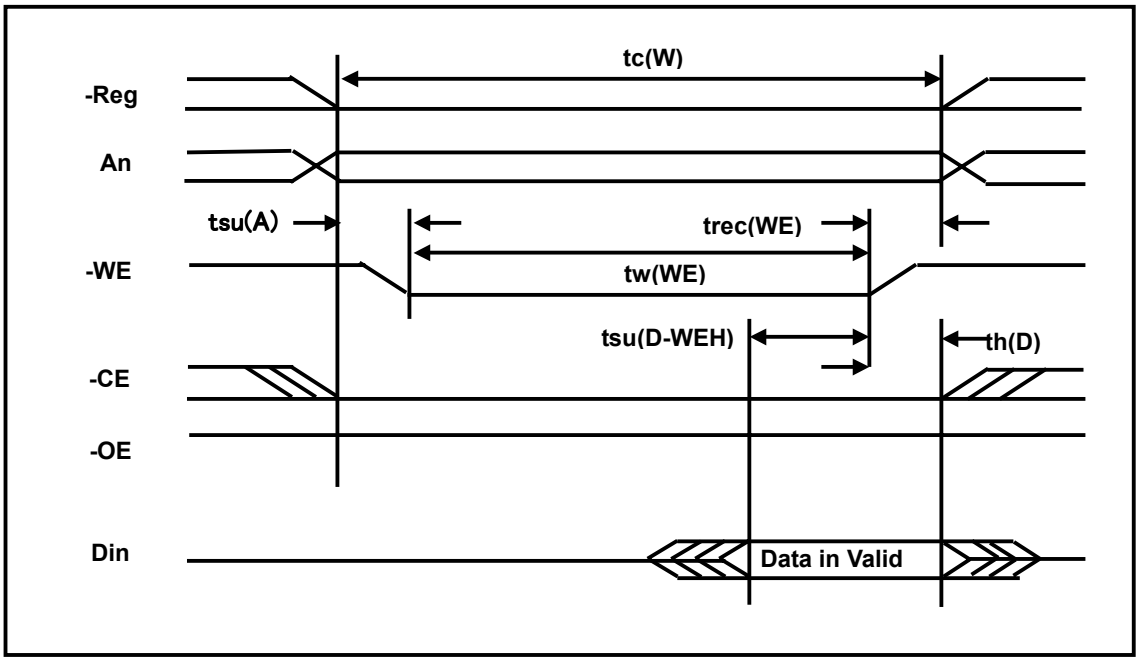
Attribute Memory Read Timing



Attribute Memory Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	tCW	100	—	—	ns
Write pulse time	tw(WE)	60	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
Data setup time (−WE)	tsu(D−WEH)	40	—	—	ns
Data hold time	th(D)	30	—	—	ns
Write recover time	trec(WE)	20	—	—	ns

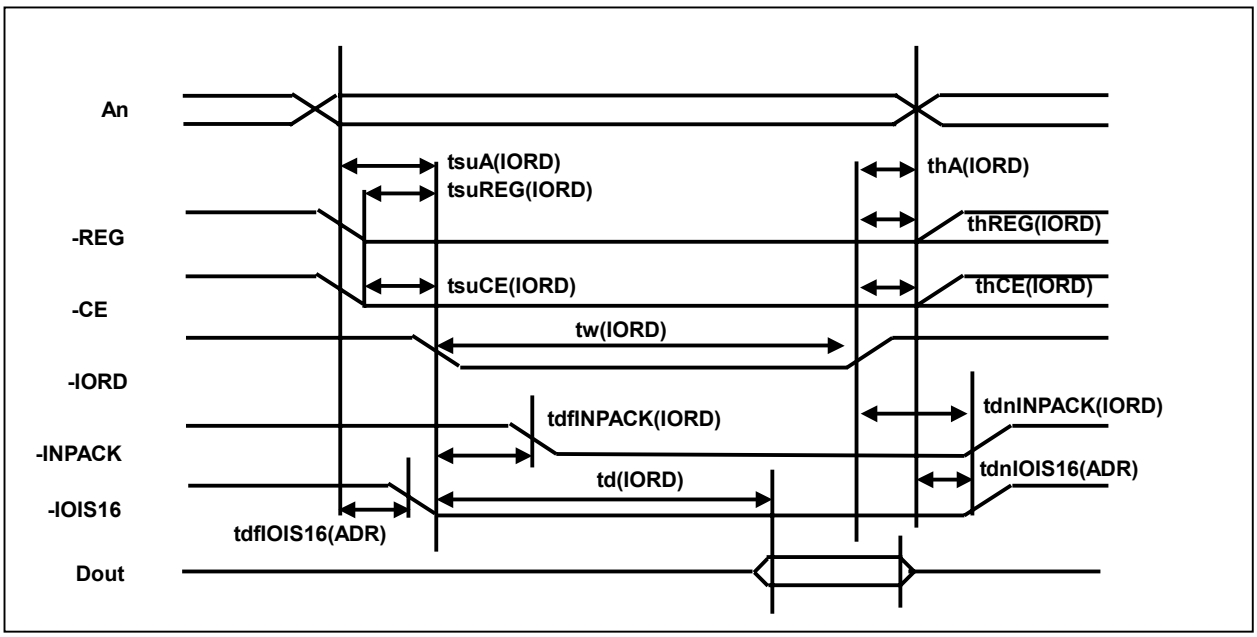
Attribute Memory Write Timing



I/O Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data delay after –IORD	td(IORD)	—	—	45	ns
Data hold following –IORD	th(IORD)	0	—	—	ns
–IORD pulse width	tw(IORD)	80	—	—	ns
Address setup before –IORD	tsuA(IORD)	30	—	—	ns
Address hold following –IORD	thA(IORD)	20	—	—	ns
–CE setup before –IORD	tsuCE(IORD)	0	—	—	ns
–CE hold following –IORD	thCE(IORD)	0	—	—	ns
–REG setup before –IORD	tsuREG(IORD)	0	—	—	ns
–REG hold following –IORD	thREG(IORD)	0	—	—	ns
–INPACK delay failing from –IORD	tdfINPACK(IORD)	0	—	45	ns
–INPACK delay rising from –IORD	tdrINPACK(IORD)	—	—	45	ns
–IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
–IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

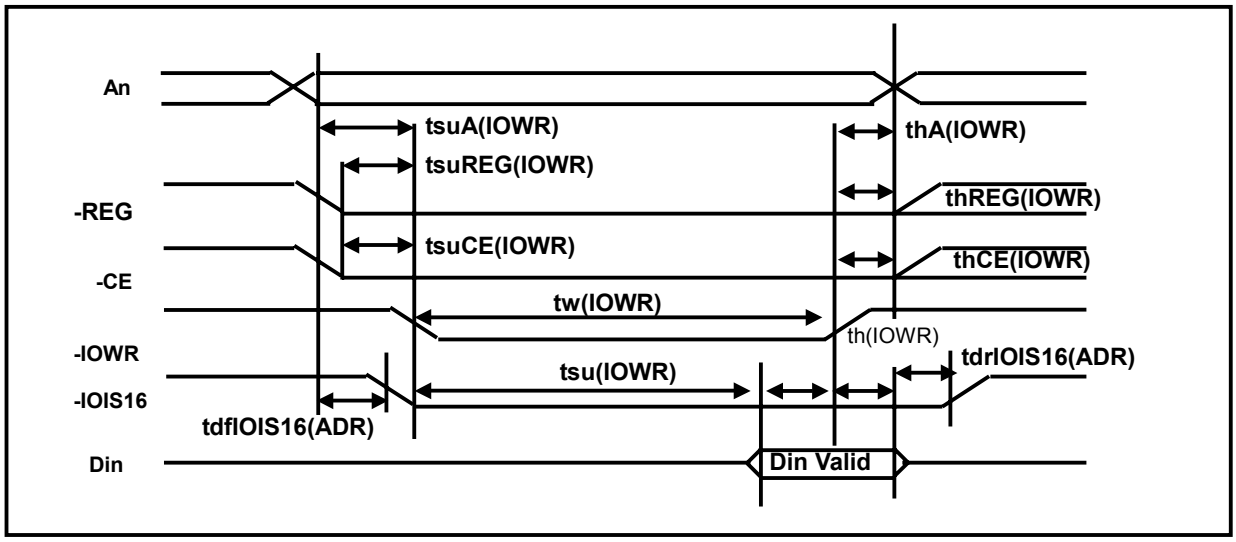
I/O Access Read Timing+



I/O Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before –IOWR	tsu(IOWR)	40	—	—	ns
Data hold following –IOWR	th(IOWR)	30	—	—	ns
–IOWR pulse width	tw(IOWR)	80	—	—	ns
Address setup before –IOWR	tsuA(IOWR)	30	—	—	ns
Address hold following –IOWR	thA(IOWR)	20	—	—	ns
–CE setup before –IOWR	tsuCE(IOWR)	0	—	—	ns
–CE hold following –IOWR	thCE(IOWR)	0	—	—	ns
–REG setup before –IOWR	tsuREG(IOWR)	0	—	—	ns
–REG hold following –IOWR	thREG(IOWR)	0	—	—	ns
–IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
–IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

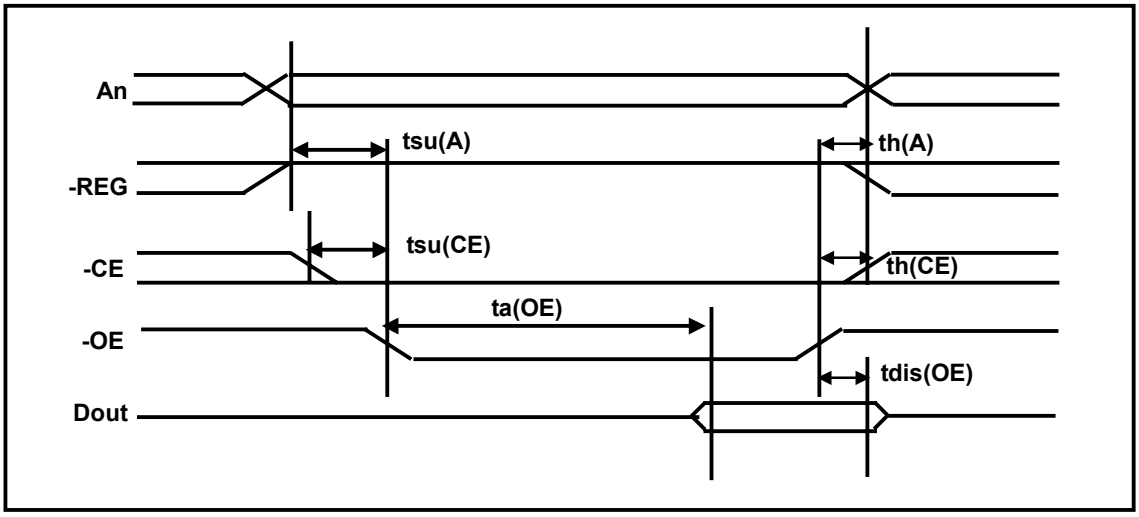
I/O Access Write Timing



Command Memory Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
−OE access time	ta(OE)	—	—	60	ns
Output disable time (−OE)	tdis(OE)	—	—	40	ns
Address setup time	tsu(A)	30	—	—	ns
Address hold time	th(A)	20	—	—	ns
−CE setup time	tsu(CE)	0	—	—	ns
−CE hold time	th(CE)	0	—	—	ns

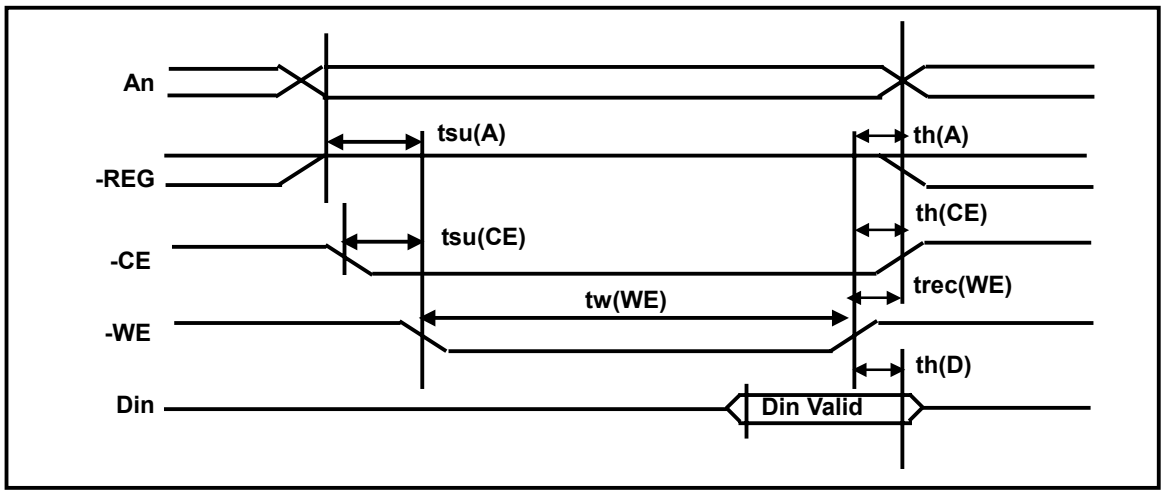
Common Memory Access Read Timing



Common Memory Access Write AC Characteristic

Parameter	Symbol	Min	Typ	Max	Unit
Data setup time (−WE)	tsu(D−WEH)	40	—	—	ns
Data hold time	th(D)	30	—	—	ns
Write pulse time	tw(WE)	80	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
−CE setup time	tsu(CE)	0	—	—	ns
Write recover time	trec(WE)	20	—	—	ns
−CE hold following −WE	th(CE)	0	—	—	ns

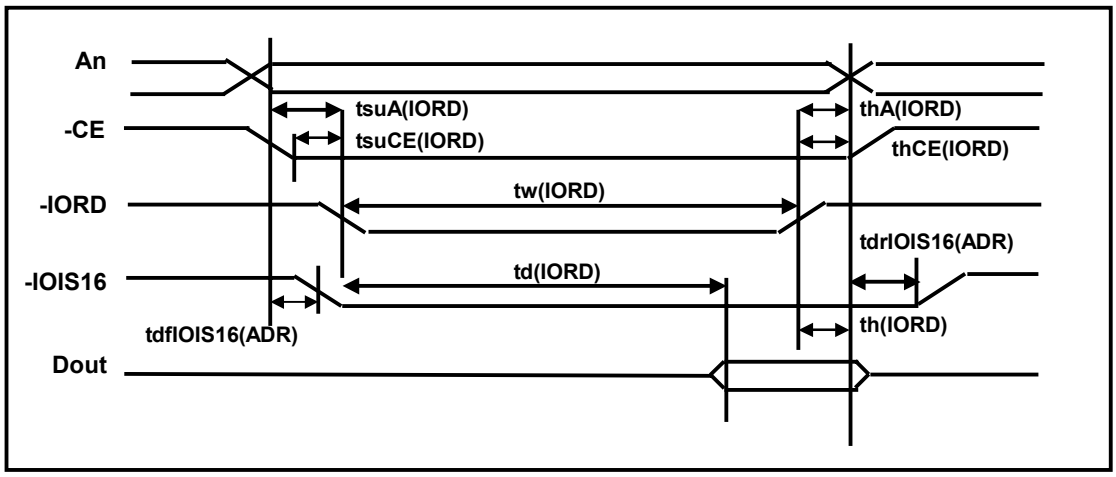
Common Memory Access Write Timing



The IDE Mode Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data delay after IORD	td(IORD)	—	—	45	ns
Data hold following IORD	th(IORD)	0	—	—	ns
IORD with time	tw(IORD)	80	—	—	ns
Address setup before IORD	tsuA(IORD)	30	—	—	ns
Address hold following IORD	thA(IORD)	20	—	—	ns
CE setup before IORD	tsuCE(IORD)	0	—	—	ns
CE hold following IORD	thCE(IORD)	0	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tsfIOIS16(ADR)	—	—	35	ns

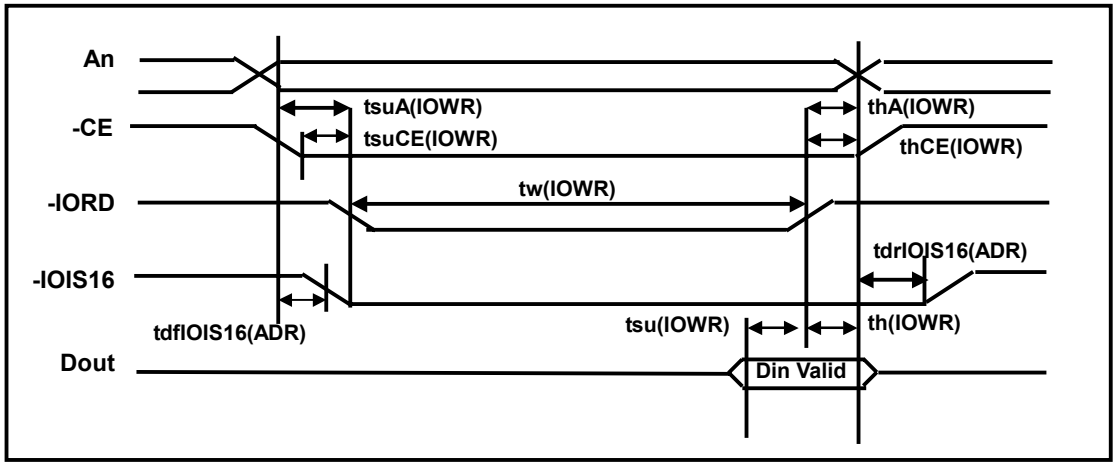
True IDE Mode Access Read Timing



True IDE Mode Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before IOWR	tsu(IOWR)	40	—	—	ns
Data hold following IOWR	th(IOWR)	30	—	—	ns
IORD width time	tw(IOWR)	80	—	—	ns
Address setup before IOWR	tsuA(IOWR)	30	—	—	ns
Address hold following IOWR	thA(IOWR)	20	—	—	ns
CE setup before IOWR	tsuCE(IOWR)	0	—	—	ns
CE hold following IOWR	thCE(IOWR)	0	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tsfIOIS16(ADR)	—	—	35	ns

True IDE Mode Access Write Timing

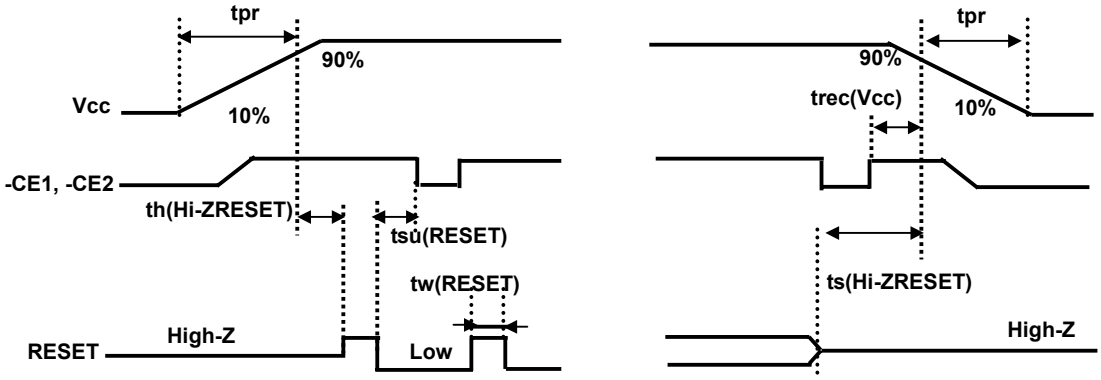


Reset Characteristics (only Memory Card Mode or I/O Card Mode)

Hard Reset Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reset setup time	tsu(RESET)	100	—	—	ms	
-CE recover time	trec(VCC)	1	—	—	μs	
VCC rising up time	tpr	0.1	—	100	ms	
VCC falling down time	tpf	3	—	300	ms	
Reset pulse width	tw(RESET)	10	—	—	μs	
	th(Hi-ZRESET)	1	—	—	ms	
	ts(Hi-ZRESET)	0	—	—	ms	

Hard Reset Timing

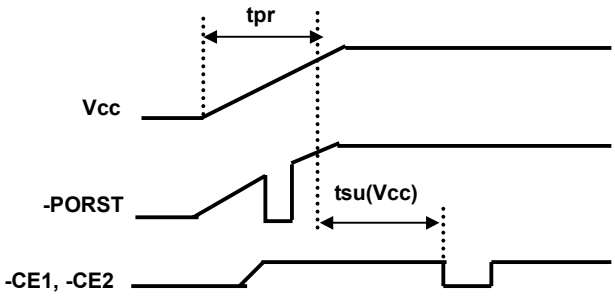


Power on Reset Characteristics

Power on reset sequence must need by –PORST at the rising of V_{CC}.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
–CE setup time	tsu(VCC)	100	—	—	ms	
VCC rising up time	tpr	0.1	—	100	ms	

Power on Reset Timing



Attention for Card Use

- In the reset or power off, the information of all registers is cleared.
- Notice that the card insertion/removal should not be executed during host is active, if the card is used in True IDE mode.
- After the card hard reset, soft reset, or power on reset, ATA reset, command applied the card cannot access during +RDY/–BSY pin is "low" level. Flash card can't be operated in this case.
- Before the card insertion V_{CC} can not be supplied to the card. After confirmation that –CD1, –CD2 pins are inserted, supply V_{CC} to the card.

Note:

–OE must be kept at the V_{CC} level during power on reset in memory card mode and I/O card mode. –OE must be kept constantly at the GND level in True IDE mode.