

HN624316N Series

Preliminary

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16M (1M x 16-bit) and (2M x 8-bit) Mask ROM

T-46-13-15

DESCRIPTION

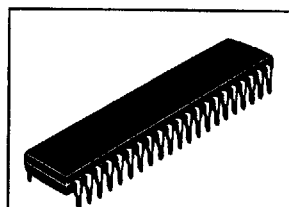
The Hitachi HN624316N is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 16-bit and 2,097,152 x 8-bit.

The high density and high speed Nibble Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN624316N is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP and 44-lead Plastic SOP packages. The HN624316N is also packaged in a 48-lead Plastic SOP.

FEATURES

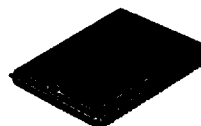
- Single Power Supply:
 $V_{CC} = 5 V \pm 10\%$
- Fast Access Times:
120 ns/150 ns (max)
- Nibble Access Times:
60 ns/70 ns (max)
- Low Power Consumption:
Active Current: 300 mW (typ)
Standby Current: 5 μ W (typ)
- User Selectable Organization:
1M x 16-bit (Word-Wide)
2M x 8-bit (Byte-Wide)
Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
42-pin Plastic DIP
44-lead Plastic SOP
48-lead Plastic SOP



(DP-42)



(FP-44D)



(FP-48DA)

ORDERING INFORMATION

Type No.	Access Time	Package
HN624316PN-12	120 ns	42-pin Plastic DIP
HN624316PN-15	150 ns	(DP-42)
HN624316FBN-12	120 ns	44-lead Plastic SOP
HN624316FBN-15	150 ns	(FP-44D)
HN624316FN-12	120 ns	48-lead Plastic SOP
HN624316FN-15	150 ns	(FP-48DA)

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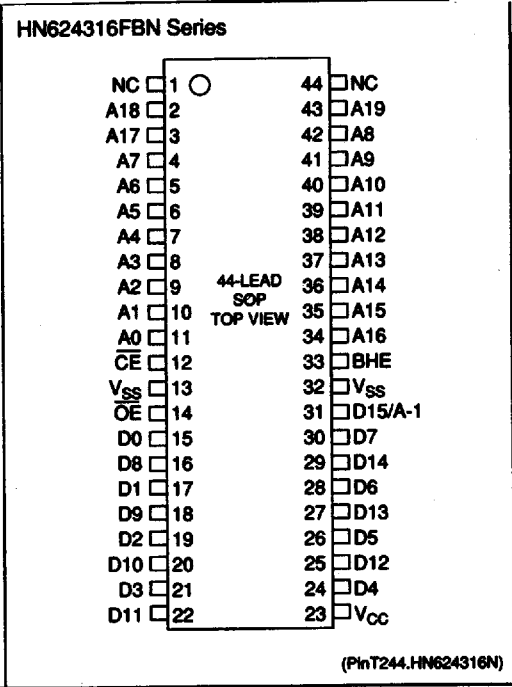
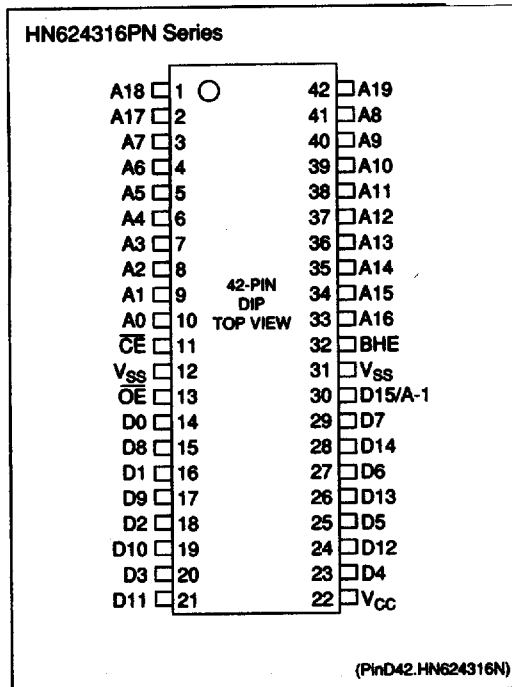
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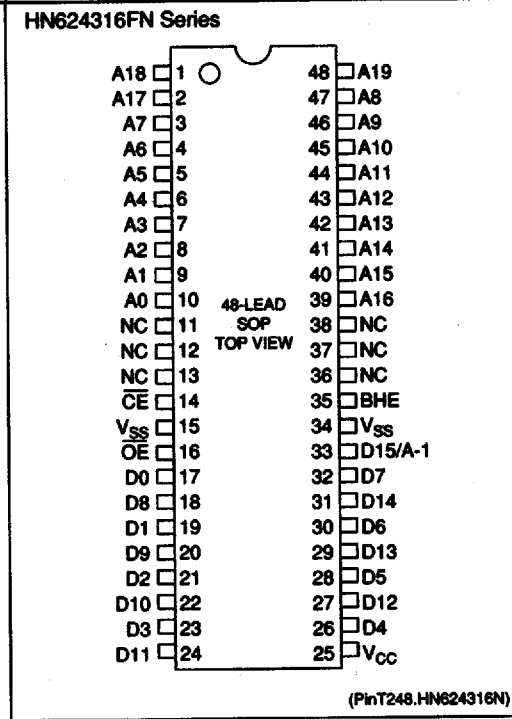
PIN ARRANGEMENT

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PIN DESCRIPTION

Pin Name	Function
A ₀ - A ₁₉	Address
A ₋₁	Address (Word-Wide)
D ₀ - D ₁₅	Output
CE	Chip Enable
OE	Output Enable
BHE	Byte Enable
V _{cc}	Power Supply
V _{ss}	Ground
NC	No Connection

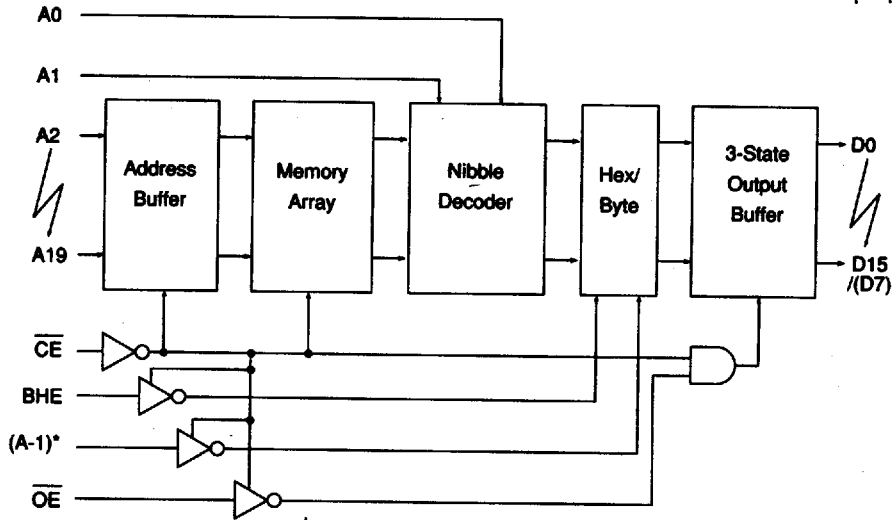


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■ BLOCK DIAGRAM

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(BD.HN624316N)

- Notes:
1. * : A₁ is the Least Significant Address bit in Byte-Wide Mode.
 2. BHE=V_{PH} : 16-bit (D₁₅ - D₀)
 BHE=V_L : 8-bit (D₇ - D₀)
 When BHE is low, D₁₄ - D₈ are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage ¹	V _{CC}	-0.3 to +7.0	V
All Input and Output Voltage ¹	V _{IN} , V _{OUT}	-0.3 to V _{CC} + 0.3	V
Operating Temperature Range	T _{OPR}	0 to +70	°C
Storage Temperature Range	T _{STG}	-55 to +125	°C
Temperature Under Bias	T _{BIAS}	-20 to +85	°C

Notes: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance ¹	C _{IN}	-	-	15	pF	V _{IN} = 0V
Output Capacitance ¹	C _{OUT}	-	-	15	pF	V _{OUT} = 0V

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I _{LI}	-	-	10	μA	V _{IN} = 0 V to V _{CC}
Output Leakage Current	I _{LO}	-	-	10	μA	$\overline{CE} = 2.2 V$, V _{OUT} = 0 V to V _{CC}
Operating V _{CC} Current	I _{CC}	-	-	75	mA	V _{CC} = 5.5 V, I _{OUT} = 0 mA, t _{RC} = 150ns
		-	-	65	mA	V _{CC} = 5.5 V, I _{OUT} = 0 mA, t _{RC} = 200
Standby V _{CC} Current	I _{SB}	-	-	30	μA	V _{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2V$
Input Voltage	V _{IH}	2.2	-	V _{CC} + 0.3	V	
	V _{IL}	-0.3	-	0.8	V	
Output Voltage	V _{OH}	2.4	-	-	V	I _{OH} = -205 μA
	V _{OL}	-	-	0.4	V	I _{OL} = 1.6 mA

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■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

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($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to $70^\circ C$)

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Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Reference level for measuring timing: 1.5 V

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Item	Symbol	HN624316N-12		HN624316N-15		Test Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150		ns
Nibble Read Cycle Time	t_{NC}	60	-	70	ns	
Address Access Time	t_{AA}	-	120	-	150	ns
Nibble Address Access Time	t_{NA}	-	120	-	70	ns
Chip Enable Access Time	t_{CE}	-	60	-	150	ns
Output Enable Access Time	t_{OE}	-	60	-	70	ns
BHE Access Time	t_{BHE}	-	120	-	150	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
Chip Enable to Output in High-Z ¹	t_{CHZ}	-	60	-	70	ns
Output Enable to Output in High-Z ¹	t_{OHZ}	-	60	-	70	ns
BHE to Output in High-Z ¹	t_{BHZ}	-	60	-	70	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ} , t_{OHZ} , t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

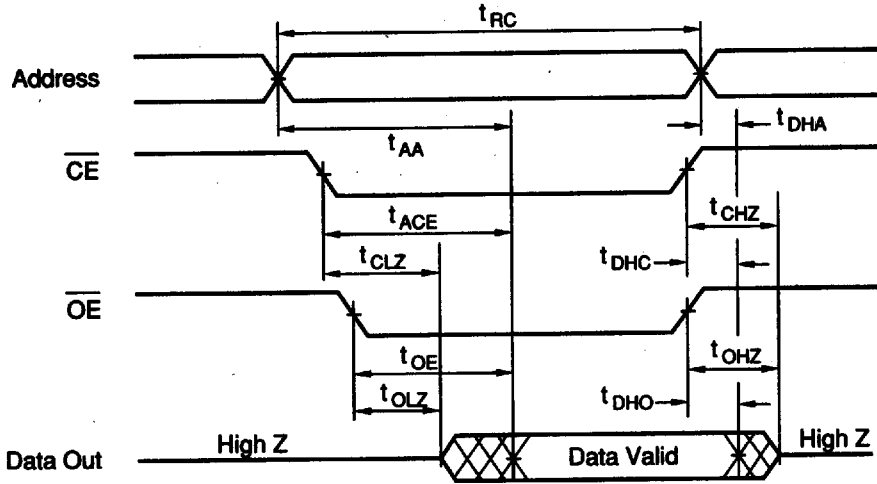


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■ READ TIMING WAVEFORM

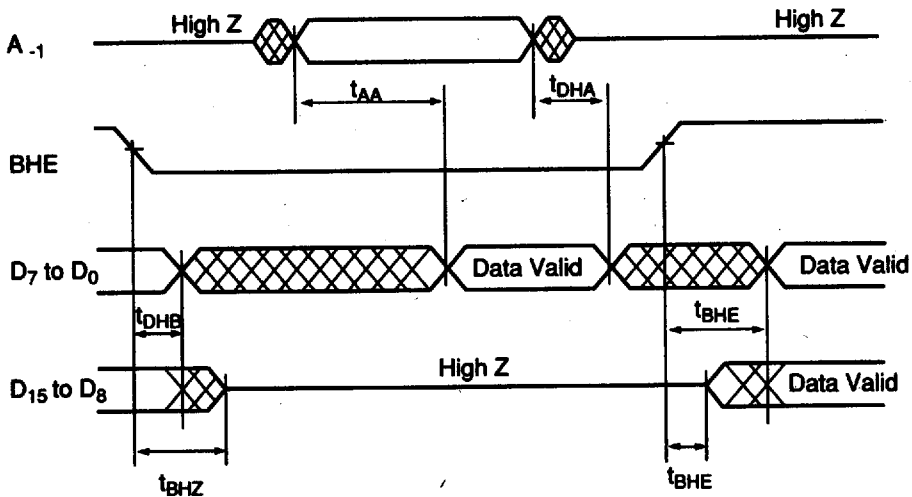
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})

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- Note:
1. t_{DHA} , t_{DHC} , t_{DHO} are determined by the faster time.
 2. t_{AA} , t_{ACE} , t_{OE} are determined by the slower time.
 3. t_{CLZ} , t_{OLZ} are determined by the slower time.
- (TD.R.HN624316N)

Word Mode/Byte Mode Switch

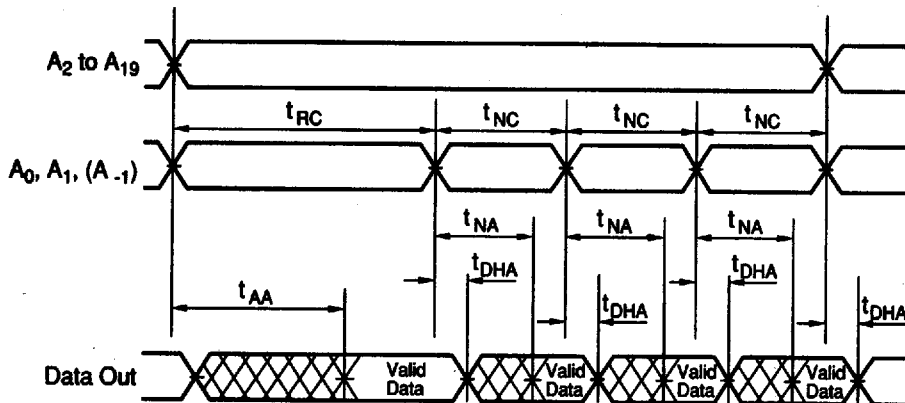


- Note:
1. If \overline{CE} and \overline{OE} are enabled, A_{10} to A_0 are valid.
 2. D_{15}/A_{10} pin is in the output state when BHE is high, \overline{CE} and \overline{OE} are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.
- (TD.R1.HN624316N)

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Nibble Mode

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(TD.RN.HN624316N)

Note: \overline{CE} and \overline{OE} are enable.