

**Specifications**  
*of*  
**X-Wall XO-64, XO-128, XO-192**  
**Real-time IDE Cryptographic Device**

**Revision History**

Rev No.	Description	Rev. Date
0.1	Initial release	04/21/04
0.2	2 <sup>nd</sup> release	6/20/04
0.3	3 <sup>rd</sup> release	06/22/04
0.3.1	4 <sup>th</sup> release	08/04/04
0.4	5 <sup>th</sup> release	05/16/05

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## **1. Introduction**

The *X-Wall XO* ASIC (Application Specific Integrated Circuit) family is engineered specifically to encrypt/decrypt the entire ATA hard disk including boot sector, operating system, and all swap/spool files without performance loss. The operation of en/decryption is totally transparent to all users. The *X-Wall XO* eliminates platform dependency and requires no device drivers or software upgrade, reducing dramatically your total cost of ownership. The NIST (National Institute of Standards and Technology) of the United States of America and CSE (Communications Security Establishment) of the Government of Canada **certified DES**<sup>1</sup> (Data Encryption Standard) and **TDES**<sup>2</sup> (Triple DES) hardware cryptographic engines are being utilized in the *X-Wall XO* microchips to ensure the quality of cryptographic operations.

The *X-Wall XO* differs from previous *X-Wall* family chips (SE & LX versions) with its lower operating frequency (66MHz) of cryptographic hardware engine for significant power saving, Chip Status Register (CSR), and built-in Application Programming Interface (API). More, it has a built-in Power On Self Test (POST) function, that allows a program to verify if the *XO* is actually functioning.

The *X-Wall XO* is an IDE interface based cryptographic real-time device. It's ATA-6 compliant and supports up to Ultra ATA 133MB/sec operation. It can also be operated at PIO modes 0 to 4 and Ultra ATA modes 0 to 6.

With *X-Wall XO* proprietary design you can choose to deliver the required "**Secret\_Key**" via the Host IDE interface to *X-Wall XO* using *XO* specific command sets through the built-in API. Alternately, the "**Secret\_Key**" may also be delivered through *XO*'s built-in 2-wire serial EEPROM interface.

### **Features**

- NIST and CSE certified hardware DES/TDES cryptographic engine delivers significant performance improvement over traditional software disk encryption software
- Offers strong hardware based security to protect the critical "data at rest"
- Eliminates entirely platform dependency
- Real-time automatic transparent cryptographic operations
- 1.1Gbit/sec cryptographic engine design to meet Ultra ATA mode 6 (133MB/sec) burst mode
- ATA-6 Interface Compliant
- Supports PIO modes 0 to 4 and Ultra ATA modes 0 to 6
- Supports 48-bit LBA addressing
- 3.3V at 66MHz operation to conserve power consumption
- 128-pin TQFP or BGA package

<sup>1</sup> You can view Enova's DES certification #143 at <http://csrc.nist.gov/cryptval/des/desval.html>

<sup>2</sup> You can view Enova's TDES certification #92 at <http://csrc.nist.gov/cryptval/des/tripledesval.html>

The following table shows the current available *X-Wall SE*, *LX*, and *XO* family microchips. Please note, all *X-Wall SE* series chips are pin-to-pin compatible. Likewise, all *X-Wall LX* series chips are pin-to-pin compatible, and all *X-Wall XO* series chips are pin-to-pin compatible. However, the pin assignment of the three series is different. The major differences among the *X-Wall LX*, *SE*, and *XO* are listed below.

	Crypto Engine Throughput	Ultra ATA Protocols Supported	Required External OSC?	Core Voltage	Secure Key Voltage
<i>X-Wall XO</i>	1.1Gbit/sec	Ultra ATA 66/100/133	No, Just crystal	+3.3V	+3.3V
<i>X-Wall LX</i>	1.6Gbit/sec	Ultra ATA 66/100/133	No, Just crystal	+3.3V	+3.3V/5V
<i>X-Wall SE</i>	1.1Gbit/sec	Ultra ATA 33/66/100	YES	+5V	+5V

**Table 1. The major differences amongst *X-Wall XO*, *LX* and *SE***

Status	X-Wall	Key Strength	NIST Certified 100% hardware Crypto Engine	Maximum Throughput of the Crypto Engine	Protocol & Interface support up to	Package
Ready	SE-40NB	40-bit	DES	712Mbit/sec @66MHz	Ultra ATA Mode 4	128-pin LQFP
Ready	SE-64NB	64-bit	DES	712Mbit/sec @66MHz	Ultra ATA Mode 4	128-pin LQFP
Ready	SE-40A	40-bit	DES	1.1Gbit/sec @100 or 133MHz	Ultra ATA Mode 4	128-pin LQFP
Ready	SE-64A	64-bit	DES	1.1Gbit/sec @100 or 133MHz	Ultra ATA Mode 4	128-pin LQFP
Ready	SE-128A	128-bit	TDES	1.1Gbit/sec @100 or 133MHz	Ultra ATA Mode 4	128-pin LQFP
Ready	SE-192A	192-bit	TDES	1.1Gbit/sec @100 or 133MHz	Ultra ATA Mode 4	128-pin LQFP
Ready	LX-40	40-bit	DES	1.6Gbit/sec @100 or 133MHz	Ultra ATA Mode 6	128-pin LQFP
Ready	LX-64	64-bit	DES	1.6Gbit/sec @100 or 133MHz	Ultra ATA Mode 6	128-pin LQFP
Ready	LX-128	128-bit	TDES	1.6Gbit/sec @100 or 133MHz	Ultra ATA Mode 6	128-pin LQFP
Ready	LX-192	192-bit	TDES	1.6Gbit/sec @100 or 133MHz	Ultra ATA Mode 6	128-pin LQFP
Ready	XO-64	64-bit	DES	1.1Gbit/sec @66MHz	Ultra ATA Mode 6	128-pin TQFP
Ready	XO-128	128-bit	TDES	1.1Gbit/sec @66MHz	Ultra ATA Mode 6	128-pin TQFP
Ready	XO-192	192-bit	TDES	1.1Gbit/sec @66MHz	Ultra ATA Mode 6	128-pin TQFP

Table 2. The X-Wall XO, LX, & SE Family Microchips

### System Requirement

- ❑ All operating systems
- ❑ Ultra ATA (Ultra DMA) 66/100/133 (66MByte/sec, 100MByte/sec, 133MByte/sec) compliant hard disk drive
- ❑ Motherboard with standard IDE interface
- ❑ One disk drive per X-Wall XO
- ❑ Does NOT support ATAPI devices such as CD-ROM, CD-R, CD-RW, DVD-ROM or DVD-RW

## 2. System Configurations

### 2.1 Disk Drive Configurations

The configuration of X-Wall XO is flexible. You may select your X-Wall XO configuration from one of the four configurations to control disk drives. Please refer to Table 3. Four possible configurations below.

X-Wall XO	Primary	Secondary
Master	Yes	Yes
Slave	Yes	Yes

Table 3. Four possible configurations

### 2.2 System Configurations

Considering each standard computer comes only two IDE channels (Primary and Secondary), there are three possible configurations of X-Wall XO to work with the IDE hard drive on respective channel:

1. One X-Wall XO configured with one hard drive;
2. One X-Wall XO configured with two hard drives;
3. Two X-Wall XO configured with two hard drives;

The one X-Wall XO configured with one hard drive configuration comprises with only one hard drive in either Primary or Secondary IDE channels. **Figure 1. One X-Wall XO configured with one hard drive** shows one X-Wall XO configured with one hard drive. The hard drive connected after the X-Wall XO is fully encrypted and protected.

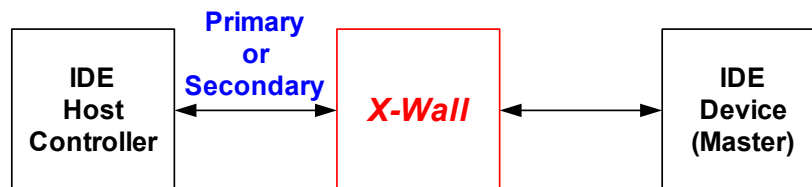


Figure 1: One X-Wall XO configured with one hard drive

The one X-Wall XO configured with two hard drives configuration comprises with two hard drives with only one X-Wall XO in either Primary or Secondary channel. **Figure 2. One X-Wall XO configured with two hard drives** shows this configuration, of which drive connected after the X-Wall XO is fully encrypted and protected. The hard drive before the X-Wall XO is unencrypted and unprotected.

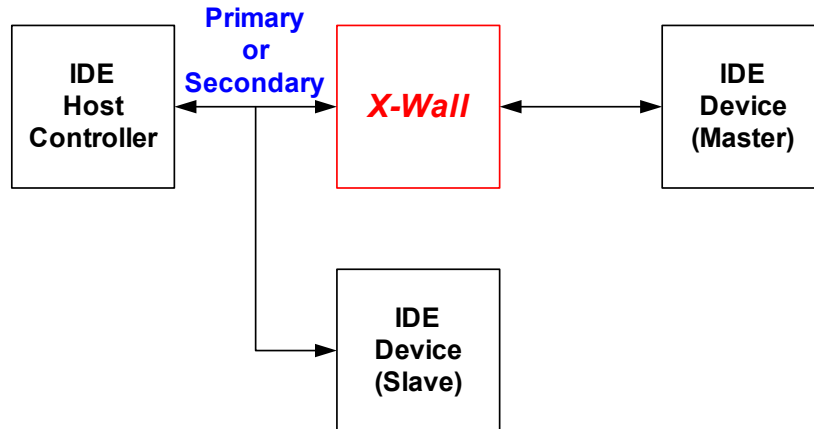


Figure 2. One X-Wall XO configured with two hard drives

The two X-Wall XO configured with two hard drives configuration comprises with two hard drives with two X-Wall XO in either Primary or Secondary channel. Figure 3. Two X-Wall XO configured with two hard drives shows this configuration, of which two hard drives connected respectively after X-Wall XO are fully encrypted and protected.

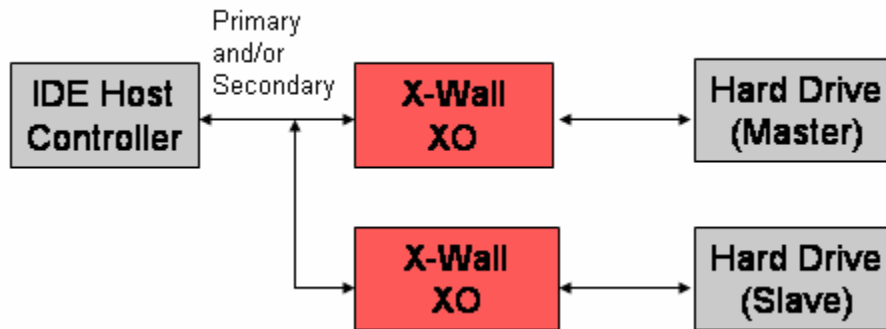


Figure 3. Two X-Wall XO configured with two hard drives

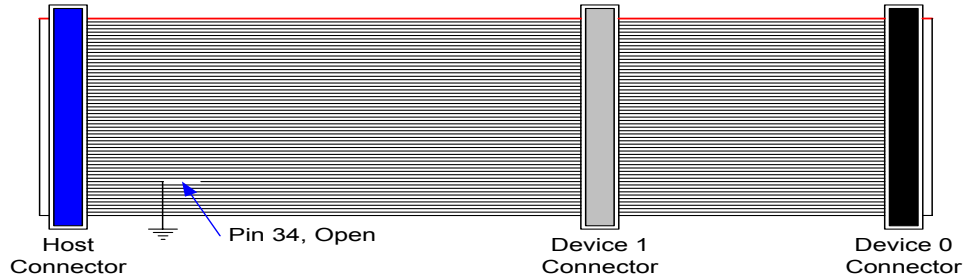
### 2.3 IDE Cables

The Ultra ATA 66/100/133 transfer modes require an 80-conductor cable (as shown in Figure 4. A standard 80-conductor cable) whereas Ultra ATA 33 and below (including PIO) only demand a 40-conductor cable (as shown in Figure 5. A standard 40-conductor cable).

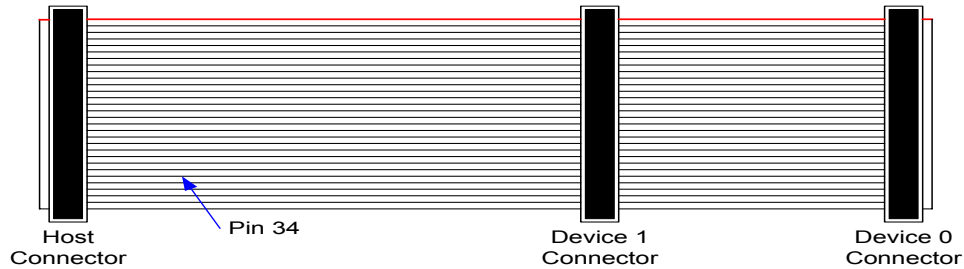
An 80-conductor IDE cable uses the same 40-pin connector as the 40-conductor IDE cable. The wires of the 80-conductor cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard or circuit board through the ground pins in the 40-conductor Connector).

To determine that if Ultra DMA transfer modes greater than 2 (Ultra ATA/33, 33MB/sec transfer rate) can be enabled, the host requires the system software to attempt to determine the cable type used in the system through **Pin 34** of the connector as shown

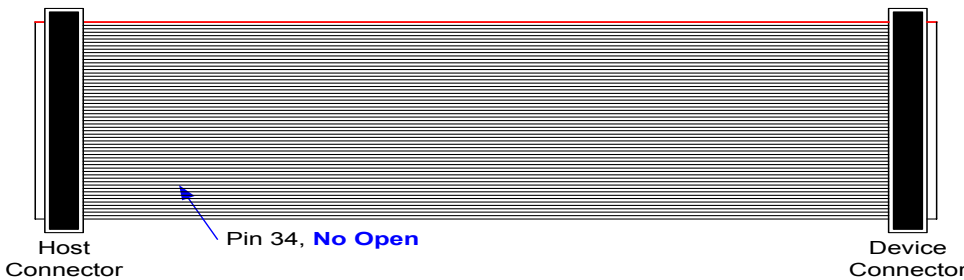
in Figure 4. A standard 80-conductor cable. If the system software detects an 80-conductor cable, the system may use any one of all the available Ultra DMA transfer modes up to the highest transfer mode supported by both the south bridge chipset and the IDE device. If a 40-conductor cable is detected, the system software can NOT enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).



**Figure 4. A standard 80-conductor cable (Pin 34 is grounded inside the 40-pin connector)**

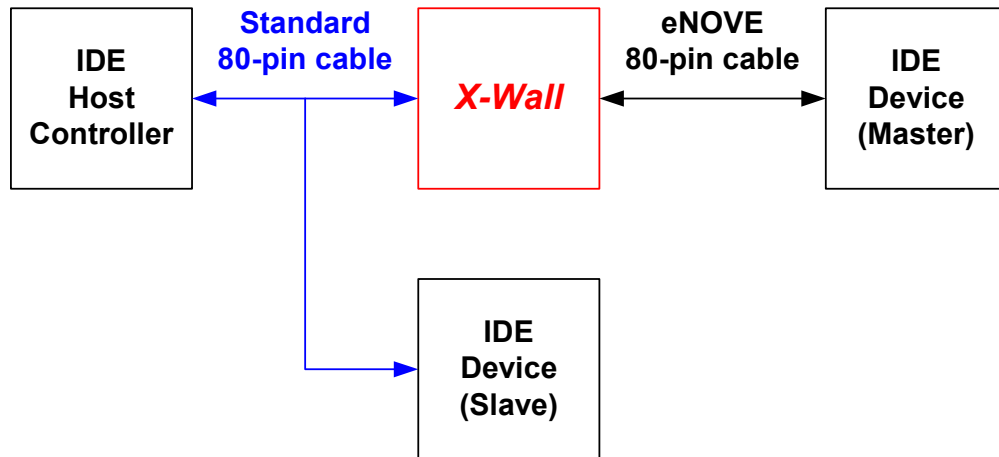


**Figure 5. A standard 40-conductor cable (Pin 34 is NOT grounded)**



**Figure 6. Enova specifically assembled 80-conductor cable (Pin 34 is NOT grounded)**

If the system configuration comprises with one X-Wall XO and two hard drives as shown in Figure 2. One X-Wall XO configured with two hard drives, we suggest that the system maker should provide one Enova specifically assembled 80-conductor cable as shown in Figure 6. Enova specifically assembled 80-conductor cable. The suggested connection with two hard drives on the same channel is shown in Figure 7. Suggested cable connection to avoid possible technical problems.

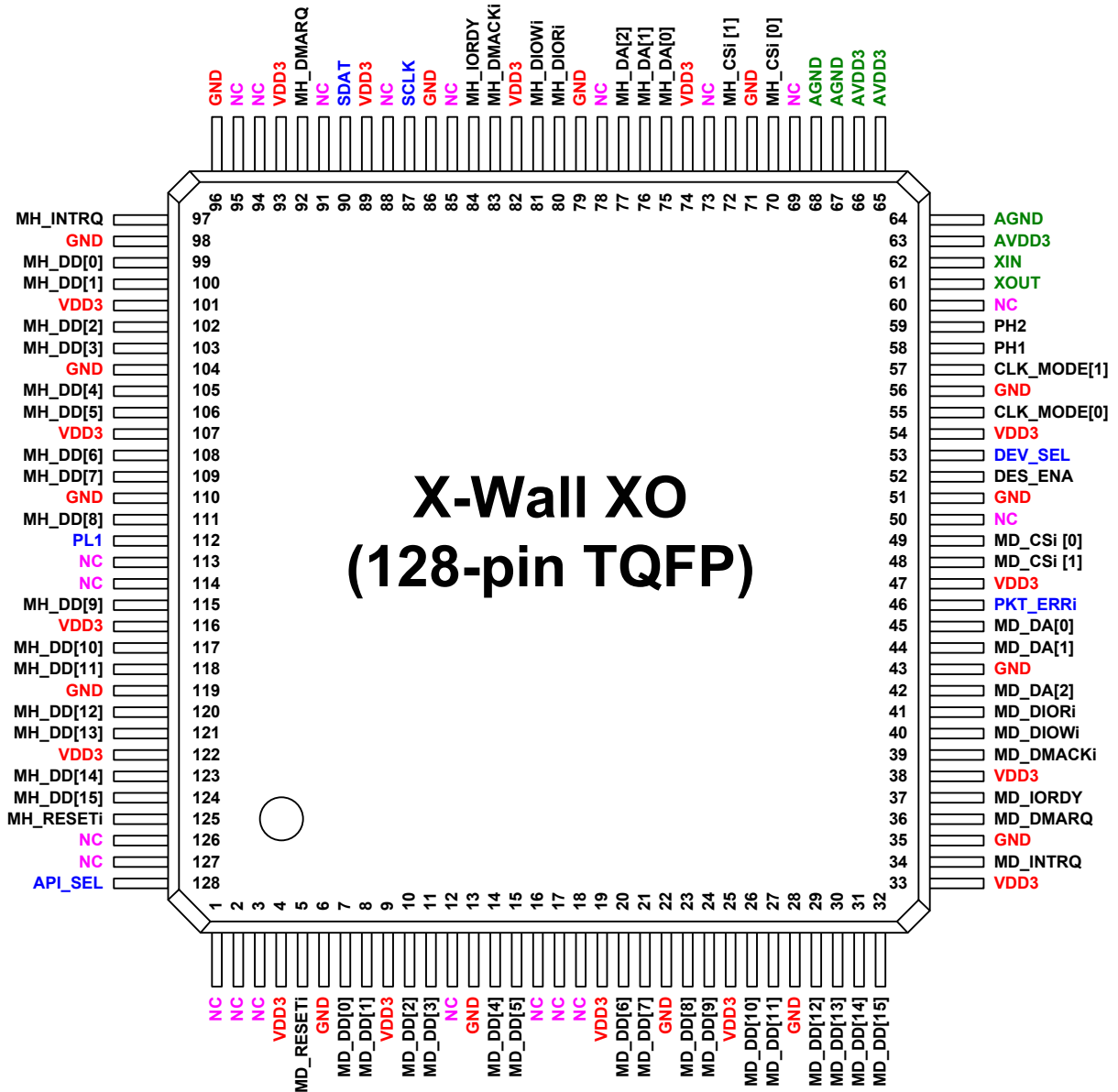


**Figure 7. Suggested cable connection**

### 3. X-Wall XO Pin Definition & Description

#### 3.1 Pin Assignment

All X-Wall XO family microchips (including XO-64, XO-128 and XO-192) share the same pin assignment and pin definition.



#### 3.2 Pin Definition & Description

##### 3.2.1 Host IDE Interface (From IDE Host Controller)

Pin Names	I/O	TQFP	Description
-----------	-----	------	-------------

MH_CSi [1:0]	I	72, 70	Chip select 0 & Chip select 1 driven by the Host
MH_DD[15:0]	I/O 8mA	124, 123, 121, 120, 118, 117, 115, 111, 109, 108, 106, 105, 103, 102, 100, 99	IDE Data Driven by the Host and X-Wall
MH_DA[2:0]	I	77, 76, 75	IDE address driven by the Host
MH_DMACKi	I	83	IDE DMA acknowledge driven by Host
MH_DMARQ	O 8mA	92	IDE DMA request driven by X-Wall
MH_INTRQ	O 8mA	97	IDE Interrupt request driven by X-Wall
MH_DIORi	I	80	Driven by the Host, internally splits into: for PIO Mode: MH_DIORi for UDMA Data-In: MH_HDMARDYi for UDMA Data-Out: MH_HSTROBE
MH_IORDY	O 8mA	84	Driven by X-Wall, one of the 3 signals is selected: for PIO Mode: MH_IORDY for UDMA Data-In: MH_DSTROBE for UDMA Data-Out: MH_DDMARDYi
MH_DIOWi	I	81	Driven by the Host, internally splits into: for PIO Mode: MH_DIOWi for UDMA Data-In: MH_STOP for UDMA Data-Out: MH_STOP
MH_RESETi	I	125	Host reset signal

### 3.2.2 Device IDE Interface (to hard drive)

Pin Names	Type	TQFP	Description
MD_CSi [1:0]	O 8mA	48, 49	Chip select 0 & Chip select 1 driven by the X-Wall
MD_DD[15:0]	I/O 8mA	32, 31, 30, 29, 27, 26, 24, 23, 21, 20, 15, 14, 11, 10, 8, 7	IDE Data Driven by both X-Wall and Device
MD_DA[2:0]	O 8mA	42, 44, 45	IDE address driven by X-Wall
MD_DMACKi	O 8mA	39	IDE DMA acknowledge driven by X-Wall
MD_DMARQ	I	36	IDE DMA request driven by Device
MD_INTRQ	I	34	IDE Interrupt request driven by Device
MD_DIORi	O	41	Driven by X-Wall, one of the 3 signals is selected:

	8mA		for PIO Mode: MD_DIORi for UDMA Data-In: MD_HDMARDYi for UDMA Data-Out: MD_HSTROBE
MD_IORDY	I	37	Driven by X-Wall, internal splits into: for PIO Mode: MD_IORDY for UDMA Data-In: MD_DSTROBE for UDMA Data-Out: MD_DDMARDYi
MD_DIOWi	O 8mA	40	Driven by X-Wall, one of the 2 signals is selected: for PIO Mode: MD_DIOWi for UDMA Data-In: MD_STOP for UDMA Data-Out: MD_STOP
MD_RESETi	O 8mA	5	Reset signal, driven by X-Wall

### 3.2.3 Serial EEPROM interface

Pin Names	Type	TQFP	Description
SCLK	O 4mA	87	Serial EEPROM Clock Output Connect to external 24C01 type serial EEPROM
SDAT	I/O 4mA	90	Serial EEPROM Data Input/Output Connect to external 24C01 type serial EEPROM

### 3.2.4 Power pins

Pin Names	Type	TQFP	Description
VDD3	P	4, 9, 19, 25, 33, 38, 47, 54, 74, 82, 89, 93, 101, 107, 116, 122	+3.3V Power Supply (Digital)
AVDD3	P	63, 65, 66	+3.3V Power Supply (Analog)
GND	P	6, 13, 22, 28, 35, 43, 51, 56, 71, 79, 86, 96, 98, 104, 110, 119	Ground
AGND	P	64, 67, 68	Analog Ground

### 3.2.5 Others

Pin Names	Type	TQFP	Description
CLK_MODE [1:0]	I	57, 55	Hardware Traps to set X-Wall internal clock frequency
DES_ENA	I	52	Hardware Traps for Encryption/Decryption Enabling

DEV_SEL	I	53	Hardware Traps to set device as master or slave
API_SEL	I	128	Hardware Traps to select the way to input Secret_Key via either 2-wire serial EEPROM Interface or Host IDE interface
PH1	I	58	PULL-HIGH 1(Pull-High with 10K $\Omega$ )
PH2	I	59	PULL-HIGH 2(Pull-High with 10K $\Omega$ )
PL1	I	112	PULL-LOW 1 (Pull-Low with 1K $\Omega$ )
PKT_ERRi	O 4mA	46	Output Low for non-existence of Secret_Key or Secret_Key parity error
XIN	I	62	Crystal input pad (14.318MHz)
XOUT	O	61	Crystal output pad
NC	-	1, 2, 3, 12, 16, 17, 18, 50, 60, 69, 73, 78, 85, 88, 91, 94, 95, 113, 114, 126, 127	No Connection

#### 4. X-Wall XO Specific Command & Register Sets

In addition to the standard ATA commands, the X-Wall XO has implemented two ATA mode commands and four USER mode commands. With these commands the host can get status and information via X-Wall XO register sets. Those commands and register sets are listed below.

##### ■ X-Wall XO Specific Command Sets

Command	Command Code/Set	Description
<b>READ_CHIP_STATUS</b>	58h/ATA	For the Host to read out the status of XO via the Status Register
<b>START_USER_MODE</b>	59h/ATA	For the Host to force XO into USER mode for KEY entry
<b>SET_BYPASS</b>	01h/USER	To force XO into By-pass mode from Encryption mode
<b>SET_ENCRYPTION</b>	02h/USER	To force XO into Encryption mode from By-pass mode
<b>LOAD_KEY</b>	1Ah/USER	For loading the KEY
<b>END_USER_MODE</b>	0Fh/USER	To end the USER mode

##### ■ X-Wall XO Register Sets

ATA mode Register Sets		User Mode Register Sets	
Name	Location	Name	Location
Command Register	1F7W	Command Register	1F7W
Chip Status Register	1F0R	Acknowledge Register	1F2R
		Data Port Register	1F0W
		USER mode Chip Status Register	1F0R

The two ATA mode commands (58h and 59h) are reserved in the ATA standard. When the IDE host issues these two XO specific ATA mode commands, only X-Wall XO will respond to them. In addition, the USER mode commands are only valid while XO is under the USER mode and won't be presented to the hard disk.

The XO Register Sets have two different classes: ATA mode register sets and USER mode register sets.

For more information of this section, please refer to the X-Wall XO programming guide.

## 5. Electrical Characteristics

This section contains the electrical specifications for the X-Wall XO. Please note, however, stressing conditions beyond the “Absolute Maximum Ratings” may cause permanent damage to the X-Wall device. Operating beyond the “operating conditions” is not recommended and extended exposure beyond “operating conditions” may adversely affect life and reliability of the X-Wall device.

### ■ Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
Ts	Storage Temperature	-55	+125	°C
Ta	Operating Temperature	0	70	°C
VDD3	Supply Voltage (Digital)	-0.5	3.6	V
AVDD3	Supply Voltage (Analog)	-0.5	3.6	V
VSIN	Input Signal Voltage (Apply to all pins)	-0.5	5	V
VSO	Output Signal Voltage (Apply to all pins)	-0.5	VDD3	V

### ■ DC Characteristics

Operating Conditions: VDD3=AVDD3=3.3V(±9.09%), GND=0V

Symbol	Parameter		Value		Unit	
			Min	Max		
VDD3	Supply voltage (Digital)		3.0	3.6	V	
AVDD3	Supply voltage (Analog)		3.0	3.6	V	
IVDD	Supply current (IVDD3 + IAVDD3)	XO-64	66MHz	75	150	mA
			100MHz	105	210	mA
			133MHz	133	280	mA
		XO-128	66MHz	75	195	mA
		XO-192	100MHz	105	275	mA
			133MHz	133	360	mA

## 6. Layout & Package Information

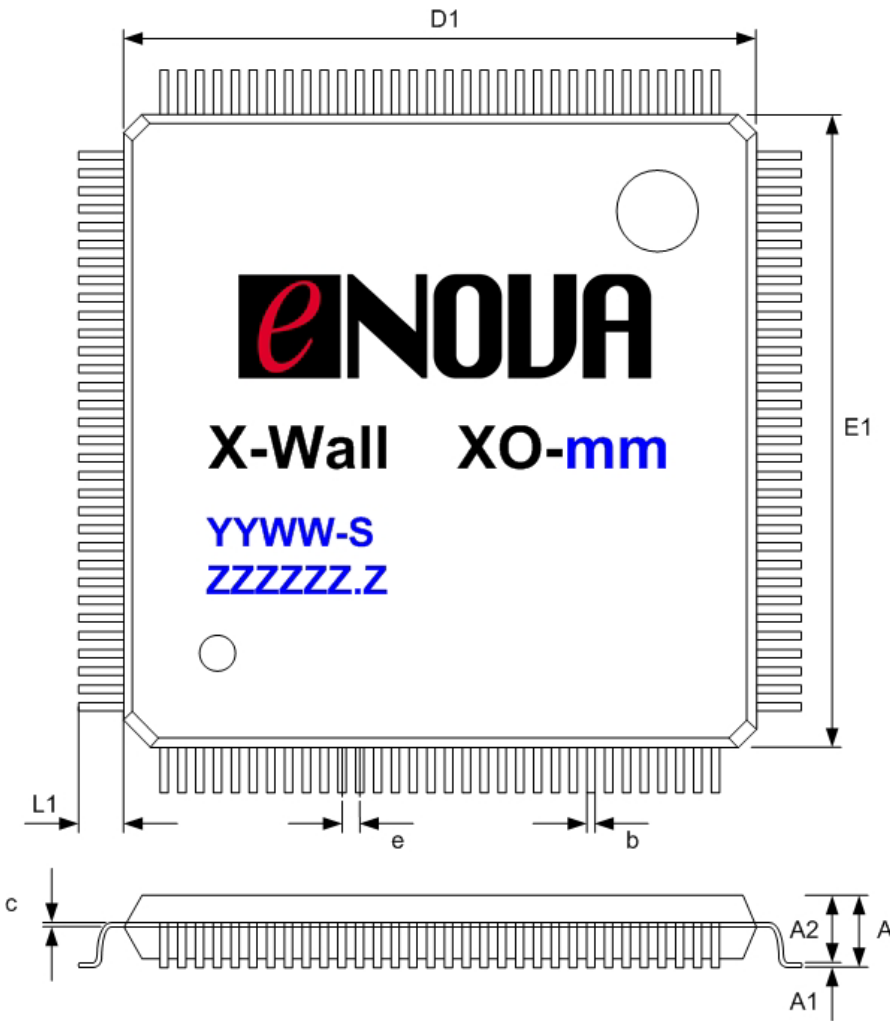
### 6.1 128-pin TQFP

TQFP (Thin Quad Flat Package) provides low profile with 1.2mm body thickness, suitable for space concerned applications. Package size 14×14mm and lead-count 128 are offered for portable, lightweight and low profile applications.

### 6.2 FEATURES

- ◆ 14×14mm body size with 128 lead count
- ◆ Copper leadframe
- ◆ Low profile 1.40mm body thickness
- ◆ JEDEC standard outlines

### 6.3 Outline & Dimension



Symbol	Dimension in [mm]
D1	14.00
E1	14.00
L1	1.00
e	0.40
b	0.18
c	0.127
A	1.20(MAX)
A2	1.00
A1	0.05(MIN)

\*L/F Materia Cu:C7025

X-Wall XO Top Mark

mm:  
 = 64, DES 64-bits  
 = 128, TDES 128-bits  
 = 192, TDES 192-bits

YYWW-S:  
 Date Code  
 ZZZZZZ.Z  
 Lot NO.

## 7. Reliability Tests

### 7.1 Product Life Test

Test Items	Test Condition/Result	Reference Standard
Operating Life	TA=125°C , 500Hours, Pass TA=125°C , 1,000Hours, On going	JESD22-A108-A

### 7.2 Electrical Test

Test Items	Test Condition/Result	Reference Standard
ESD	Level II	MIL-STD-883E 3015.7 JEDEC EIA/JESD22-A115
Latch-up	Level II	JEDEC-STD NO 78

### 7.3 Packaging Test

Test Items	Test Condition	Reference Standard
Thermal Shock	-65 Deg C/+150 Deg C 5min within 10 sec 5min 300 Cycles	MIL-STD-883E 1011.9
Temp. Cycling	-65 Deg C/+150 Deg C 1000 Cycles	MIL-STD-883E 1010.7
Pressure Cooker	121 Deg C, 15 psig (2atm) 100% R.H. 216 hours	JEDEC-STD A102-2
Salt Atmosphere	35 Deg C, 0.5%~3% NaCl PH6.5~7.2 24 hours	MIL-STD-883E 1009.8
HAST	TA=130 Deg C, 85%R.H. 64 hours	JEDEC-STD NO. 22-A110

**8. Marking Description (RoHS compliant in RED)**

**X-Wall XO-64 & X-Wall XO-64U**

XO – version  
 64 – DES 64-bit strength  
**U – RoHS compliant**

**X-Wall XO-128 & X-Wall XO-128U**

XO – version  
 128 – TDES 128-bit strength  
**U – RoHS compliant**

**X-Wall XO-192 & X-Wall XO-192U**

XO – version  
 192 – TDES 192-bit strength  
**U – RoHS compliant**

**0426-S**

0426 -- Year and Week of manufacturing date; Year 2004 on Week 26<sup>th</sup>  
 S -- Package & assembly House; SPIL

**F60227.3** – Silicon Wafer Lot Number

**9. Logistics**

Package	Dimension	Capacity (Max.)	Weight
Chip	14*14*1.2mm	1ea	
Tray	322*136*7 mm, 6*15 grid, black	90ea	
Inner Box	364*156*87 mm, white	900ea	2.2kg
Carton	382*341*294 mm, white	5400ea	12kg Max

**10. Standard Material (RoHS compliant in RED)**

<b>Chip</b>	<b>Non-epi wafer + TSMC process</b>
Lead frame	Copper
Die Attach Adhesive	Silver paste
Bonding Wire	Gold
Encapsulant	Mold Compound
Lead Finish	85/15 Sn/Pb ( <b>Eutectic 63/37 Sn/Pb</b> )

**11. Platform Placement**

Signal arrangement of the X-Wall XO is shown in Figure 8. Signal arrangement of X-Wall XO.

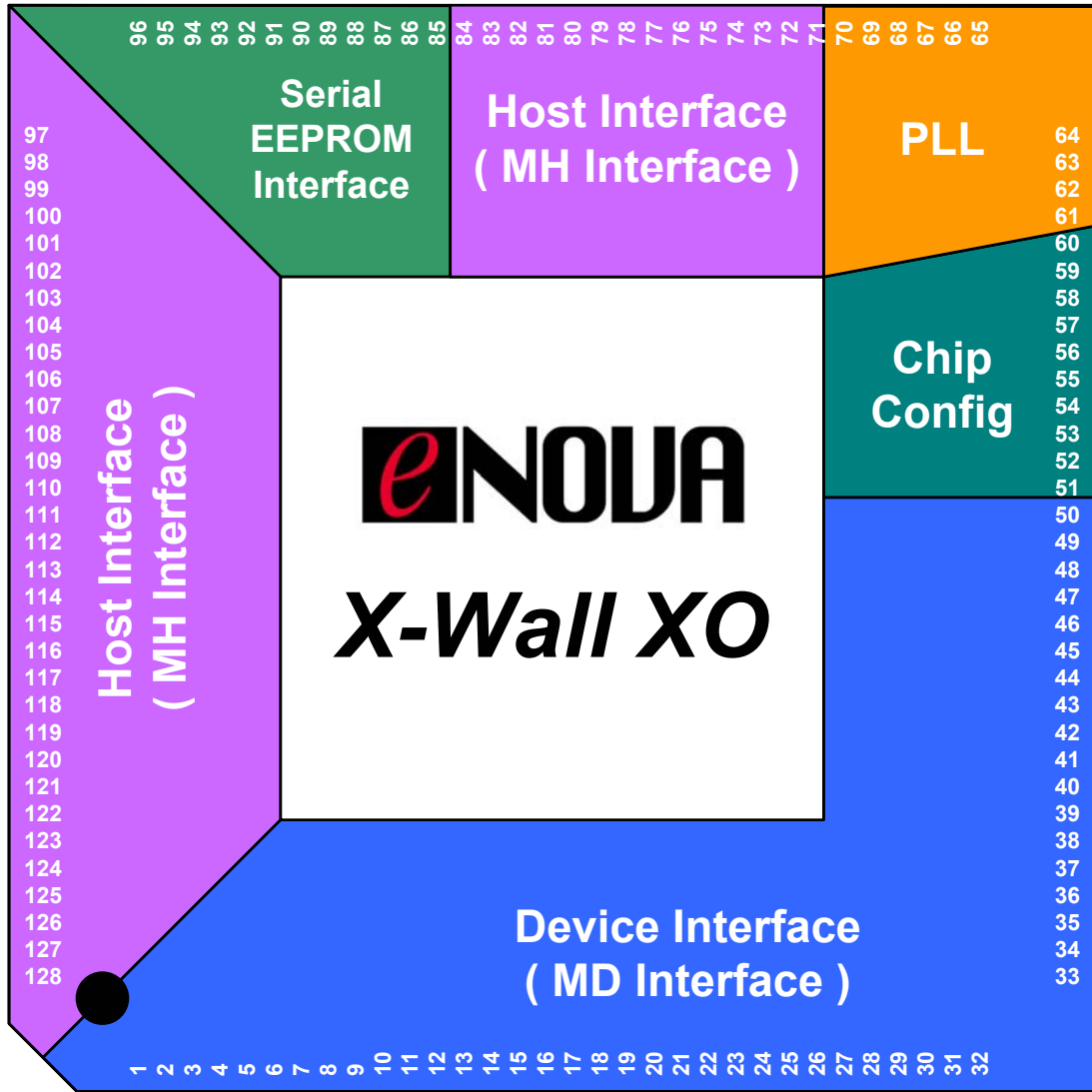


Figure 8. Signal arrangement of X-Wall XO

Filename: X-Wall XO Specifications Rev 0.4 051605  
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Template: C:\Documents and Settings\Robert Wann\Application  
Data\Microsoft\Templates\Normal.dot  
Title: X-Wall XO Specifications Rev 0.31  
Subject: X-Wall XO  
Author: Robert Wann  
Keywords:  
Comments:  
Creation Date: 5/20/2005 1:14 PM  
Change Number: 5  
Last Saved On: 5/20/2005 1:26 PM  
Last Saved By: Robert Wann  
Total Editing Time: 5 Minutes  
Last Printed On: 5/20/2005 1:27 PM  
As of Last Complete Printing  
Number of Pages: 19  
Number of Words: 2,989 (approx.)  
Number of Characters: 17,039 (approx.)