

# SN54CDC586

## 3.3-V PHASE-LOCK-LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS

SGBS311 – FEBRUARY 1997

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V  $V_{CC}$
- Distributes One Clock Input to Twelve Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input
- Application for Synchronous DRAM, High-Speed Microprocessor
- TTL-Compatible Inputs and Outputs
- Outputs Drive Parallel 50- $\Omega$  Terminated Transmission Lines
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed  $V_{CC}$  and Ground Pins Reduce Switching Noise
- Packaged in 56-Pin Ceramic Flat Package

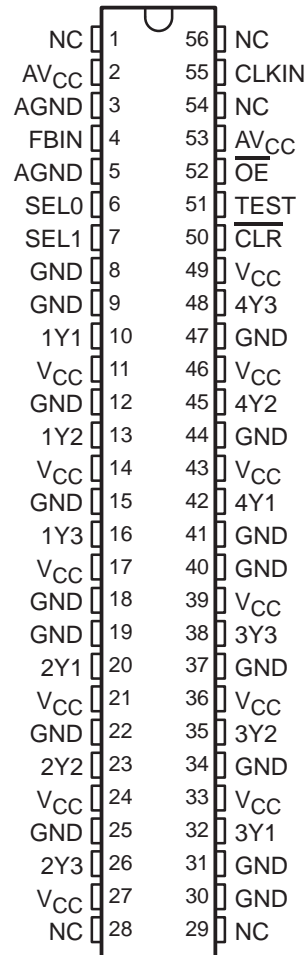
### description

The SN54CDC586 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with popular microprocessors operating at speeds from 50 MHz to 100 MHz, or down to 25 MHz on outputs configured as half-frequency outputs. The SN54CDC586 operates at 3.3-V  $V_{CC}$  and is designed to drive a properly terminated 50- $\Omega$  transmission line.

The feedback input (FBIN) is used to synchronize the output clocks in frequency and phase to CLKIN. One of the 12 output clocks must be fed back to FBIN for the PLL to maintain synchronization between the CLKIN input and the outputs. The output used as the feedback pin is synchronized to the same frequency as the CLKIN input.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. Select inputs (SEL1, SEL0) configure up to nine Y outputs, in banks of three, to operate at one-half or double the CLKIN frequency, depending on which pin is fed back to FBIN (see Tables 1 and 2). All output-signal duty cycles are adjusted to 50%, independent of the duty cycle at CLKIN.

WD PACKAGE  
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

# SN54CDC586

## 3.3-V PHASE-LOCK-LOOP CLOCK DRIVER WITH 3-STATE OUTPUTS

SGBS311 – FEBRUARY 1997

---

### description (continued)

Output-enable ( $\overline{OE}$ ) is provided for output control. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. When  $\overline{OE}$  is low, the outputs are active.  $\overline{CLR}$  is negative-edge triggered and can be used to reset the outputs operating at half frequency. TEST is used for factory testing of the device and can be used to bypass the PLL. TEST should be strapped to GND for normal operation.

Unlike many products containing PLLs, the SN54CDC586 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the SN54CDC586 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLKIN, as well as following any changes to the PLL reference or feedback signals. Such changes occur upon change of the select inputs, enabling of the PLL via TEST, and upon enable of all outputs via  $\overline{OE}$ .

The SN54CDC586 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### detailed description of output configurations

The voltage-controlled oscillator (VCO) used in the SN54CDC586 PLL has a frequency range of 100 MHz to 200 MHz, twice the operating frequency range of the SN54CDC586 outputs. The output of the VCO is divided by two and by four to provide reference frequencies with a 50% duty cycle of one-half and one-fourth the VCO frequency. SEL0 and SEL1 select which of the two signals are buffered to each bank of device outputs.

One device output must be externally wired to FBIN to complete the PLL. The VCO operates such that the frequency and phase of this output match that of CLKIN. In the case in which a VCO/2 output is wired to FBIN, the VCO must operate at twice the CLKIN frequency, resulting in device outputs that operate at either the same or one-half the CLKIN frequency. If a VCO/4 output is wired to FBIN, the device outputs operate at twice or the same frequency as the CLKIN frequency.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**output configuration A**

Output configuration A is valid when any output configured as a 1x frequency output in Table 1 is fed back to FBIN. The input frequency range for CLKIN is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at one-half the CLKIN frequency, while outputs configured as 1x outputs operate at the same frequency as CLKIN.

**Table 1. Output Configuration A**

INPUTS		OUTPUTS	
SEL1	SEL0	1/2X FREQUENCY	1X FREQUENCY
L	L	None	All
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

**output configuration B**

Output configuration B is valid when any output configured as a 1x frequency output in Table 2 is fed back to FBIN. The input frequency range for CLKIN is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the CLKIN frequency, while outputs configured as 2x outputs operate at double the frequency of CLKIN.

**Table 2. Output Configuration B**

INPUTS		OUTPUTS	
SEL1	SEL0	1X FREQUENCY	2X FREQUENCY
L	L	All	None
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3



### Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLKIN	55	I	Clock input. CLKIN is the clock signal distributed by the SN54CDC586 clock-driver circuit. CLKIN provides the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{\text{CLR}}$	50	I	Clear. $\overline{\text{CLR}}$ resets the VCO/4 reference frequency. $\overline{\text{CLR}}$ is negative-edge triggered and should be strapped to GND or $V_{CC}$ for normal operation.
FBIN	4	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the 12 clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between FBIN and CLKIN.
$\overline{\text{OE}}$	52	I	Output enable. $\overline{\text{OE}}$ is the output enable for all outputs. When $\overline{\text{OE}}$ is low, all outputs are enabled. When $\overline{\text{OE}}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output terminal, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{\text{OE}}$ , enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	7, 6	I	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g., 1 $\times$ , 1/2 $\times$ , or 2 $\times$ ). (see Tables 1 and 2).
TEST	51	I	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	10, 13, 16 20, 23, 26 32, 35, 38	O	Output ports. These outputs are configured by SEL1 and SEL0 to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on SEL1 and SEL0 and the frequency of the output being fed back to FBIN. The duty cycle of the Y-output signals is nominally 50%, independent of the duty cycle of CLKIN.
4Y1–4Y3	42, 45, 48	O	Output ports. 4Y1–4Y3 transmit one-half the frequency of the VCO regardless of the state of SEL1 and SEL0. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y-output signals is nominally 50%, independent of the duty cycle of CLKIN.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**SN54CDC586**  
**3.3-V PHASE-LOCK-LOOP CLOCK DRIVER**  
**WITH 3-STATE OUPUTS**

SGBS311 – FEBRUARY 1997

**recommended operating conditions (see Note 2)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.6	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	V
I <sub>OH</sub>	High-level output current		-32	mA
I <sub>OL</sub>	Low-level output current		32	mA
T <sub>A</sub>	Operating free-air temperature	-55	125	°C

NOTE 2: Unused inputs must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C		UNIT
		MIN	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 3 V, I <sub>I</sub> = -18 mA		-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN to MAX†, I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.2		V
	V <sub>CC</sub> = 3 V, I <sub>OH</sub> = -32 mA	2		
V <sub>OL</sub>	V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 100 μA		V
		I <sub>OL</sub> = 32 mA		
I <sub>I</sub>	V <sub>CC</sub> = 0 or MAX†, V <sub>I</sub> = 3.6 V	±10		μA
	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND	±1		
I <sub>OZH</sub>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V	10		μA
I <sub>OZL</sub>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0	-10		μA
I <sub>CC</sub>	V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		mA
		Outputs low		
		Outputs disabled		
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	4		pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	8		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



**timing requirements over recommended ranges of supply voltage and operating free-air temperature**

		MIN	MAX	UNIT	
f <sub>clock</sub>	Clock frequency	VCO is operating at four times the CLKIN frequency	25	50	MHz
		VCO is operating at double the CLKIN frequency	50	100	
Input clock duty cycle		40%	60%		
Stabilization time <sup>†</sup>	After SEL1, SEL0		50		μs
	After $\overline{OE}$ ↓		50		
	After power up		50		
	After CLKIN		50		

<sup>†</sup> Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 30 pF, unless otherwise noted (see Note 3 and Figures 1 through 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f <sub>max</sub>			100		MHz
Duty cycle		Y	42%	58%	
t <sub>phase error</sub> <sup>‡</sup>	CLKIN↑	Y	-900	200	ps
Jitter <sub>(pk-pk)</sub> <sup>*</sup>	CLKIN↑	Y		200	ps
t <sub>sk(o)</sub> <sup>‡</sup>				0.75	ns
t <sub>sk(pr)</sub> <sup>‡*</sup>				1.1	ns
t <sub>r</sub>				1.4	ns
t <sub>f</sub>				1.4	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

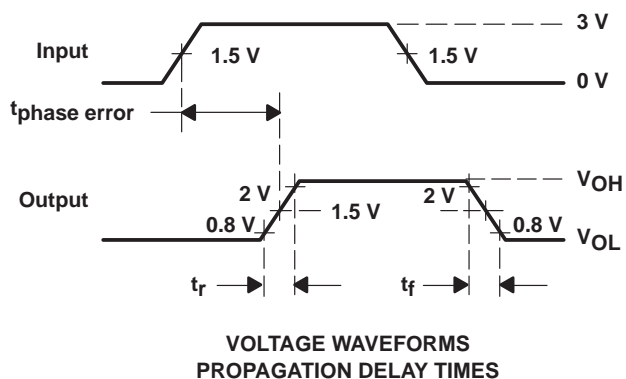
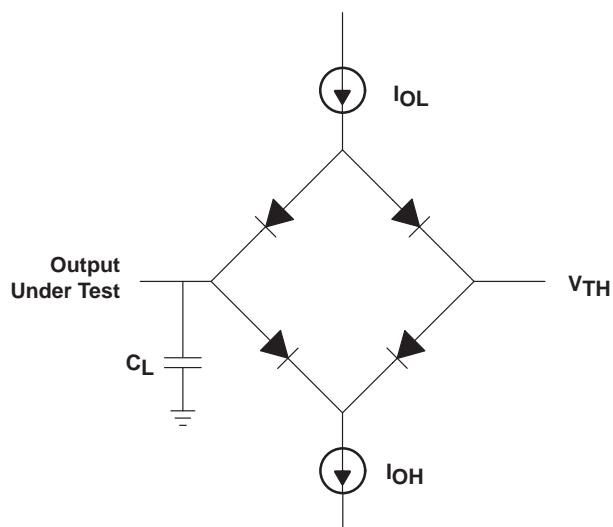
<sup>‡</sup> The propagation delay, t<sub>phase error</sub>, is dependent on the feedback path from any output to FBIN. The t<sub>phase error</sub>, t<sub>sk(o)</sub>, and t<sub>sk(pr)</sub> specifications are valid only for equal loading of all outputs.

NOTE 3: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

**SN54CDC586**  
**3.3-V PHASE-LOCK-LOOP CLOCK DRIVER**  
**WITH 3-STATE OUPUTS**

SGBS311 – FEBRUARY 1997

**PARAMETER MEASUREMENT INFORMATION**

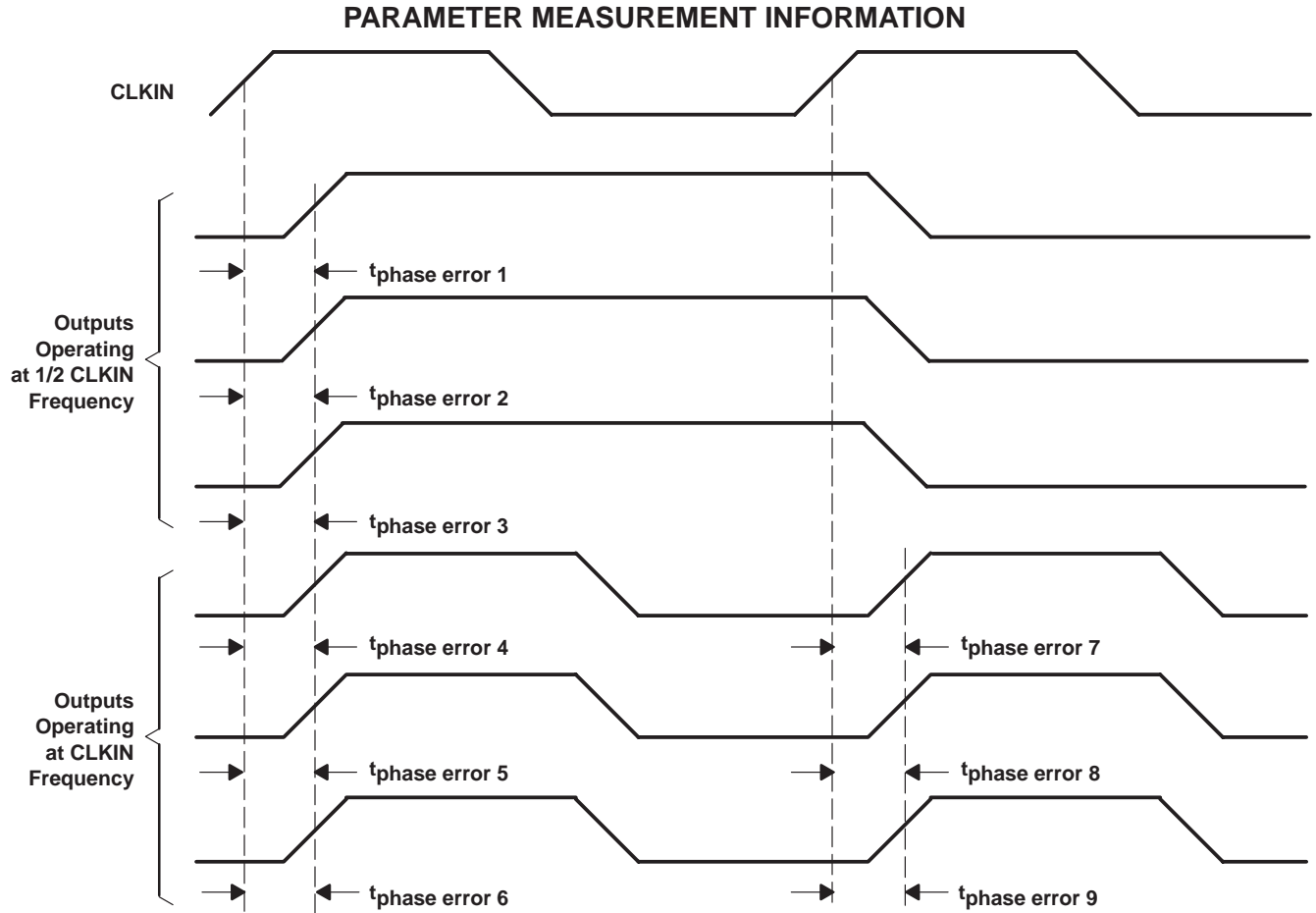


PARAMETER	$I_{OL}$	$I_{OH}$	$V_{TH}$	$C_L$ (typical)
$t_{\text{phase error}}$	32 mA	32 mA	1.5 V	20 pF
$t_r, t_f$	16 mA	16 mA	1.5 V	20 pF

**LOAD CIRCUIT**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The outputs are measured one at a time with one transition per measurement.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 100$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.

**Figure 1. Load Circuit and Voltage Waveforms**



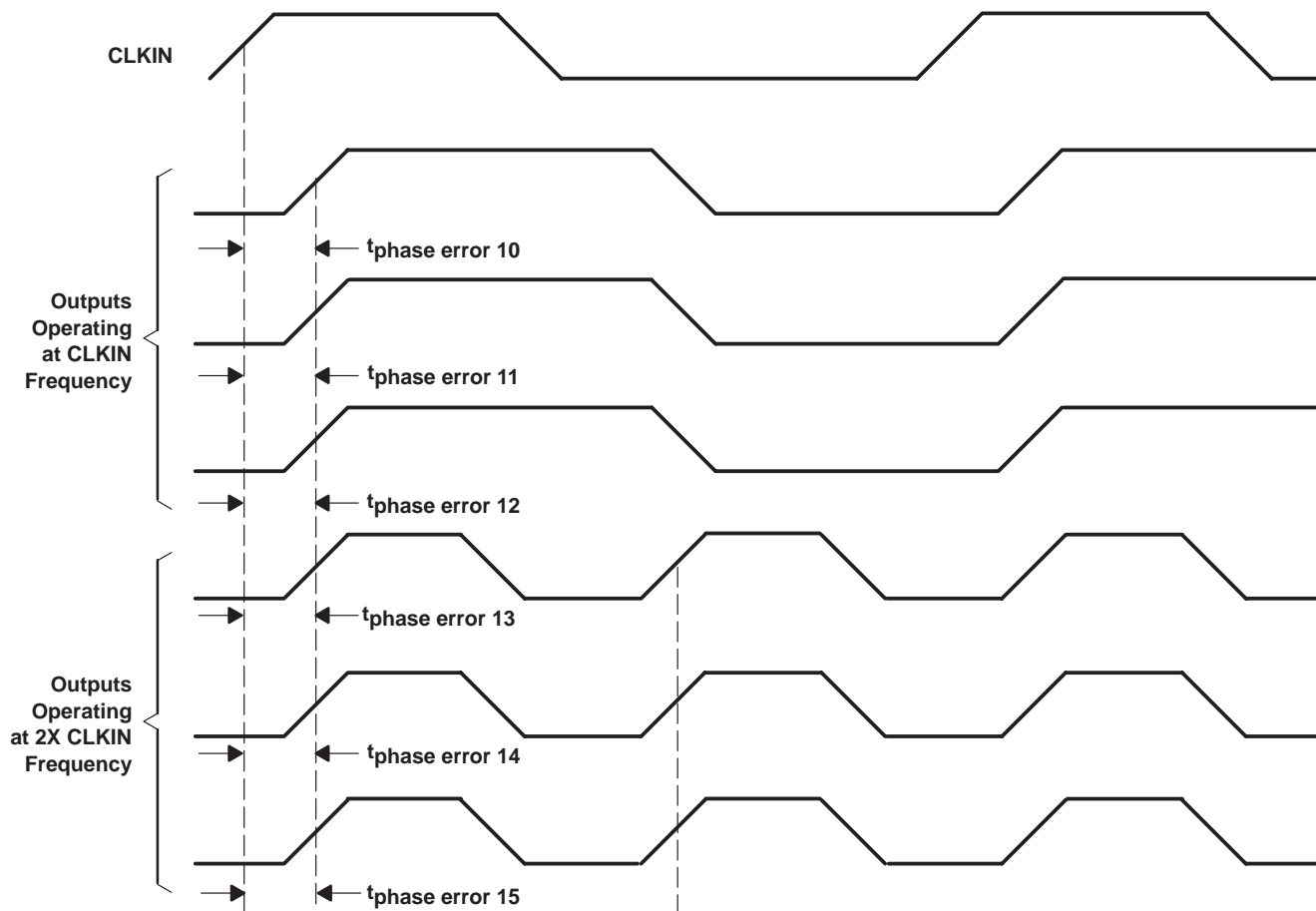
- NOTES: A. Output skew,  $t_{sk(o)}$ , is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{phase\ error\ n}$  ( $n = 1, 2, \dots, 6$ )
  - The difference between the fastest and slowest of  $t_{phase\ error\ n}$  ( $n = 7, 8, 9$ )
- B. Process skew,  $t_{sk(pr)}$ , is calculated as the greater of:
- The difference between the maximum and minimum  $t_{phase\ error\ n}$  ( $n = 1, 2, \dots, 6$ ) across multiple devices under identical operating conditions.
  - The difference between the maximum and minimum  $t_{phase\ error\ n}$  ( $n = 7, 8, 9$ ) across multiple devices under identical operating conditions.

**Figure 2. Waveforms for Calculation of  $t_{sk(o)}$**

**SN54CDC586**  
**3.3-V PHASE-LOCK-LOOP CLOCK DRIVER**  
**WITH 3-STATE OUPUTS**

SGBS311 – FEBRUARY 1997

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. Output skew,  $t_{sk(o)}$ , is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{phase\ error\ n}$  ( $n = 10, 11, \dots, 15$ )
- B. Process skew,  $t_{sk(pr)}$ , is calculated as the greater of:
- The difference between the maximum and minimum  $t_{phase\ error\ n}$  ( $n = 10, 11, \dots, 15$ ) across multiple devices under identical operating conditions.

**Figure 3. Waveforms for Calculation of  $t_{sk(o)}$  and  $t_{sk(pr)}$**

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.




**TEXAS INSTRUMENTS**
THE WORLD LEADER IN DSP AND ANALOG

Advanced Search
  TI Home
  TI&ME
  Employment  
 Tech Support
  Comments
  Site Map
  TI Global

[PRODUCT FOLDER](#) | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY](#) | [BLOCK DIAGRAMS](#)

PRODUCT SUPPORT: [APPLICATIONS](#)

## SN54CDC586, 3.3-V Phase-Lock-Loop Clock Driver With 3-State Outputs

DEVICE STATUS: **ACTIVE**

### FEATURES

[▲ Back to Top](#)

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V  $V_{CC}$
- Distributes One Clock Input to Twelve Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input
- Application for Synchronous DRAM, High-Speed Microprocessor
- TTL-Compatible Inputs and Outputs
- Outputs Drive Parallel 50- Terminated Transmission Lines
- State-of-the-Art EPIC-IIB<sup>TM</sup> BiCMOS Design Significantly Reduces Power Dissipation
- Distributed  $V_{CC}$  and Ground Pins Reduce Switching Noise
- Packaged in 56-Pin Ceramic Flat Package

EPIC-IIB is a trademark of Texas Instruments Incorporated.

### DESCRIPTION

[▲ Back to Top](#)

The SN54CDC586 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with popular microprocessors operating at speeds from 50 MHz to 100 MHz, or down to 25 MHz on outputs configured as half-frequency outputs. The SN54CDC586 operates at 3.3-V  $V_{CC}$  and is designed to drive a properly terminated 50- transmission line.

The feedback input (FBIN) is used to synchronize the output clocks in frequency and phase to CLKIN. One of the 12 output clocks must be fed back to FBIN for the PLL to maintain synchronization between the CLKIN input and the outputs. The output used as the feedback

pin is synchronized to the same frequency as the CLKIN input.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. Select inputs (SEL1, SEL0) configure up to nine Y outputs, in banks of three, to operate at one-half or double the CLKIN frequency, depending on which pin is fed back to FBIN (see Tables 1 and 2). All output-signal duty cycles are adjusted to 50%, independent of the duty cycle at CLKIN.

Output-enable ( $\overline{OE}$ ) is provided for output control. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. When  $\overline{OE}$  is low, the outputs are active.  $\overline{CLR}$  is negative-edge triggered and can be used to reset the outputs operating at half frequency. TEST is used for factory testing of the device and can be used to bypass the PLL. TEST should be strapped to GND for normal operation.

Unlike many products containing PLLs, the SN54CDC586 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the SN54CDC586 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLKIN, as well as following any changes to the PLL reference or feedback signals. Such changes occur upon change of the select inputs, enabling of the PLL via TEST, and upon enable of all outputs via  $\overline{OE}$ .

The SN54CDC586 is characterized for operation over the full military temperature range of -55°C to 125°C.

## detailed description of output configurations

The voltage-controlled oscillator (VCO) used in the SN54CDC586 PLL has a frequency range of 100 MHz to 200 MHz, twice the operating frequency range of the SN54CDC586 outputs. The output of the VCO is divided by two and by four to provide reference frequencies with a 50% duty cycle of one-half and one-fourth the VCO frequency. SEL0 and SEL1 select which of the two signals are buffered to each bank of device outputs.

One device output must be externally wired to FBIN to complete the PLL. The VCO operates such that the frequency and phase of this output match that of CLKIN. In the case in which a VCO/2 output is wired to FBIN, the VCO must operate at twice the CLKIN frequency, resulting in device outputs that operate at either the same or one-half the CLKIN frequency. If a VCO/4 output is wired to FBIN, the device outputs operate at twice or the same frequency as the CLKIN frequency.

### output configuration A

Output configuration A is valid when any output configured as a 1x frequency output in Table

1 is fed back to FBIN. The input frequency range for CLKIN is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at one-half the CLKIN frequency, while outputs configured as 1x outputs operate at the same frequency as CLKIN.

## output configuration B

Output configuration B is valid when any output configured as a 1x frequency output in Table 2 is fed back to FBIN. The input frequency range for CLKIN is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the CLKIN frequency, while outputs configured as 2x outputs operate at double the frequency of CLKIN.

### TECHNICAL DOCUMENTS

[▲ Back to Top](#)

To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

### DATASHEET

[▲ Back to Top](#)

Full datasheet in Acrobat PDF: [sgbs311.pdf](#) (150 KB) (Updated: 02/01/1997)

Full datasheet in Zipped PostScript: [sgbs311.psz](#) (135 KB)

### BLOCK DIAGRAMS

[▲ Back to Top](#)

- [Radar](#)
- [Set Top Box](#)
- [Video Teleconference](#)

### PRICING/AVAILABILITY

[▲ Back to Top](#)

<u>ORDERABLE DEVICE</u>	<u>PACKAGE</u>	<u>PINS</u>	<u>TEMP (°C)</u>	<u>STATUS</u>	<u>BUDGETARY PRICE US\$/UNIT QTY=1000+</u>	<u>PACK QTY</u>	<u>DSCC NUMBER</u>	<u>PRICING/AVAILABILITY</u>
SN54CDC586WD	<u>WD</u>	56	-55 TO 125	ACTIVE	30.39	1		<u>Check stock or order</u>
SNJ54CDC586WD	<u>WD</u>	56	-55 TO 125	ACTIVE	35.75	1	5962-9754001QXA	<u>Check stock or order</u>

Table Data Updated on: 11/19/2000