BURST CellularRAM™

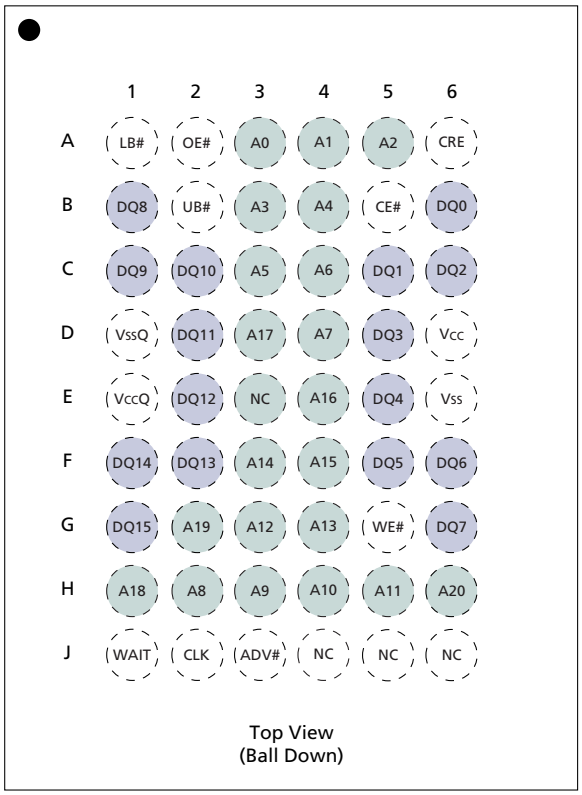
MT45W2MW16BAFB

Features

- Single device supports asynchronous, page, and burst operations
- VCC, VCCQ Voltages
  1.70V–1.95V VCC
  1.70V–2.25V VCCQ (Option W)
  2.30V–2.70V VCCQ (Option V—contact factory)
  2.70V–3.30V VCCQ (Option L—contact factory)
- Random Access Time: 70ns
- Burst Mode Write Access
  Continuous burst
- Burst Mode Read Access
  4, 8, or 16 words, or continuous burst
  MAX clock rate: 104 MHz (^{t}CLK = 9.62ns)
  Burst initial latency: 39ns (4 clocks) @ 104 MHz
  ^{t}ACLK: 6.5ns @ 104 MHz
- Page Mode Read Access
  Sixteen-word page size
  Interpage read access: 70ns
  Intrapage read access: 20ns
- Low Power Consumption
  Asynchronous READ < 25mA
  Intrapage READ < 15mA
  Initial access, burst READ:
  (39ns [4 clocks] @ 104 MHz) < 35mA
  Continuous burst READ < 15mA
  Standby: 90µA Low-power; 110µA Standard
  Deep power-down < 10µA
- Low-Power Features
  Temperature Compensated Refresh (TCR)
  On-Chip Sensor Control
  Partial Array Refresh (PAR)
  Deep Power-Down (DPD) Mode

Options	**Designator**
• Configuration:	
2 Meg x 16	MT45W2Mx16BA
• VCC Core Voltage Supply:	
1.80V – MT45WxMx16BA	W
• VCCQ I/O Voltage	
3.0V – MT45WxML16BA	L[1]
2.5V – MT45WxMV16BA	V[1]
1.8V – MT45WxMW16BA	W
• Package	
54-ball FBGA	FB
54-ball FBGA—Lead-free	BB[1]
• Timing	
60ns access	-60[1]
70ns access	-70
85ns access	-85

Figure 1: Ball Assignment 54-Ball FBGA



See Table 1 on page 6 for ball descriptions, and Figure 44 on page 52 for 54-ball mechanical drawing.

Options (continued)	**Designator**
• Frequency	
66 MHz	6
104 MHz	1[1]
• Standby Power	
Standard	None
Low-power	L
• Operating Temperature Range	
Wireless (-25°C to +85°C)	WT
Industrial (-40°C to +85°C)	IT[1]

NOTE:
1. Contact factory.

Part Number Example:
MT45W2MW16BAFB-706LWT

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General Description

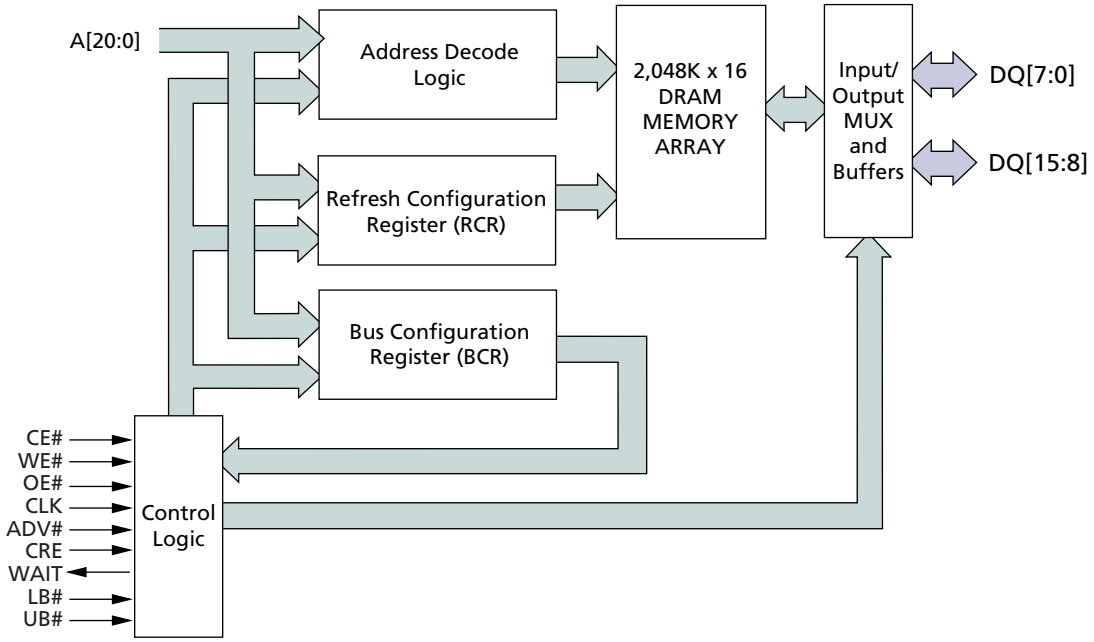
Micron® CellularRAM™ products are high-speed, CMOS dynamic random access memories developed for low-power, portable applications. The MT45W2MW16BA is a 32Mb device organized as 2 Meg x 16 bits. These devices include an industry-standard burst mode Flash interface that dramatically increases read/write bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three system-accessible mechanisms to minimize standby current. Partial array refresh (PAR) limits refresh to only that part of the DRAM array that contains essential data. Temperature compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature. The refresh rate decreases at lower temperatures to minimize current consumption during standby. TCR can also be set by the system for maximum device temperatures of +85°C, +45°C, and +15°C. Deep power-down (DPD) halts the refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the RCR.

Figure 2: Functional Block Diagram—2 Meg x 16



NOTE:

Functional block diagrams illustrate simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.

Table 1: FBGA Ball Descriptions

FBGA ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3, H1, G2, H6	A[20:0]	Input	Address Inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the bus configuration register or the refresh configuration register.
J2	CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static (HIGH or LOW) during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations.
J3	ADV#	Input	Address Valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# can be held LOW during asynchronous READ and WRITE operations.
A6	CRE	Input	Configuration Register Enable: When CRE is HIGH, WRITE operations load the refresh configuration register or bus configuration register.
B5	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode.
A2	OE#	Input	Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
A1	LB#	Input	Lower Byte Enable. DQ[7:0]
B2	UB#	Input	Upper Byte Enable. DQ[15:8]
B6, C5, C6, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	DQ[15:0]	Input/ Output	Data Inputs/Outputs.
J1	WAIT	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is asserted when a burst crosses a row boundary. WAIT is also used to mask the delay associated with opening a new internal page. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH.
E3, J4, J5, J6	NC	–	Not internally connected.
D6	V_{CC}	Supply	Device Power Supply: (1.70V–1.95V) Power supply for device core operation.
E1	V_{CCQ}	Supply	I/O Power Supply: (1.70V–1.95V) Power supply for input/output buffers.
E6	V_{SS}	Supply	V_{SS} must be connected to ground.
D1	V_{SSQ}	Supply	V_{SSQ} must be connected to ground.

NOTE:

The CLK and ADV# inputs can be tied to V_{SS} if the device is always operating in asynchronous or page mode. WAIT will be asserted but should be ignored during asynchronous and page mode operations.

Table 2: Bus Operations—Asynchronous Mode

MODE	POWER	CLK[1]	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[2]	DQ[15:0][3]	NOTES
Read	Active	X	L	L	L	H	L	L	Low-Z	Data-Out	4
Write	Active	X	L	L	X	L	L	L	Low-Z	Data-In	4
Standby	Standby	X	X	H	X	X	L	X	High-Z	High-Z	5, 6
No Operation	Idle	X	X	L	X	X	L	X	Low-Z	X	4, 6
Configuration Register	Active	X	L	L	H	L	H	X	Low-Z	High-Z	
DPD	Deep Power-Down	X	X	H	X	X	X	X	High-Z	High-Z	7

Table 3: Bus Operations—Burst Mode

MODE	POWER	CLK[1]	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[2]	DQ[15:0][3]	NOTES
Async Read	Active	X	L	L	L	H	L	L	Low-Z	Data-Out	4
Async Write	Active	X	L	L	X	L	L	L	Low-Z	Data-In	4
Standby	Standby	X	X	H	X	X	L	X	High-Z	High-Z	5, 6
No Operation	Idle	X	X	L	X	X	L	X	Low-Z	X	4, 6
Initial Burst Read	Active		L	L	X	H	L	L	Low-Z	Data-Out	4, 8
Initial Burst Write	Active		L	L	H	L	L	X	Low-Z	Data-In	4, 8
Burst Continue	Active		H	L	X	X	L	X	Low-Z	Data-In or Data-Out	4, 8
Burst Suspend	Active	X	X	L	H	X	L	X	Low-Z	High-Z	4, 8
Configuration Register	Active		L	L	H	L	H	X	Low-Z	High-Z	8
DPD	Deep Power-Down	X	X	H	X	X	X	X	High-Z	High-Z	7

NOTE:

1. CLK may be HIGH or LOW, but must be static during async read, async write, burst suspend, and DPD modes; and to achieve standby power during standby and active modes.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. V_{IN} = $V_{CC}Q$ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
7. DPD is maintained until RCR is reconfigured.
8. Burst mode operation is initialized through the bus configuration register (BCR[15]).

Table 4: Abbreviated Component Marks— CellularRAM FBGA-Packaged Components

PART NUMBER	ENGINEERING SAMPLE	QUALIFIED SAMPLE
MT45W2MW16BAFB-701 WT	PX408[1]	PW408[1]
MT45W2MW16BAFB-706 WT	PX406	PW406
MT45W2MW16BAFB-856 WT	PX409	PW409

NOTE:
1. Contact factory for availability.

Functional Description

In general, the MT45W2MW16BA device is a high-density alternative to SRAM and Pseudo SRAM products, popular in low-power, portable applications.

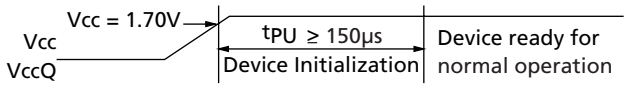
The MT45W2MW16BA contains 33,554,432 bits organized as 2,097,152 addresses by 16 bits. The device implements the same high-speed bus interface found on burst mode Flash products.

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Table 5 on page 17 and Table 8 on page 21). VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.70V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 3: Power-Up Initialization Timing



Bus Operating Modes

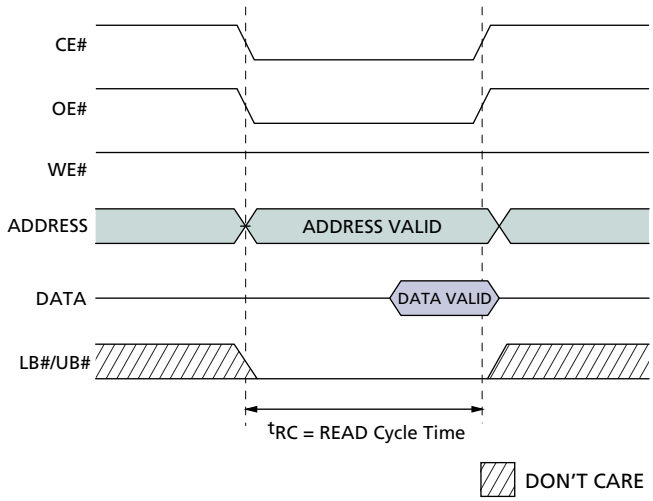
The MT45W2MW16BA CellularRAM product incorporates a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the bus configuration register. Page mode is controlled by the refresh configuration register (RCR[7]).

Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 4) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 5) occur when CE#, WE#, and LB#/UB# are driven LOW. During asynchronous WRITE operations, the OE# level is a "Don't Care," and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV input to latch the address, or ADV can be driven LOW during the entire READ/WRITE operation.

During asynchronous operation, the CLK input must be static (HIGH or LOW—no transition). WAIT will be driven while the device is enabled and its state should be ignored.

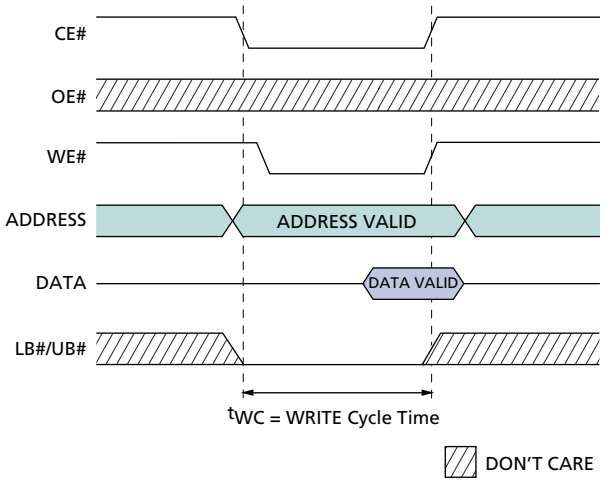
Figure 4: READ Operation (ADV = LOW)



NOTE:

ADV must remain LOW for page mode operation.

Figure 5: WRITE Operation (ADV = LOW)

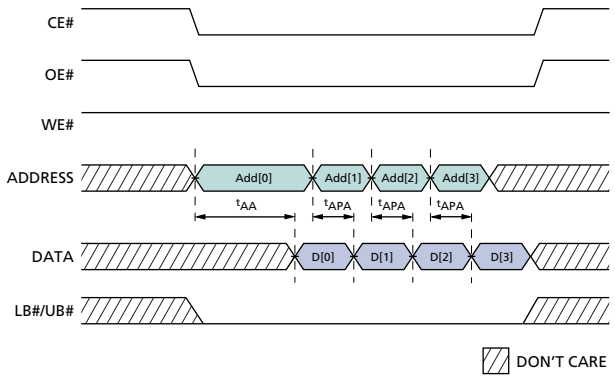


Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Addresses A[4] and higher must remain fixed during the entire page mode access. Figure 6 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be held LOW. CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. WRITE operations do not include comparable page mode functionality. ADV must be driven LOW during all page mode read accesses.

Figure 6: Page Mode READ Operation (ADV = LOW)



Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the next rising edge of CLK that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 7 on page 11) or WRITE (WE# = LOW, Figure 8 on page 11).

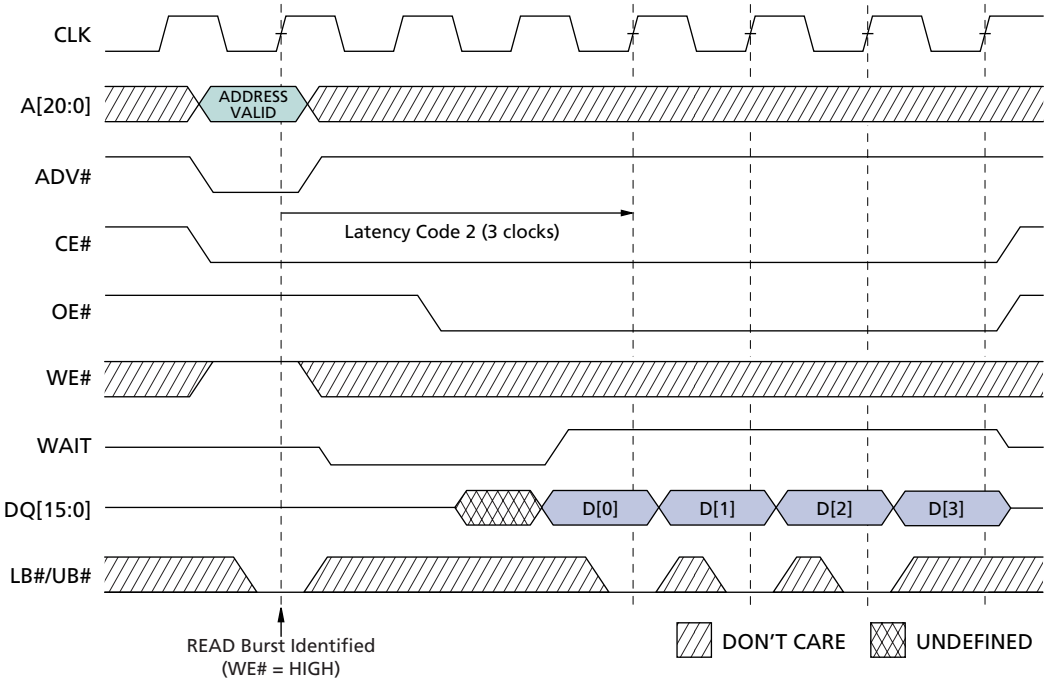
The size of a burst can be specified in the BCR as either a fixed length or continuous. Fixed-length bursts consist of four, eight, or sixteen words. Continuous bursts have the ability to start at a specified address and burst through the entire memory. The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device.

The WAIT output will be asserted as soon as a burst is initiated, and will be de-asserted to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted if the burst crosses a row boundary. Once the CellularRAM device has restored the previous row's data and accessed the next row, WAIT will be de-asserted and the burst can continue (see Figure 30 on page 38).

The processor can access other devices without incurring the timing penalty of the initial latency for a new burst by suspending burst mode. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the CellularRAM outputs; otherwise, OE# can remain LOW. Note that the WAIT output will continue to be active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, then CLK is restarted after valid data is available on the bus.

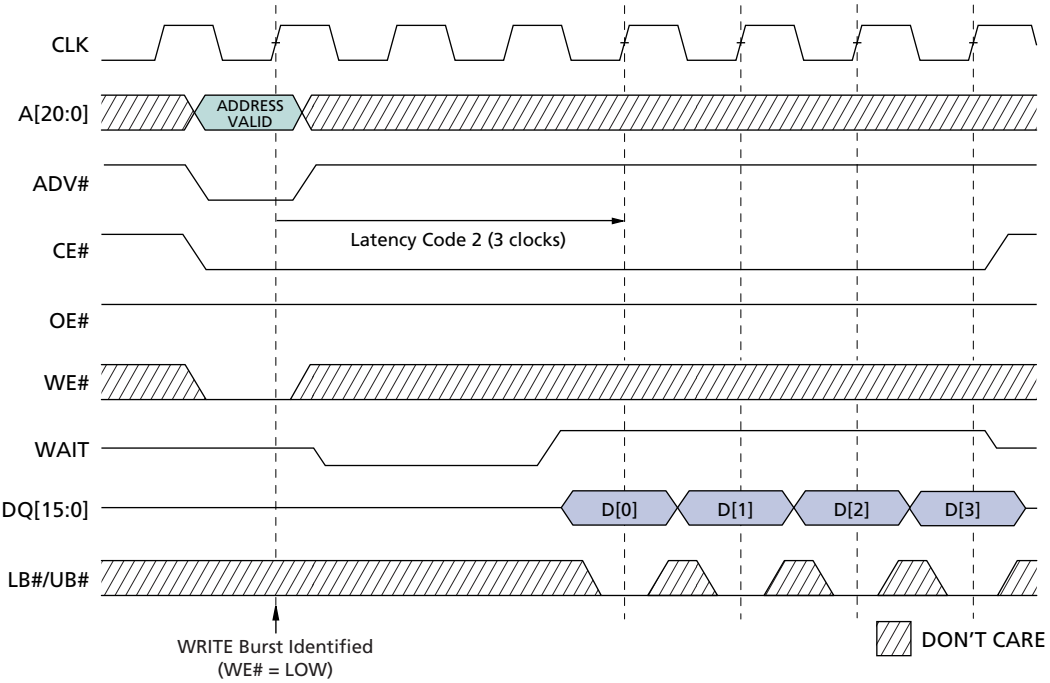
See the APPENDIX A on page 53 for restrictions on the maximum CE# LOW time during burst operations. If a burst suspension will cause CE# to remain LOW for longer than ^{t}CEM, CE# should be taken HIGH and the burst restarted with a new CE# LOW/ADV# LOW cycle.

Figure 7: Burst Mode READ (4-word burst)[1]



NOTE:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

Figure 8: Burst Mode WRITE (4-word burst)[1]



NOTE:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

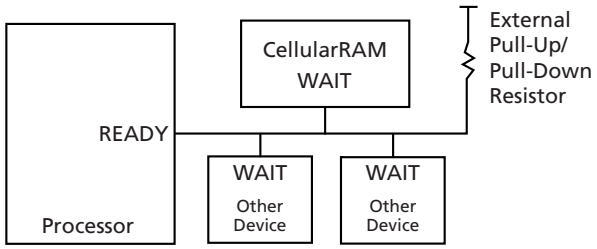
Mixed-Mode Operation

The device can support a combination of synchronous READ and asynchronous WRITE operations when the BCR is configured for synchronous operation. The asynchronous WRITE operation requires that the clock (CLK) remain static (HIGH or LOW) during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire WRITE operation. CE# must return HIGH when transitioning between mixed-mode operations. Note that the ^{t}CKA period is the same as a READ or WRITE cycle. This time is required to ensure adequate refresh. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 38 on page 46 for the "Asynchronous WRITE Followed by Burst READ" timing diagram.

WAIT Operation

The WAIT output on a CellularRAM device is typically connected to a shared, system-level WAIT signal (see Figure 9 below). The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

Figure 9: Wired or WAIT Configuration



Once a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

CE# must remain asserted during WAIT cycles (WAIT asserted and WAIT configuration BCR[8] = 1). Bringing CE# HIGH during WAIT cycles may cause data corruption. (Note that for BCR[8] = 0, the actual WAIT cycles end one cycle after WAIT deasserts, and for row boundary crossings, start one cycle after the WAIT signal asserts.)

The WAIT output also performs an arbitration role when a READ or WRITE operation is launched while an on-chip refresh is in progress. If a collision occurs, the WAIT pin is asserted for additional clock cycles until the refresh has completed (see Figures 10 and 11 on page 13). When the refresh operation has completed, the READ or WRITE operation will continue normally.

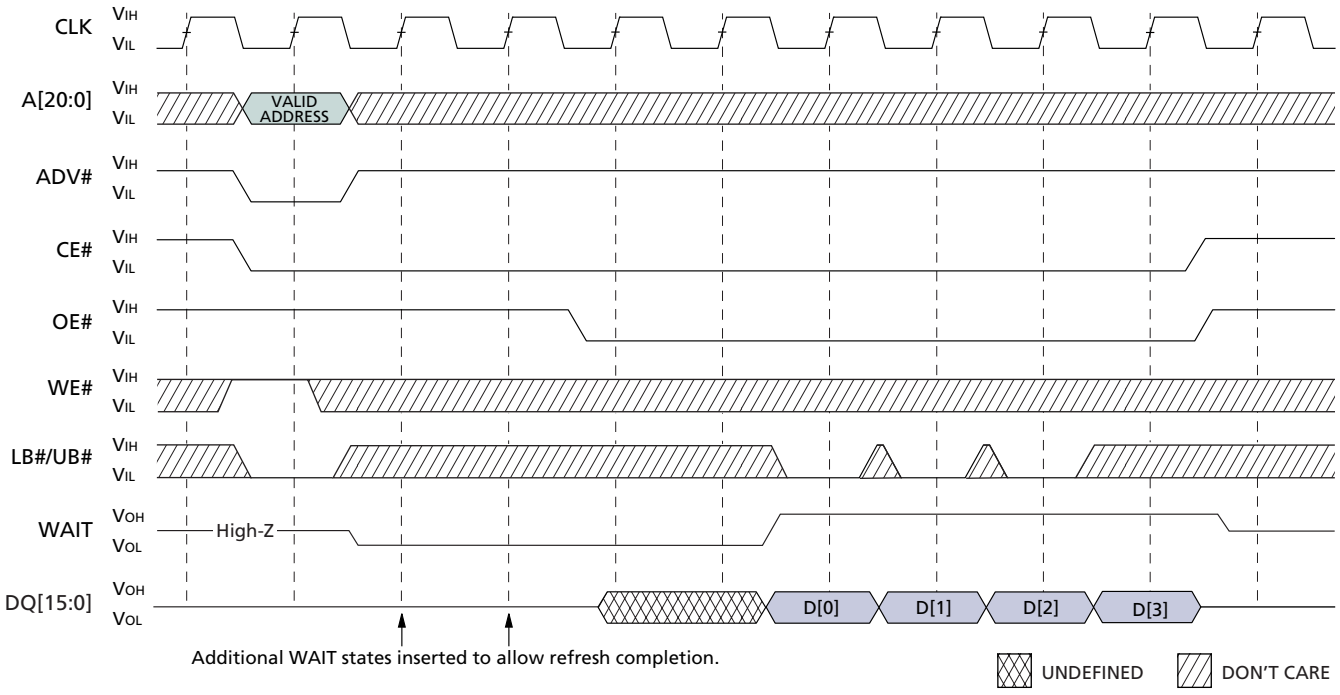
WAIT is also asserted when a continuous READ or WRITE burst crosses a row boundary. The WAIT assertion allows time for the new row to be accessed, and permits any pending refresh operations to be performed.

LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data transfers. During READ operations, the enabled byte(s) are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

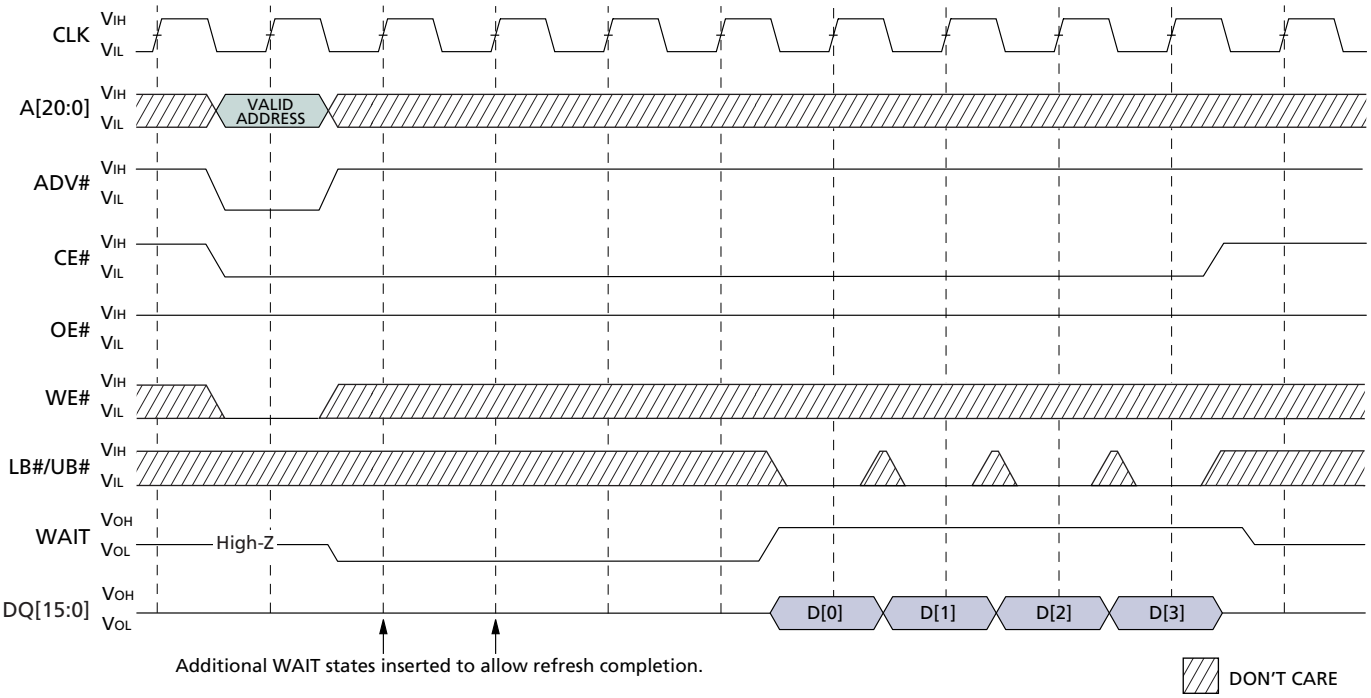
When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

Figure 10: Refresh Collision During READ Operation[1]



NOTE:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

Figure 11: Refresh Collision During WRITE Operation[1]



NOTE:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

Low-Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH.

The device will enter a reduced power state upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature Compensated Refresh

Temperature compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor. When the sensor is enabled, it continually adjusts the refresh rate according to the operating temperature. The on-chip sensor is enabled by default.

Three fixed refresh rates are also available, corresponding to temperature thresholds of +15°C, +45°C, and +85°C. The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +35°C, the system can minimize self-refresh current consumption by selecting the +45°C setting. The +15°C setting would result in inadequate refreshing and cause data corruption.

Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, three-quarters array, one-half array, one-quarter array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 9 on page 22). READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled by rewriting the RCR, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

DPD cannot be enabled or disabled by writing to the RCR using the software access sequence; the RCR should be accessed using CRE instead.

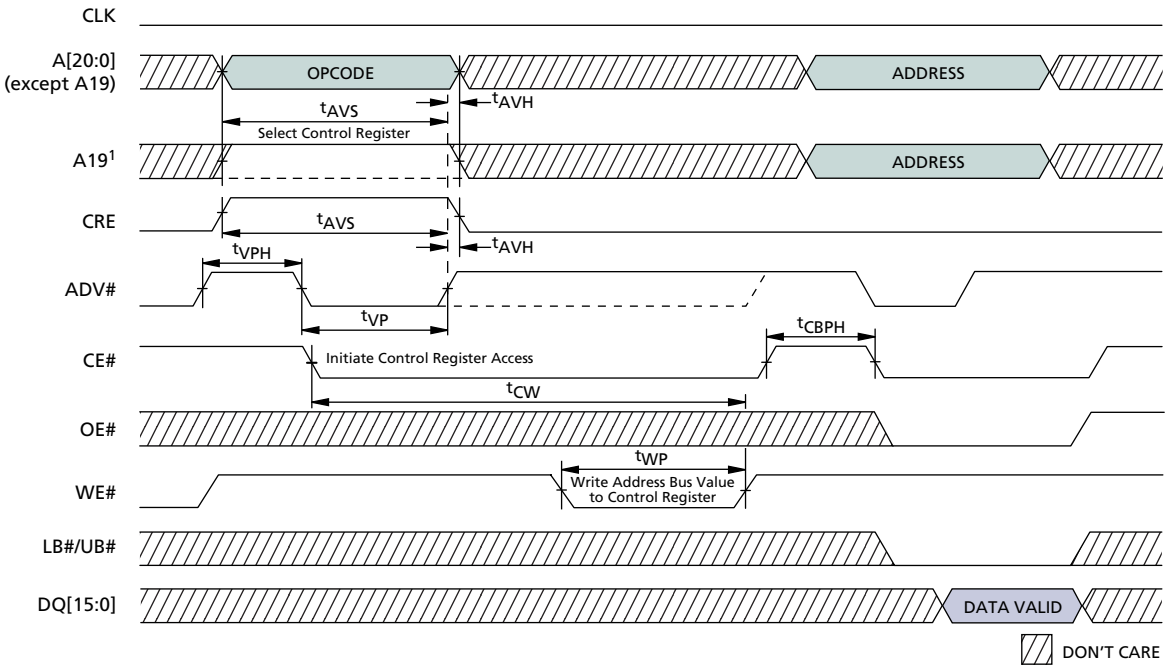
Configuration Registers

Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

Access Using CRE

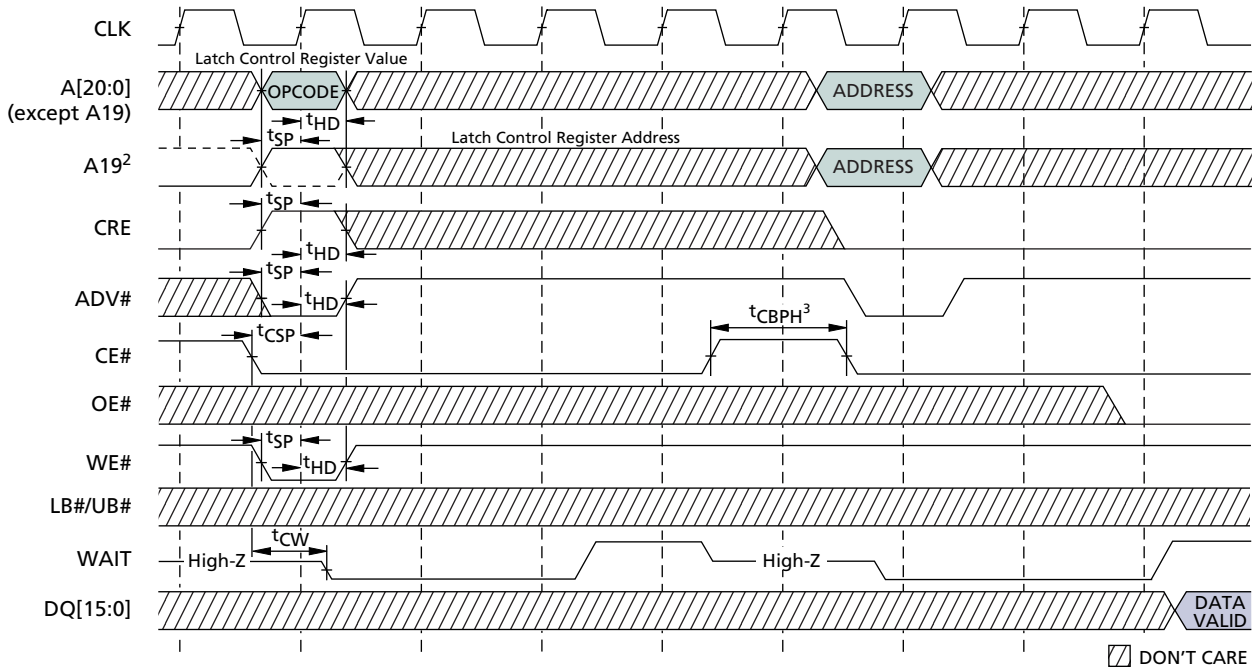
The configuration registers are loaded using either a synchronous or an asynchronous WRITE operation when the configuration register enable (CRE) input is HIGH (see Figures 12 and 13 on page 15). When CRE is LOW, a READ or WRITE operation will access the memory array. The register values are placed on address pins A[20:0]. In an asynchronous WRITE, the values are are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are “Don’t Care.” Access using CRE is WRITE only. The BCR is accessed when A[19] is HIGH; the RCR is accessed when A[19] is LOW.

Figure 12: Configuration Register WRITE in Asynchronous Mode Followed by READ ARRAY Operation



NOTE: 1. A[19] = LOW to load RCR; A[19] = HIGH to load BCR.

Figure 13: Configuration Register WRITE in Synchronous Mode Followed by READ ARRAY Operation[1]



NOTE: 1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19] = LOW to load RCR; A[19] = HIGH to load BCR.
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Software Access

Software access of the configuration registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be read or modified using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 14). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 15). The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (1FFFFFh for 32Mb); the contents of this address are not changed by using this sequence.

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR or the RCR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR. During the fourth operation, the data bus is used to transfer data in to or out of the configuration registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for the control register enable (CRE) pin. If the software mechanism is used, the CRE pin can simply be tied to VSS. The port line often used for CRE control purposes is no longer required.

Software access of the RCR should not be used to enter or exit DPD.

Figure 14: Load Configuration Register

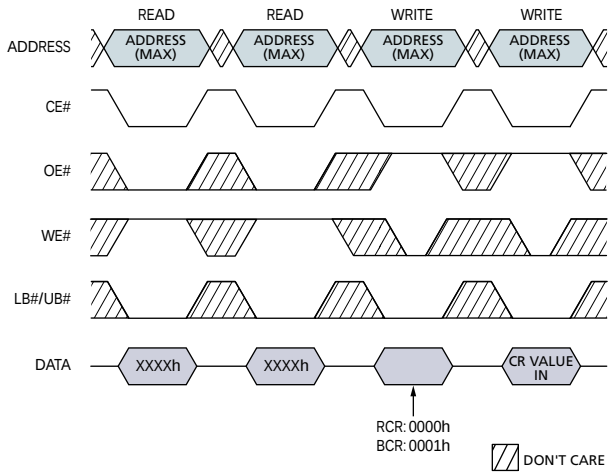
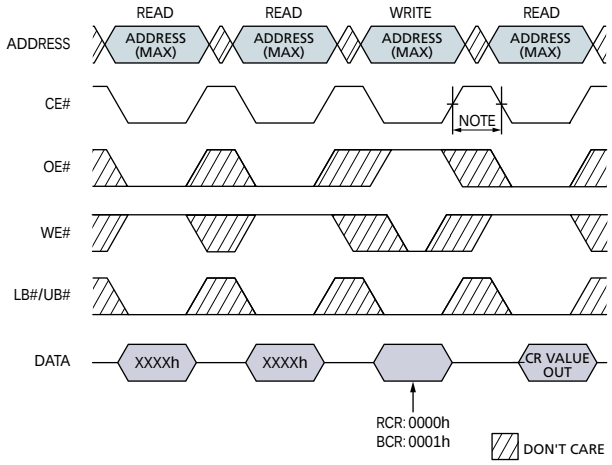


Figure 15: Read Configuration Register



NOTE:

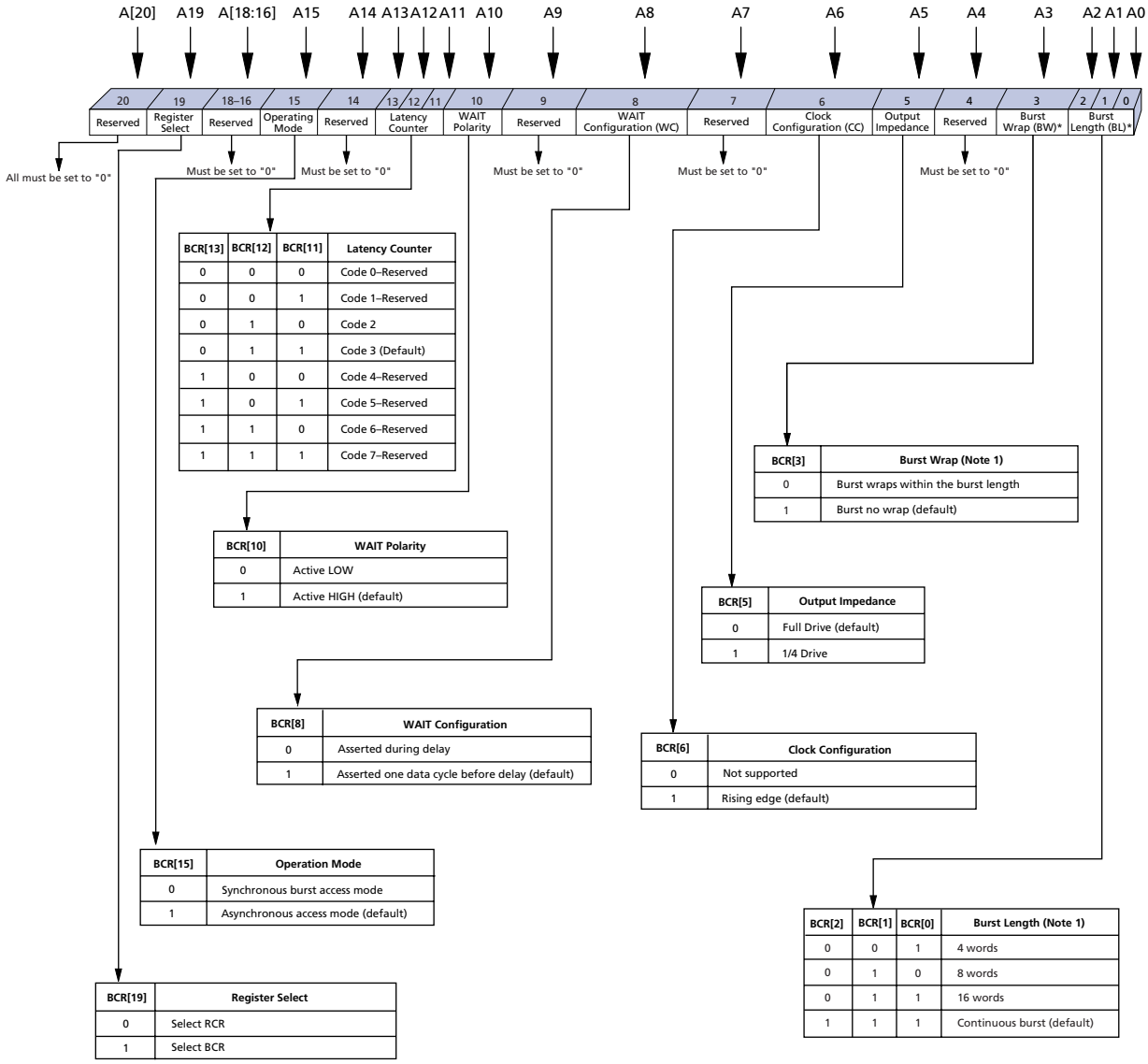
CE# must be HIGH for 150ns before performing the cycle that reads a configuration register.

Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Table 5 on page 17 describes the control bits in the BCR. At power-up, the BCR is set to 9D4Fh.

The BCR is accessed using CRE and A[19] HIGH, or through the configuration register software sequence with DQ = 0001h on the third cycle.

Table 5: Bus Configuration Register Definition



BCR[13]	BCR[12]	BCR[11]	Latency Counter
0	0	0	Code 0–Reserved
0	0	1	Code 1–Reserved
0	1	0	Code 2
0	1	1	Code 3 (Default)
1	0	0	Code 4–Reserved
1	0	1	Code 5–Reserved
1	1	0	Code 6–Reserved
1	1	1	Code 7–Reserved

BCR[3]	Burst Wrap (Note 1)
0	Burst wraps within the burst length
1	Burst no wrap (default)

BCR[10]	WAIT Polarity
0	Active LOW
1	Active HIGH (default)

BCR[5]	Output Impedance
0	Full Drive (default)
1	1/4 Drive

BCR[8]	WAIT Configuration
0	Asserted during delay
1	Asserted one data cycle before delay (default)

BCR[6]	Clock Configuration
0	Not supported
1	Rising edge (default)

BCR[15]	Operation Mode
0	Synchronous burst access mode
1	Asynchronous access mode (default)

BCR[2]	BCR[1]	BCR[0]	Burst Length (Note 1)
0	0	1	4 words
0	1	0	8 words
0	1	1	16 words
1	1	1	Continuous burst (default)

BCR[19]	Register Select
0	Select RCR
1	Select BCR

NOTE:

1. All burst WRITEs are continuous.

Table 6: Sequence and Burst Length

BURST WRAP		STARTING ADDRESS	4-WORD BURST LENGTH	8-WORD BURST LENGTH	16-WORD BURST LENGTH	CONTINUOUS BURST
BCR[3]	WRAP	(DECIMAL)	LINEAR	LINEAR	LINEAR	LINEAR
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-…
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-4-5-6-7-…
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-5-6-7-8-…
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-6-7-8-9-…
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-8-9-10-…
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-8-9-10-11-…
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-9-10-11-12-
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-10-11-12-13-…
		…			…	…
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-17-18-19-20-..
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20-21..
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-…
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-4-5-6-7-…
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-5-6-7-8-…
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-6-7-8-9-…
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-7-8-9-10-…
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-…-15-16-17-18-19-20	5-6-7-8-9-10-11…
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-…-16-17-18-19-20-21	6-7-8-9-10-11-12…
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-…-17-18-19-20-21-22	7-8-9-10-11-12-13…
		…			…	…
		14			14-15-16-17-18-19-…-23-24-25-26-27-28-29	14-15-16-17-18-19-20-…
		15			15-16-17-18-19-20-…-24-25-26-27-28-29-30	15-16-17-18-19-20-21-…

Burst Length (BCR[2:0])
Default = Continuous Burst

Burst lengths define the number of words the device outputs during a burst READ operation. The device supports a burst length of 4, 8, or 16 words. The device can also be set in continuous burst mode where data is output sequentially without regard to address boundaries. WRITE bursts are always performed using continuous burst mode.

Burst Wrap (BCR[3])
Default = Burst No Wrap

The burst wrap option determines if a 4-, 8-, or 16-word burst READ wraps within the burst length or steps through sequential addresses. If the wrap option is not enabled, the device outputs data from sequential addresses without regard to burst boundaries. When continuous burst operation is selected, the internal address wraps to 000000h if the device is read past the last address.

Output Impedance (BCR[5])
Default = Outputs Use Full Drive Strength

The output driver strength can be altered to adjust for different data bus loading scenarios. The reduced-strength option should be more than adequate in stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option is included to minimize noise generated on the data bus during READ operations. Normal output impedance should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Partial drive is approximately one-quarter full drive strength. Outputs are configured at full drive strength during testing.

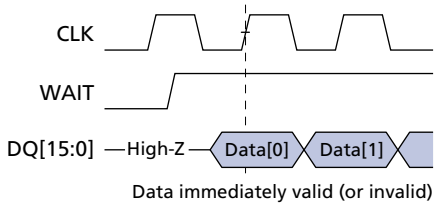
WAIT Configuration (BCR[8])
Default = WAIT Transitions One Clock Before Data Valid/Invalid

The WAIT configuration bit is used to determine when WAIT transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the WAIT signal to coordinate data transfer during synchronous READ and WRITE operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively (Figures 16 and 18). When A8 = 1, the WAIT signal transitions one clock period prior to the data bus going valid or invalid (Figures 17 and 16).

WAIT Polarity (BCR[10])
Default = WAIT Active HIGH

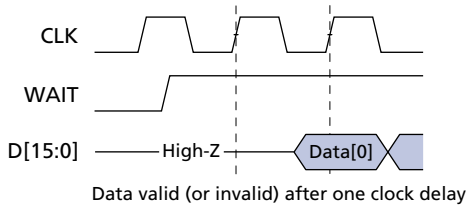
The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

Figure 16: WAIT Configuration (BCR[8] = 0)



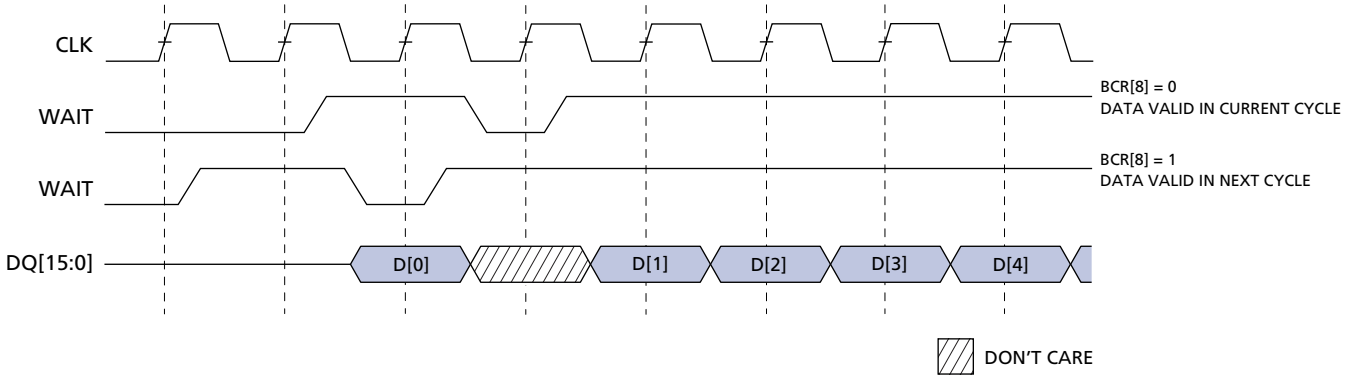
NOTE:
1. Note: Data valid/invalid immediately after WAIT transitions (BCR[8] = 0). See Figure 18.

Figure 17: WAIT Configuration (BCR[8] = 1)



NOTE:
1. Note: Valid/invalid data delayed for one clock after WAIT transitions (BCR[8] = 1). See Figure 18.

Figure 18: WAIT Configuration During Burst Operation[1]



NOTE:
1. Non-default BCR setting: WAIT active LOW.

Latency Counter (BCR[13:11])
Default = Three-Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. Only latency code two (three clocks) or latency code three (four clocks) is allowed (see Table 7 and Figure 19 below).

Operating Mode (BCR[15])
Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

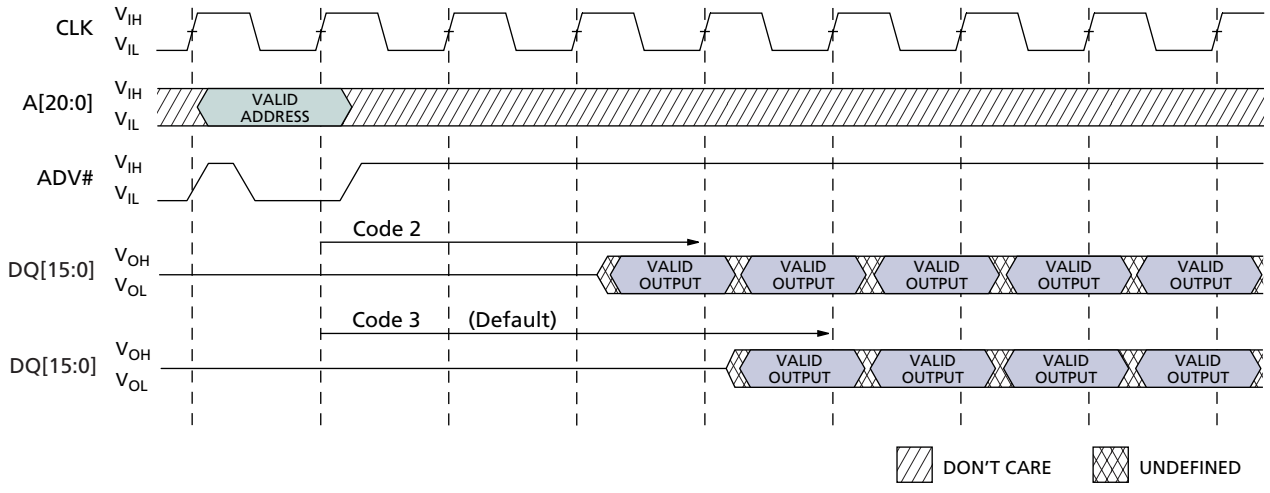
Table 7: Latency Configuration

LATENCY CONFIGURATION CODE	MAX INPUT CLK FREQUENCY (MHz)		
	-701	-706	-856
2 (3 clocks)	66 (15.2ns)	44[1] (22.7ns)	44[1] (22.7ns)
3 (4 clocks) – default	104 (9.62ns)	66 (15.2ns)	66 (15.2ns)

NOTE:

1. Clock rates below 50 MHz are allowed as long as ^{t}CSP specifications are met.

Figure 19: Latency Counter



Refresh Configuration Register

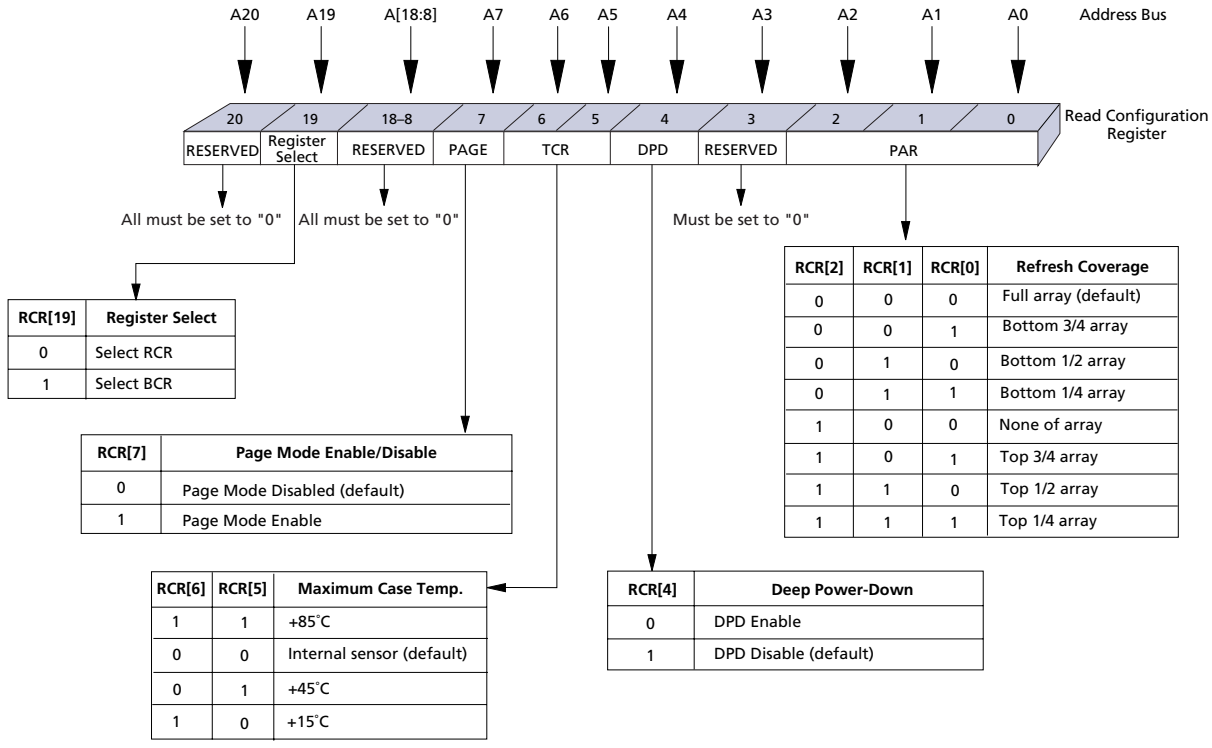
The refresh configuration register (RCR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the RCR. Table 8 below describes the control bits used in the RCR. At power-up, the RCR is set to 0010h.

The RCR is accessed using CRE and A[19] LOW; or through the configuration register software access sequence with DQ = 0000h on the third cycle (see Configuration Registers on page 14.)

Partial Array Refresh (RCR[2:0])
Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, three-quarters array, one-half array, one-quarter array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 9 on page 22.

Table 8: Refresh Configuration Register Mapping



RCR[19]	Register Select
0	Select RCR
1	Select BCR

RCR[7]	Page Mode Enable/Disable
0	Page Mode Disabled (default)
1	Page Mode Enable

RCR[6]	RCR[5]	Maximum Case Temp.
1	1	+85°C
0	0	Internal sensor (default)
0	1	+45°C
1	0	+15°C

RCR[4]	Deep Power-Down
0	DPD Enable
1	DPD Disable (default)

RCR[2]	RCR[1]	RCR[0]	Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 3/4 array
0	1	0	Bottom 1/2 array
0	1	1	Bottom 1/4 array
1	0	0	None of array
1	0	1	Top 3/4 array
1	1	0	Top 1/2 array
1	1	1	Top 1/4 array

Table 9: 32Mb Address Patterns for PAR (RCR[4] = 1)

RCR[2]	RCR[1]	RCR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	0	1	Three-quarters of die	000000h–17FFFFh	1.5 Meg x 16	24Mb
0	1	0	One-half of die	000000h–0FFFFFh	1 Meg x 16	16Mb
0	1	1	One-quarter of die	000000h–07FFFFh	512K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	Three-quarters of die	080000h–1FFFFFh	1.5 Meg x 16	24Mb
1	1	0	One-half of die	100000h–1FFFFFh	1 Meg x 16	16Mb
1	1	1	One-quarter of die	180000h–1FFFFFh	512K x 16	8Mb

Deep Power-Down (RCR[4])
Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume.

Deep power-down is enabled when RCR[4] = 0, and remains enabled until RCR[4] is set to "1." DPD should not be enabled or disabled with the software access sequence; instead, use CRE to access the RCR.

Temperature Compensated Refresh (RCR[6:5])
Default = On-Chip Temperature Sensor

This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The on-chip TCR is enabled by clearing both of the TCR bits in the refresh configuration register (RCR[6:5] = 00b). Any other TCR setting enables a fixed refresh rate. When the on-chip temperature sensor is enabled, the device continually adjusts the refresh rate according to the operating temperature.

The TCR bits also allow for adequate fixed-rate refresh at three different temperature thresholds (+15°C, +45°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +35°C, the system can minimize self refresh current consumption by selecting the +45°C setting. The +15°C setting would result in inadequate refreshing and cause data corruption.

Page Mode Operation (RCR[7])
Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous READ operations. In the power-up default state, page mode is disabled.

Absolute Maximum Ratings*

Voltage to Any Ball Except V_{CC}, V_{CCQ}
Relative to V_{SS} . . . . . .
. . . -0.50V to (4.0V or V_{CCQ} + 0.3V, whichever is less)
Voltage on V_{CC} Supply Relative to V_{SS}. . -0.2V to +2.45V
Voltage on V_{CCQ} Supply Relative to V_{SS} . -0.2V to +4.0V
Storage Temperature (plastic). . . . . -55°C to +150°C
Operating Temperature (case)
Wireless. . . . . -25°C to +85°C
Industrial . . . . . -40°C to +85°C
Soldering Temperature and Time
10s (lead only) . . . . . +260°C

*Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 10: Electrical Characteristics and Operating Conditions

Wireless Temperature (-25°C < T_C < +85°C); Industrial Temperature (-40°C < T_C < +85°C)

DESCRIPTION	CONDITIONS	SYMBOL		MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}		1.70	1.95	V	
I/O Supply Voltage		V_{CCQ}	W: 1.8V	1.70	2.25	V	
			V: 2.5V	2.30	2.70	V	
			L: 3.0V	2.70	3.30	V	
Input High Voltage		V_{IH}		1.40	V_{CCQ} + 0.2	V	1
Input Low Voltage		V_{IL}		-0.20	0.4	V	2
Output High Voltage	I_{OH} = -0.2mA	V_{OH}		0.80 V_{CCQ}		V	3
Output Low Voltage	I_{OL} = +0.2mA	V_{OL}			0.20 V_{CCQ}	V	3
Input Leakage Current	V_{IN} = 0 to V_{CCQ}	I_{LI}			1	µA	
Output Leakage Current	OE# = V_{IH} or Chip Disabled	I_{LO}			1	µA	
Operating Current							
Asynchronous Random READ	V_{IN} = V_{CCQ} or 0V Chip Enabled, I_{OUT} = 0	I_{CC1}	-70		25	mA	4
			-85		20		
Asynchronous Page READ			-70		15		
			-85		12		
Initial Access, Burst READ	V_{IN} = V_{CCQ} or 0V Chip Enabled, I_{OUT} = 0	I_{CC1}	104 MHz		35	mA	4
			66 MHz		30		
Continuous Burst READ			104 MHz		11		
			66 MHz		11		
WRITE Operating Current	V_{IN} = V_{CCQ} or 0V Chip Enabled	I_{CC2}	-70		25	mA	
			-85		20		
Standby Current	V_{IN} = V_{CCQ} or 0V CE# = V_{CCQ}	I_{SB}	Standard		110	µA	5
			Low-Power (L)		90		

NOTE:

1. Input signals may overshoot to VccQ + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to Vss - 1.0V for periods less than 2ns during transitions.
3. BCR[5:4] = 00b.
4. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
5. I_{SB} (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C. In order to achieve low standby current, all inputs must be driven to either V_{CCQ} or V_{SS}.

Table 11: Temperature Compensated Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	POWER	MAX CASE TEMPERATURE SETTING (RCR[6:5])	MAX	UNITS
Temperature Compensated Refresh Standby Current	V_{IN} = V_{CCQ} or 0V CE# = V_{CCQ}	I_{TCR}	Standard Power (no desig.)	+85°C	110	µA
				+45°C	TBD	
				+15°C	TBD	
			Low-Power Option (L)	+85°C	90	µA
				+45°C	TBD	
				+15°C	TBD	

NOTE:

I_{TCR} (MAX) values measured with PAR set to FULL ARRAY.

Table 12: Partial Array Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	POWER	ARRAY PARTITION	MAX	UNITS
Partial Array Refresh Standby Current	V_{IN} = V_{CCQ} or 0V, CE# = V_{CCQ}	I_{PAR}	Standard Power (no desig.)	Full	110	µA
				3/4	TBD	
				1/2	TBD	
				1/4	TBD	
				0	TBD	
			Low-Power Option (L)	Full	90	µA
				3/4	TBD	
				1/2	TBD	
				1/4	TBD	
				0	TBD	

NOTE:

I_{PAR} (MAX) values measured with TCR set to 85°C.

Table 13: Deep Power-Down Specifications

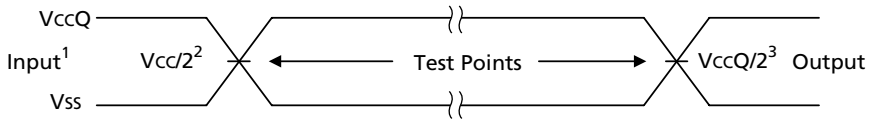
DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS
Deep Power-Down	V_{IN} = V_{CCQ} or 0V; +25°C	Izz	10	µA

Table 14: Capacitance

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_C = +25°C; f = 1 MHz; V_{IN} = 0V	C_{IN}	–	6	pF	1
Input/Output Capacitance (DQ)		C_{IO}	–	6	pF	1

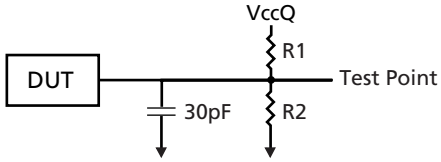
NOTE:
1. These parameters are verified in device characterization and are not 100% tested.

Figure 20: AC Input/Output Reference Waveform



NOTE:
1. AC test inputs are driven at V_{CCQ} for a logic 1 and V_{SS} for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at $V_{CC}/2$. Due to the possibility of a difference between V_{CC} and V_{CCQ}, the input test point may not be shown to scale.
3. Output timing ends at $V_{CCQ}/2$.

Figure 21: Output Load Circuit



NOTE:
All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).

Table 15: Output Load Circuit

VccQ	R1/R2
1.8V	2.7K Ω
2.5V	3.7K Ω
3.0V	4.5K Ω

Table 16: Asynchronous READ Cycle Timing Requirements[1]

PARAMETER	SYMBOL	-701, -706		-856		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Access Time	^tAA		70		85	ns	
ADV# Access Time	^tAADV		70		85	ns	
Page Access Time	^tAPA		20		25	ns	
Address Hold from ADV# HIGH	^tAVH	5		5		ns	
Address Setup to ADV# HIGH	^tAVS	10		10		ns	
LB#/UB# Access Time	^tBA		70		85	ns	
LB#/UB# Disable to DQ High-Z Output	^tBHZ		8		8	ns	4
LB#/UB# Enable to Low-Z Output	^tBLZ	10		10		ns	3
CE# HIGH between Subsequent Mixed-Mode Operations	^tCBPH	5		5		ns	
Maximum CE# Pulse Width	^tCEM		10		10	µs	2
CE# LOW to WAIT Valid	^tCEW	1	7.5	1	7.5	ns	
Chip Select Access Time	^tCO		70		85	ns	
CE# LOW to ADV# HIGH	^tCVS	10		10		ns	
Chip Disable to DQ and WAIT High-Z Output	^tHZ		8		8	ns	4
Chip Enable to Low-Z Output	^tLZ	10		10		ns	3
Output Enable to Valid Output	^tOE		20		20	ns	
Output Hold from Address Change	^tOH	5		5		ns	
Output Disable to DQ High-Z Output	^tOHZ		8		8	ns	4
Output Enable to Low-Z Output	^tOLZ	5		5		ns	3
Page Cycle Time	^tPC	20		25		ns	
READ Cycle Time	^tRC	70		85		ns	
ADV# Pulse Width LOW	^tVP	10		10		ns	
ADV# Pulse Width HIGH	^tVPH	10		10		ns	

NOTE:

1. All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).
2. See the Appendix at the end of this data sheet.
3. High-Z to Low-Z timings are tested with the circuit shown in Figure 21 on page 25. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ}/2$) level toward either V_{OH} or V_{OL}.
4. Low-Z to High-Z timings are tested with the circuit shown in Figure 21 on page 25. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CCQ}/2$.

Table 17: Burst READ Cycle Timing Requirements[1]

PARAMETER	SYMBOL	-701		-706, -856		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Burst to READ Access Time	^{t}ABA		35		55	ns	
CLK to Output Delay	$^{t}ACLK$		6.5		10	ns	
Burst OE# LOW to Output Delay	^{t}BOE		20		20	ns	
CE# HIGH between Subsequent Mixed-Mode Operations	$^{t}CBPH$	5		5		ns	
CE# LOW to WAIT Valid	^{t}CEW	1	7.5	1	7.5	ns	
CLK Period	^{t}CLK	9.62	20	15	20	ns	4
CE# Setup Time to Active CLK Edge	^{t}CSP	4	20	5	20	ns	
Hold Time from Active CLK Edge	^{t}HD	2		2		ns	
Chip Disable to DQ and WAIT High-Z Output	^{t}HZ		8		8	ns	2
CLK Rise or Fall Time	$^{t}KHKL$		1.6		1.6	ns	
CLK to WAIT Valid	$^{t}KHTL$		6.5		10	ns	
CLK to DQ High-Z Output	^{t}KHZ	3	8	3	8	ns	
CLK to Low-Z Output	^{t}KLZ	2	5	2	5	ns	
Output HOLD from CLK	^{t}KOH	2		2		ns	
CLK HIGH or LOW Time	^{t}KP	3		3		ns	
Output Disable to DQ High-Z Output	^{t}OHZ		8		8	ns	2
Output Enable to Low-Z Output	^{t}OLZ	5		5		ns	3
Setup Time to Active CLK Edge	^{t}SP	3		3		ns	

NOTE:

1. All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 21 on page 25. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CCQ}/2$.
3. High-Z to Low-Z timings are tested with the circuit shown in Figure 21 on page 25. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ}/2$) level toward either V_{OH} or V_{OL}.
4. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 18: Asynchronous WRITE Cycle Timing Requirements

PARAMETER	SYMBOL	-701, -706		-856		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address and ADV# LOW Setup Time	^{t}AS	0		0		ns	
Address Hold from ADV# Going HIGH	^{t}AVH	5		5		ns	
Address Setup to ADV# Going HIGH	^{t}AVS	10		10		ns	
Address Valid to End of Write	^{t}AW	70		85		ns	
LB#/UB# Select to End of Write	^{t}BW	70		85		ns	
Maximum CE# Pulse Width	^{t}CEM		10		10	µs	1
CE# LOW to WAIT Valid	^{t}CEW	1	7.5	1	7.5	ns	
Async Address-to-Burst Transition Time	^{t}CKA	70		85		ns	
CE# Low to ADV# HIGH	^{t}CVS	10		10		ns	
Chip Enable to End of Write	^{t}CW	70		85		ns	
Data Hold from Write Time	^{t}DH	0		0		ns	
Data WRITE Setup Time	^{t}DW	23		23		ns	1
Chip Disable to WAIT High-Z Output	^{t}HZ		8		8	ns	
Chip Enable to Low-Z Output	^{t}LZ	10		10		ns	3
End WRITE to Low-Z Output	^{t}OW	5		5		ns	3
ADV# Pulse Width	^{t}VP	10		10		ns	
ADV# Pulse Width HIGH	^{t}VPH	10		10		ns	
ADV# Setup to End of WRITE	^{t}VS	70		85		ns	
WRITE Cycle Time	^{t}WC	70		85		ns	
WRITE to DQ High-Z Output	^{t}WHZ		8		8	ns	2
WRITE Pulse Width	^{t}WP	46		55		ns	1
WRITE Pulse Width HIGH	^{t}WPH	10		10		ns	
WRITE Recovery Time	^{t}WR	0		0		ns	

NOTE:

1. See the Appendix at the end of this data sheet.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 21 on page 25. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CCQ}/2$.
3. High-Z to Low-Z timings are tested with the circuit shown in Figure 21 on page 25. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ}/2$) level toward either V_{OH} or V_{OL}.

Table 19: Burst WRITE Cycle Timing Requirements

PARAMETER	SYMBOL	-701		-706, -856		UNITS	NOTES
		MIN	MAX	MIN	MAX		
CE# HIGH between Subsequent Mixed-Mode Operations	$^{t}CBPH$	5		5		ns	
CE# LOW to WAIT Valid	^{t}CEW	1	7.5	1	7.5	ns	
Clock Period	^{t}CLK	9.62	20	15	20	ns	1
CE# Setup to CLK Active Edge	^{t}CSP	4	20	5	20	ns	
Hold Time from Active CLK Edge	^{t}HD	2		2		ns	
Chip Disable to WAIT High-Z Output	^{t}HZ		8		8	ns	
CLK Rise or Fall Time	$^{t}KHKL$		1.6		1.6	ns	
Clock to WAIT Valid	$^{t}KHTL$		6.5		10	ns	
CLK HIGH or LOW Time	^{t}KP	3		3		ns	
Setup Time to Activate CLK Edge	^{t}SP	3		3		ns	

NOTE:

1. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

TIMING DIAGRAMS

Figure 22: Initialization Period

Table 20: Initialization Timing Parameters

PARAMETER	SYMBOL	-701, -706		-856		UNITS	NOTE
		MIN	MAX	MIN	MAX		
Initialization Period (required before normal operations)	t_{PU}		150		150	µs	

Figure 23: Asynchronous READ

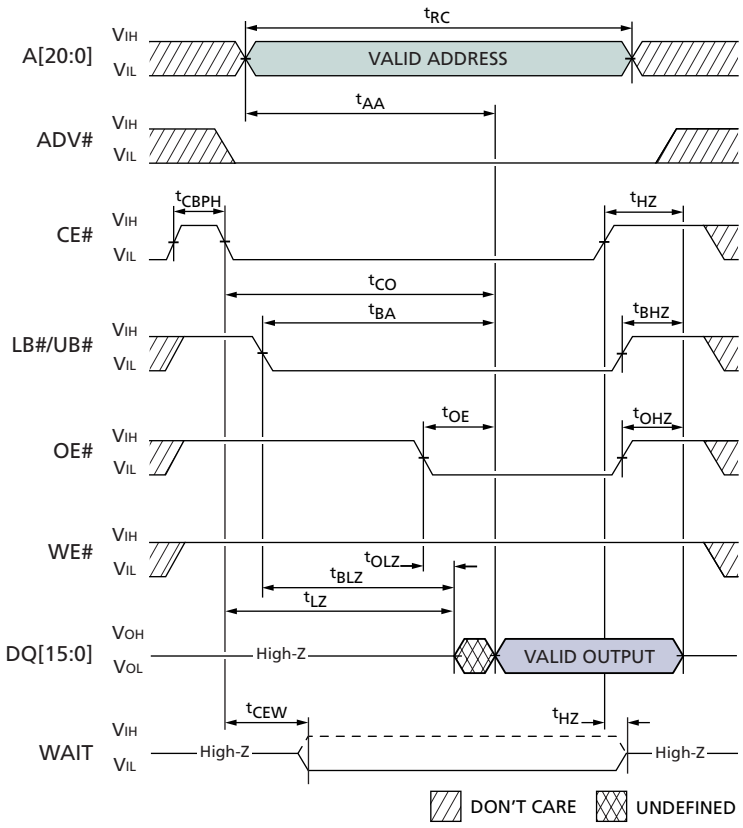


Table 21: Asynchronous READ Timing Parameters

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^tAA		70		85	ns
^tBA		70		85	ns
^tBHZ		8		8	ns
^tBLZ	10		10		ns
^tCBPH	5		5		ns
^tCEW	1	7.5	1	7.5	ns
^tCO		70		85	ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^tHZ		8		8	ns
^tLZ	10		10		ns
^tOE		20		20	ns
^tOHZ		8		8	ns
^tOLZ	5		5		ns
^tRC	70		85		ns

Figure 24: Asynchronous READ Using ADV#

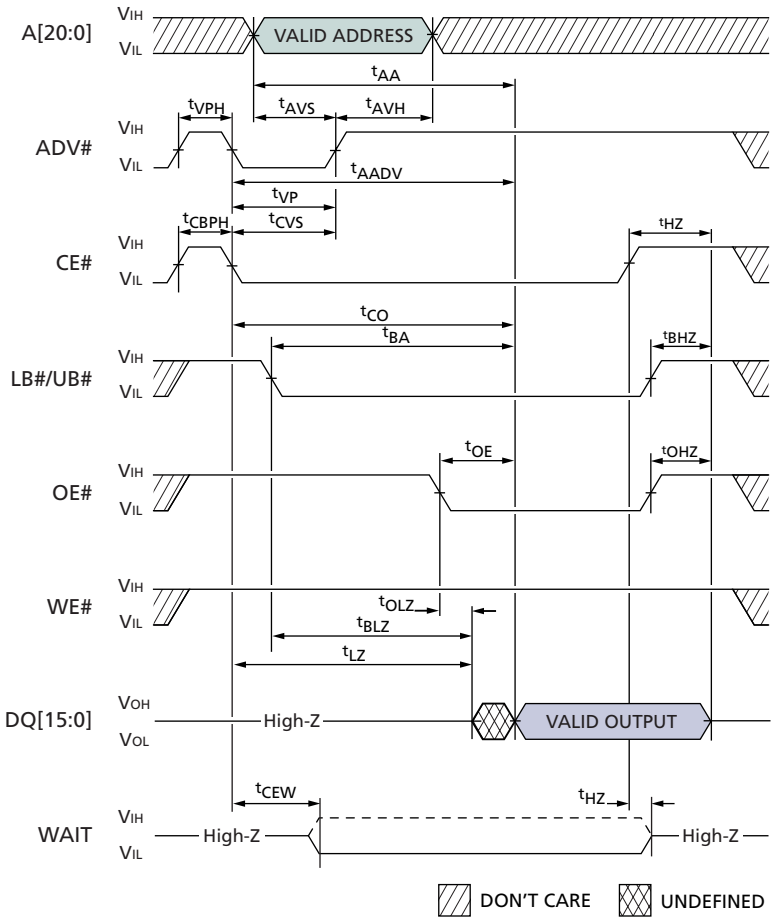


Table 22: Asynchronous READ Timing Parameters Using ADV#

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}AA		70		85	ns
$^{t}AADV$		70		85	ns
^{t}AVH	5		5		ns
^{t}AVS	10		10		ns
^{t}BA		70		85	ns
^{t}BHZ		8		8	ns
^{t}BLZ	10		10		ns
$^{t}CBPH$	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}CO		70		85	ns
^{t}CVS	10		10		ns
^{t}HZ		8		8	ns
^{t}LZ	10		10		ns
^{t}OE		20		20	ns
^{t}OHZ		8		8	ns
^{t}OLZ	5		5		ns
^{t}VP	10		10		ns
^{t}VPH	10		10		ns

Figure 25: Page Mode READ

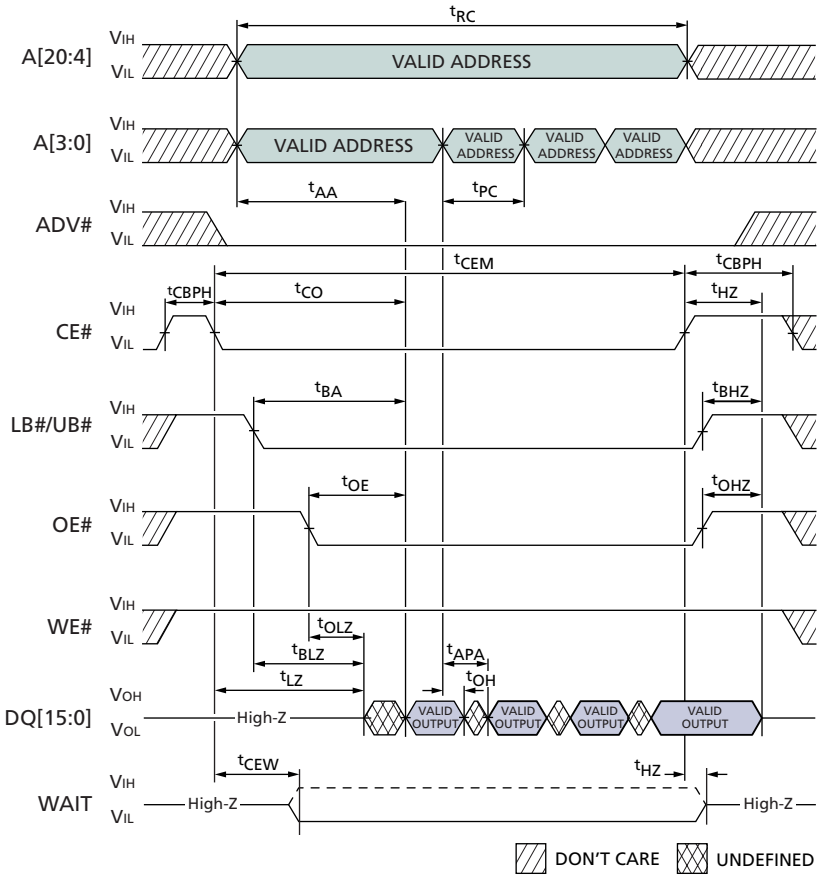
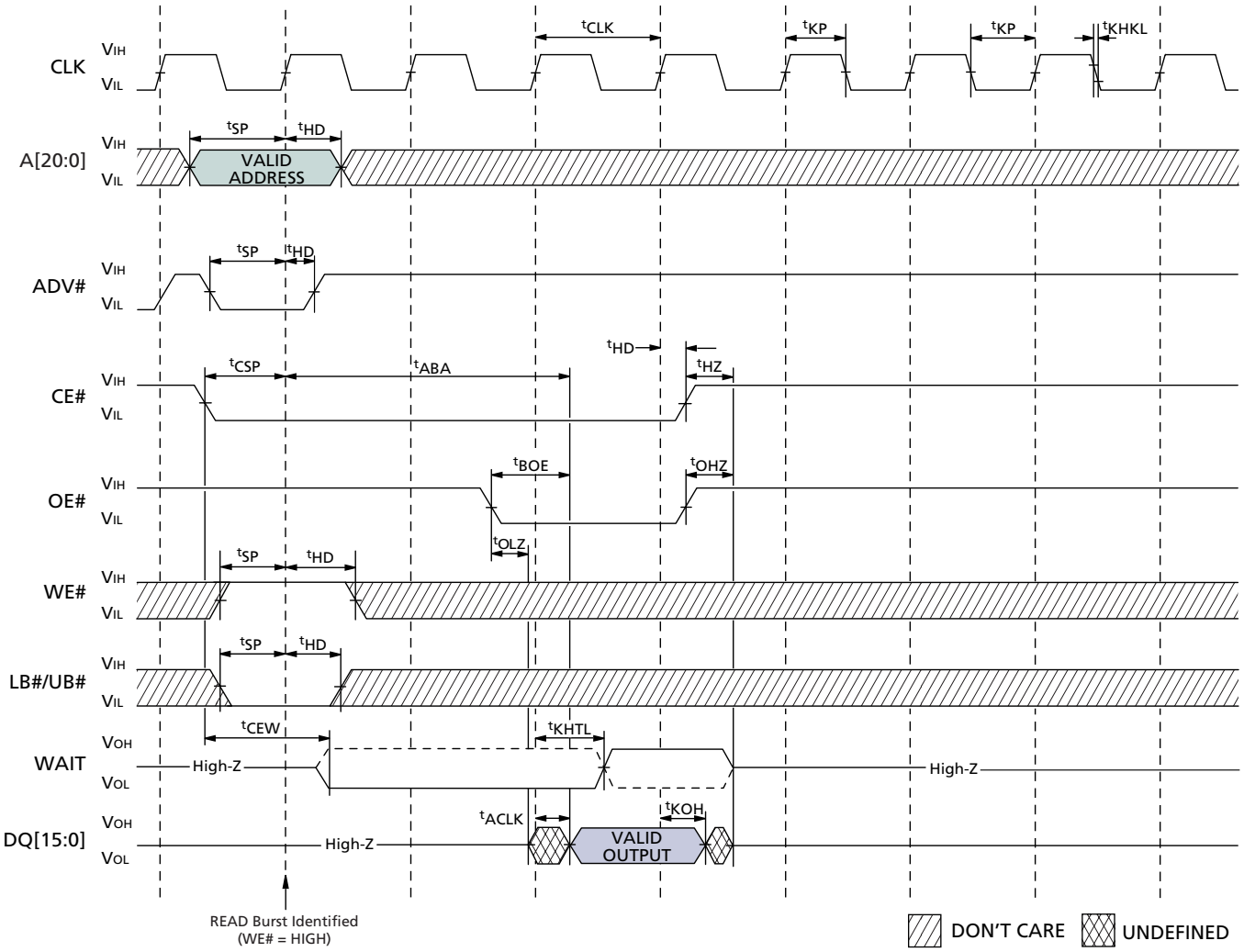


Table 23: Asynchronous READ Timing Parameters—Page Mode Operation

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		70		85	ns
t_{APA}		20		25	ns
t_{BA}		70		85	ns
t_{BHZ}		8		8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEM}		10		10	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CO}		70		85	ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OH}	5		5		ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns
t_{PC}	20		25		ns
t_{RC}	70		85		ns

Figure 26: Single-Access Burst READ Operation[1]



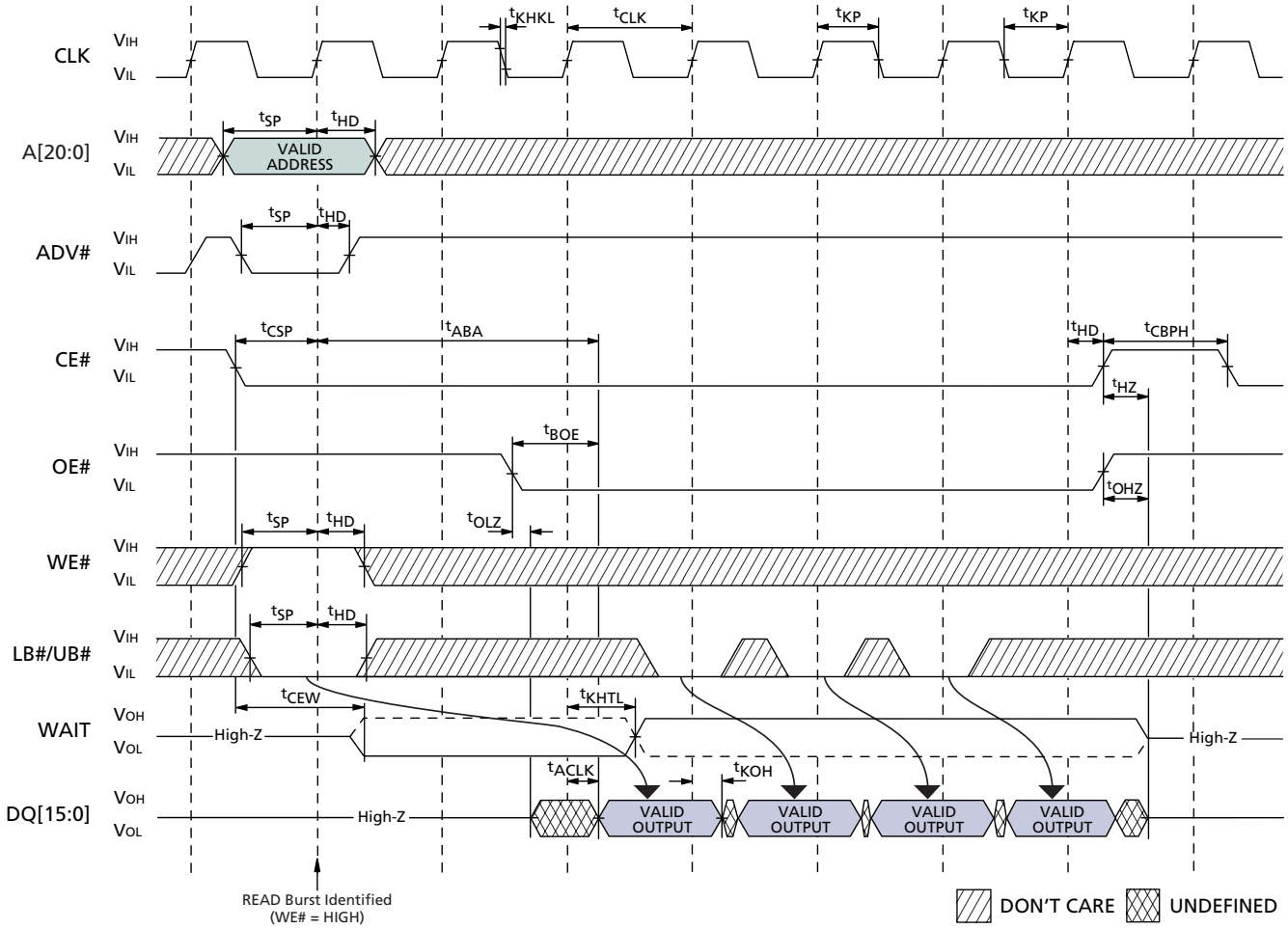
NOTE:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 24: Burst READ Timing Parameters—Single Access

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}ABA		35		55	ns
^{t}ACLK		6.5		10	ns
^{t}BOE		20		20	ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	5	20	ns
^{t}HD	2		2		ns
^{t}HZ		8		8	ns

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}KHKL		1.6		1.6	ns
^{t}KHTL		6.5		10	ns
^{t}KOH	2		2		ns
^{t}KP	3		3		ns
^{t}OHZ		8		8	ns
^{t}OLZ	5		5		ns
^{t}SP	3		3		ns

Figure 27: 4-Word Burst READ Operation[1]



NOTE:

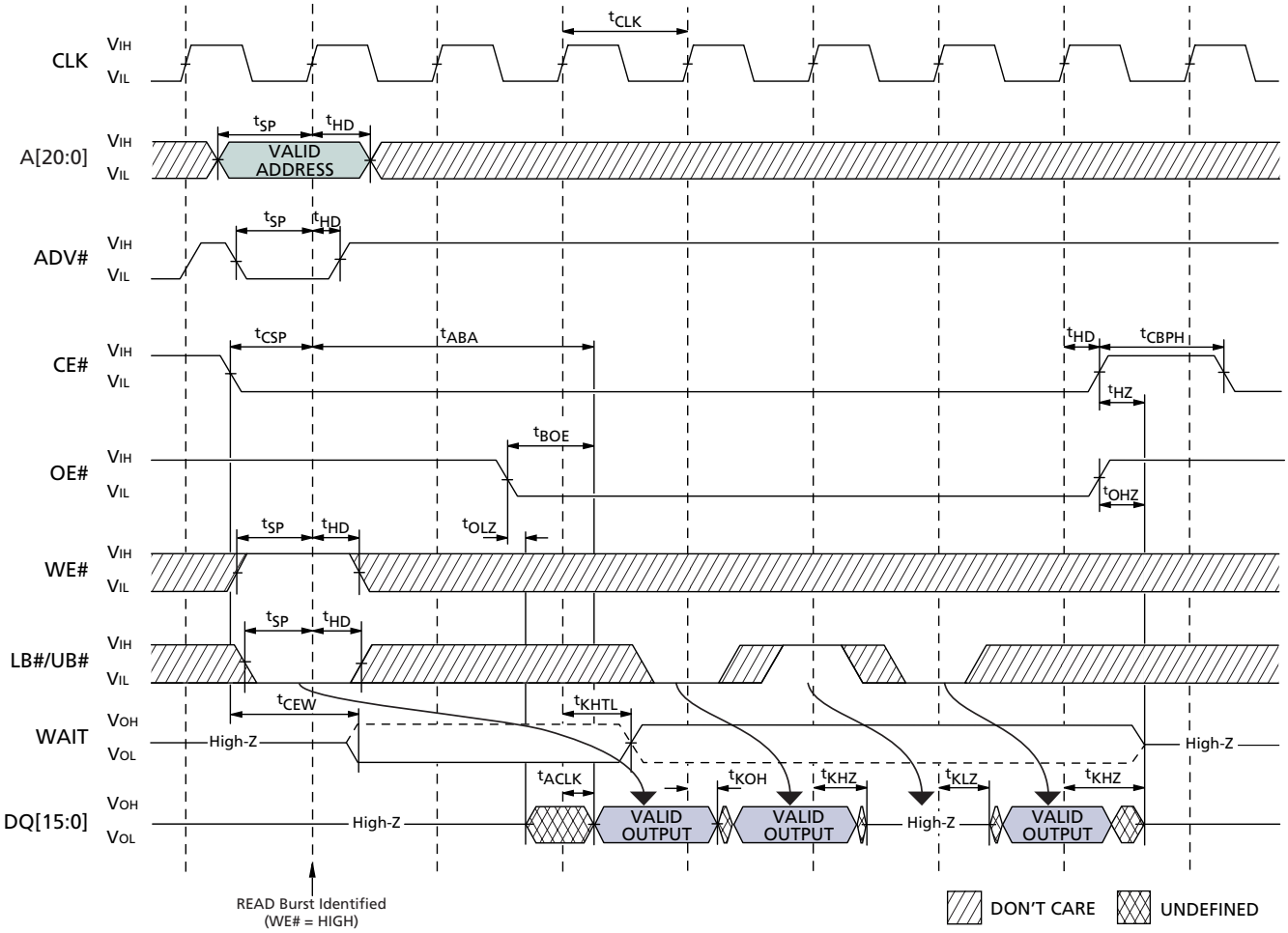
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 25: Burst READ Timing Parameters—4-Word Burst

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}ABA		35		55	ns
^{t}ACLK		6.5		10	ns
^{t}BOE		20		20	ns
^{t}CBPH	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	5	20	ns
^{t}HD	2		2		ns

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}HZ		8		8	ns
^{t}KHKL		1.6		1.6	ns
^{t}KHTL		6.5		10	ns
^{t}KOH	2		2		ns
^{t}KP	3		3		ns
^{t}OHZ		8		8	ns
^{t}OLZ	5		5		ns
^{t}SP	3		3		ns

Figure 28: 4-Word Burst READ Operation (with LB#/UB#)[1]



NOTE:

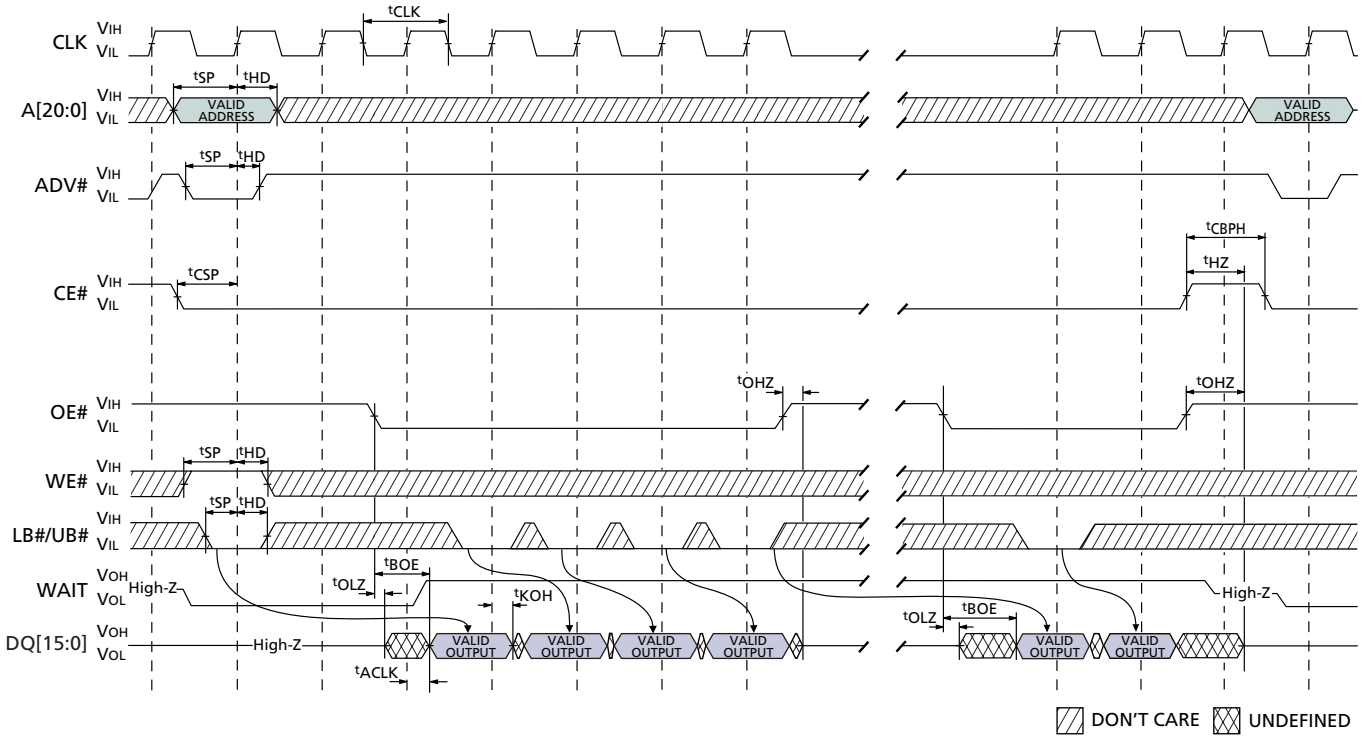
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met. BCR configured with a burst length of four.

Table 26: Burst READ Timing Parameters—4-Word Burst with LB#/UB#

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}ABA		35		55	ns
^{t}ACLK		6.5		10	ns
^{t}BOE		20		20	ns
^{t}CBPH	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	5	20	ns
^{t}HD	2		2		ns

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}HZ		8		8	ns
^{t}KHTL		6.5		10	ns
^{t}KHZ	3	8	3	8	ns
^{t}KLZ	2	5	2	5	ns
^{t}KOH	2		2		ns
^{t}OHZ		8		8	ns
^{t}OLZ	5		5		ns
^{t}SP	3		3		ns

Figure 29: READ Burst Suspend[1]



NOTE:

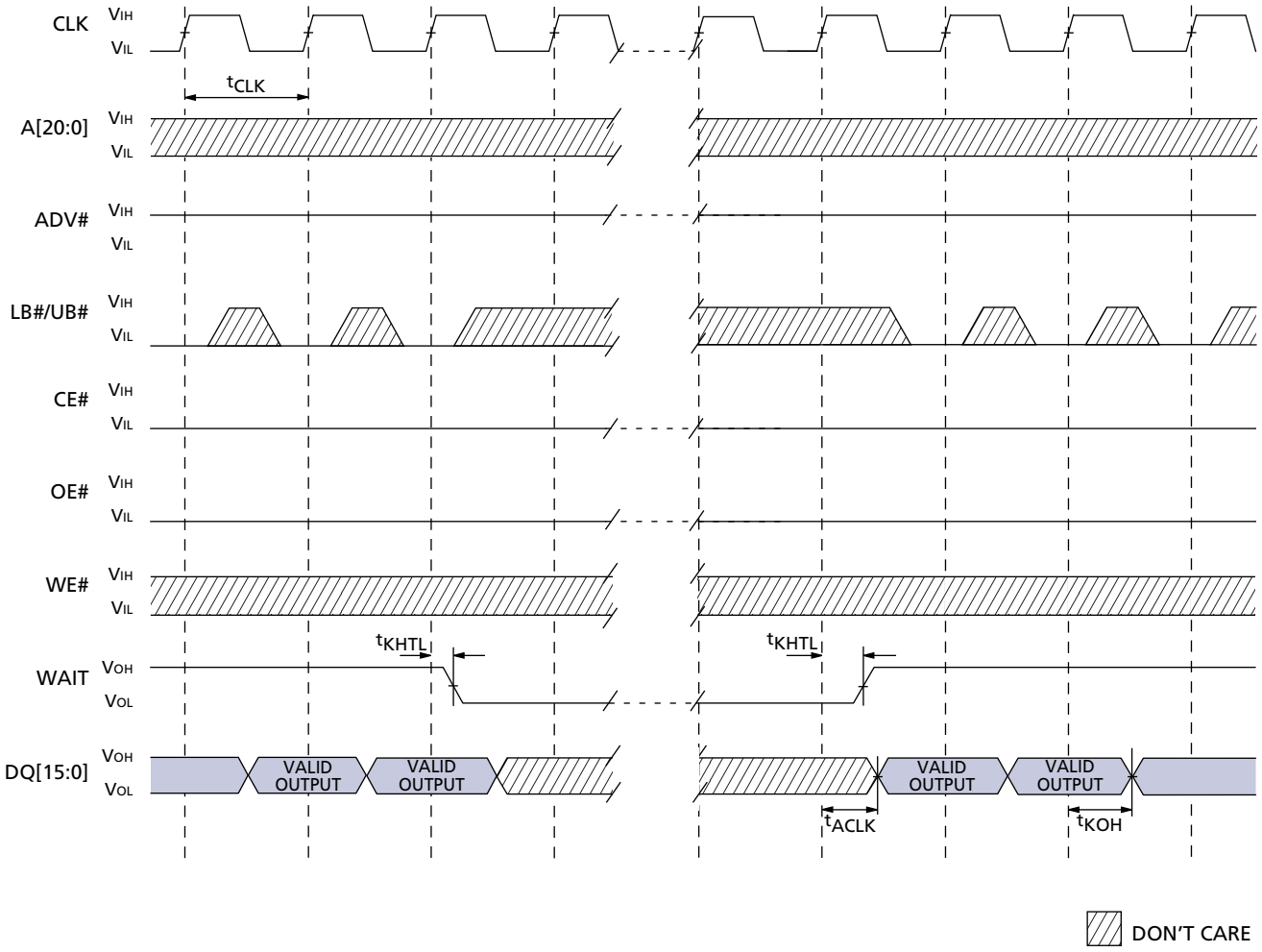
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 27: Burst READ Timing Parameters—Burst Suspend

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}ACLK		6.5		10	ns
^{t}BOE		20		20	ns
^{t}CBPH	5		5		ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	5	20	ns
^{t}HD	2		2		ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}HZ		8		8	ns
^{t}KOH	2		2		ns
^{t}OHZ		8		8	ns
^{t}OLZ	5		5		ns
^{t}SP	3		3		ns

Figure 30: Continuous Burst READ Showing an Output Delay with BCR[8] = 0 for End-of-Row Condition[1]



NOTE:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 28: Burst READ Timing Parameters—BCR[8] = 0

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}ACLK		6.5		10	ns
^{t}CLK	9.62	20	15	20	ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}KHTL		6.5		10	ns
^{t}KOH	2		2		ns

Figure 31: CE#-Controlled Asynchronous WRITE

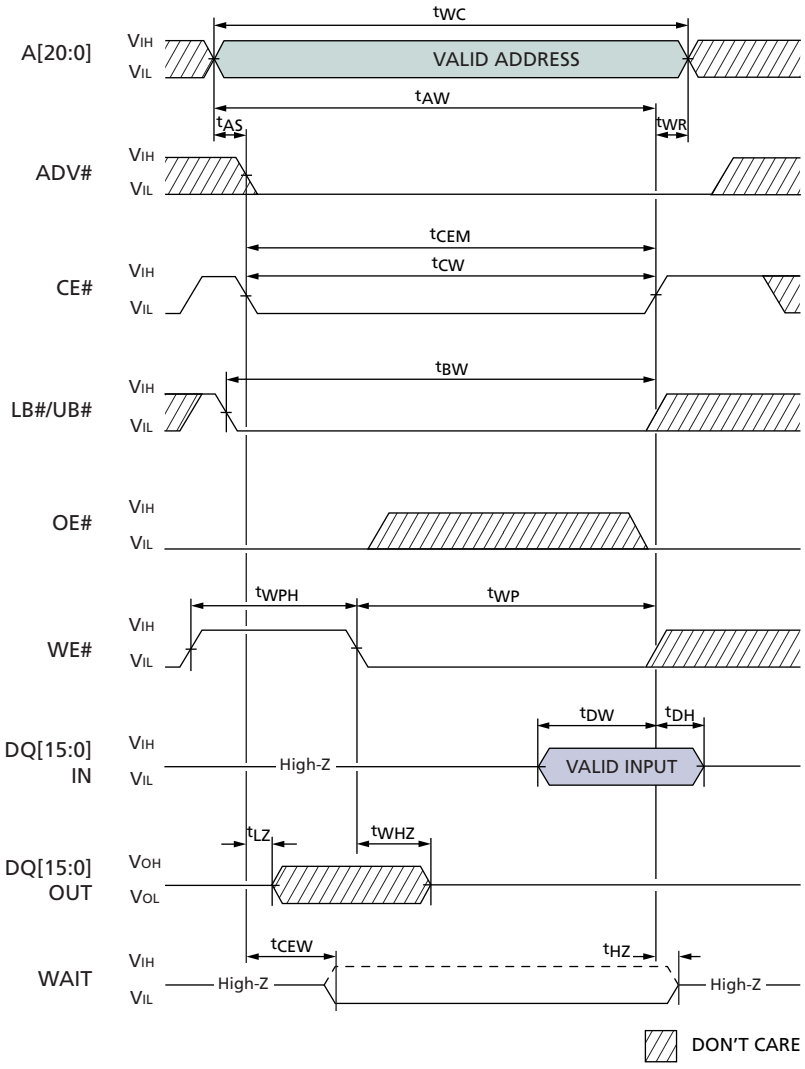


Table 29: Asynchronous WRITE Timing Parameters—CE#-Controlled

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		10		10	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Figure 32: LB#/UB#-Controlled Asynchronous WRITE

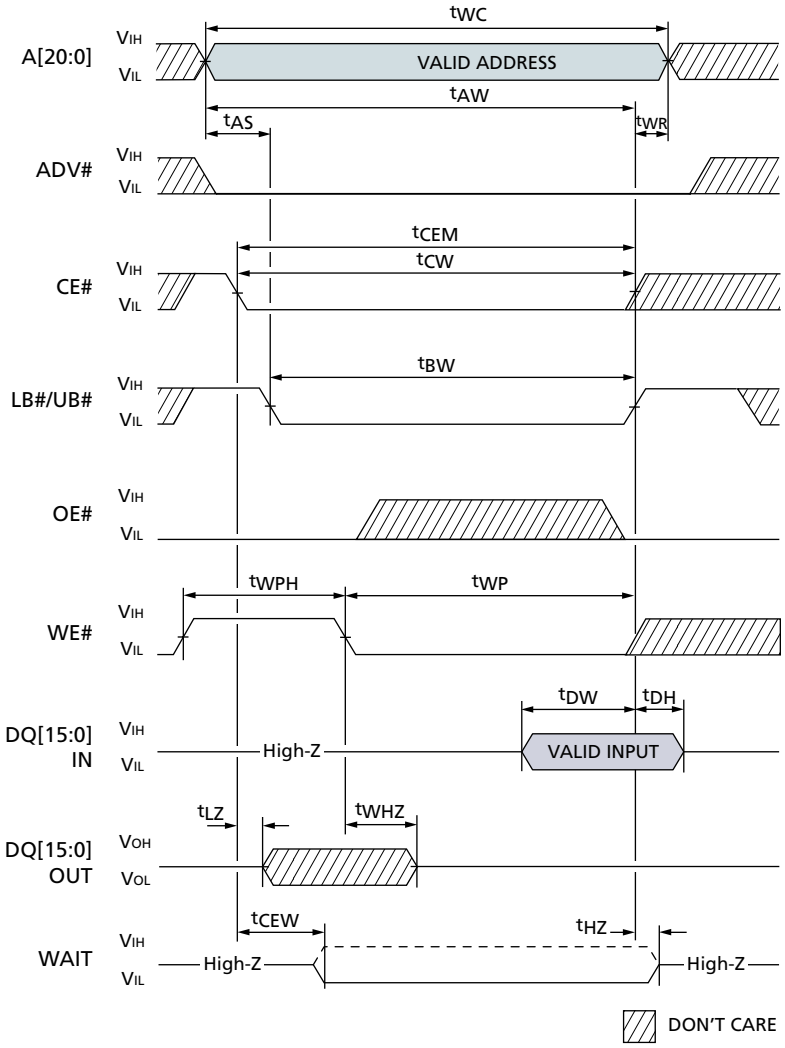


Table 30: Asynchronous WRITE Timing Parameters—LB#/UB#-Controlled

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}AS	0		0		ns
^{t}AW	70		85		ns
^{t}BW	70		85		ns
^{t}CEM		10		10	µs
^{t}CEW	1	7.5	1	7.5	ns
^{t}CW	70		85		ns
^{t}DH	0		0		ns
^{t}DW	23		23		ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}HZ		8		8	ns
^{t}LZ	10		10		ns
^{t}WC	70		85		ns
^{t}WHZ		8		8	ns
^{t}WP	46		55		ns
^{t}WPH	10		10		ns
^{t}WR	0		0		ns

Figure 33: WE#-Controlled Asynchronous WRITE

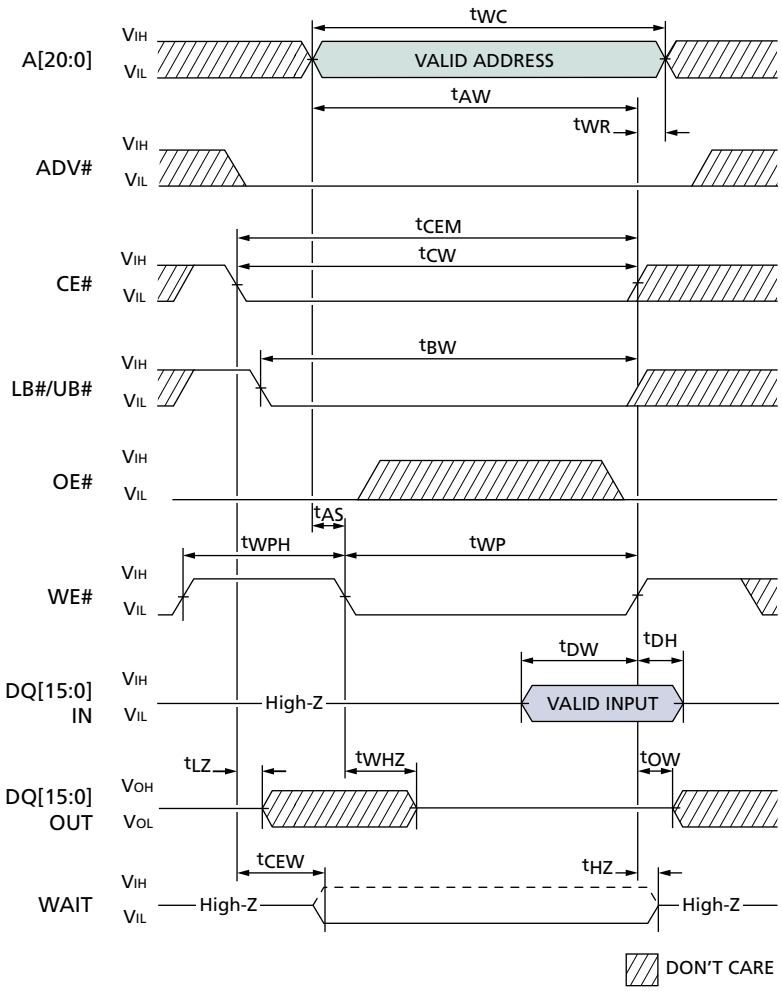


Table 31: Asynchronous WRITE Timing Parameters—WE#-Controlled

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}AS	0		0		ns
^{t}AW	70		85		ns
^{t}BW	70		85		ns
^{t}CEM		10		10	µs
^{t}CEW	1	7.5	1	7.5	ns
^{t}CW	70		85		ns
^{t}DH	0		0		ns
^{t}DW	23		23		ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}HZ		8		8	ns
^{t}LZ	10		10		ns
^{t}OW	5		5		ns
^{t}WC	70		85		ns
^{t}WHZ		8		8	ns
^{t}WP	46		55		ns
^{t}WPH	10		10		ns
^{t}WR	0		0		ns

Figure 34: Asynchronous WRITE Using ADV#

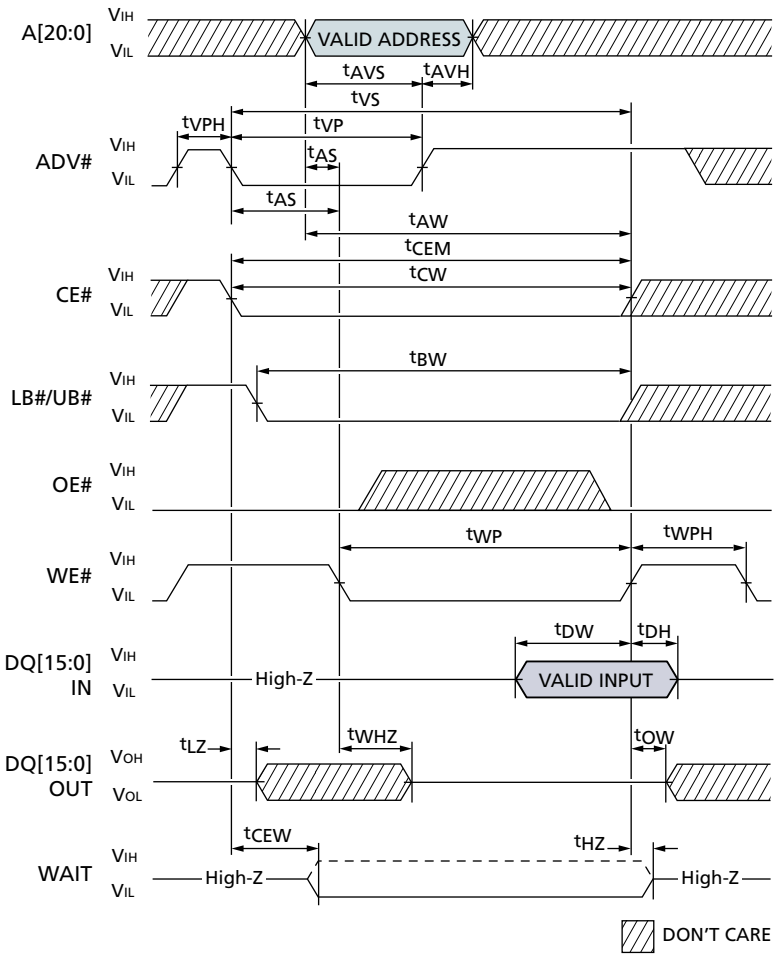
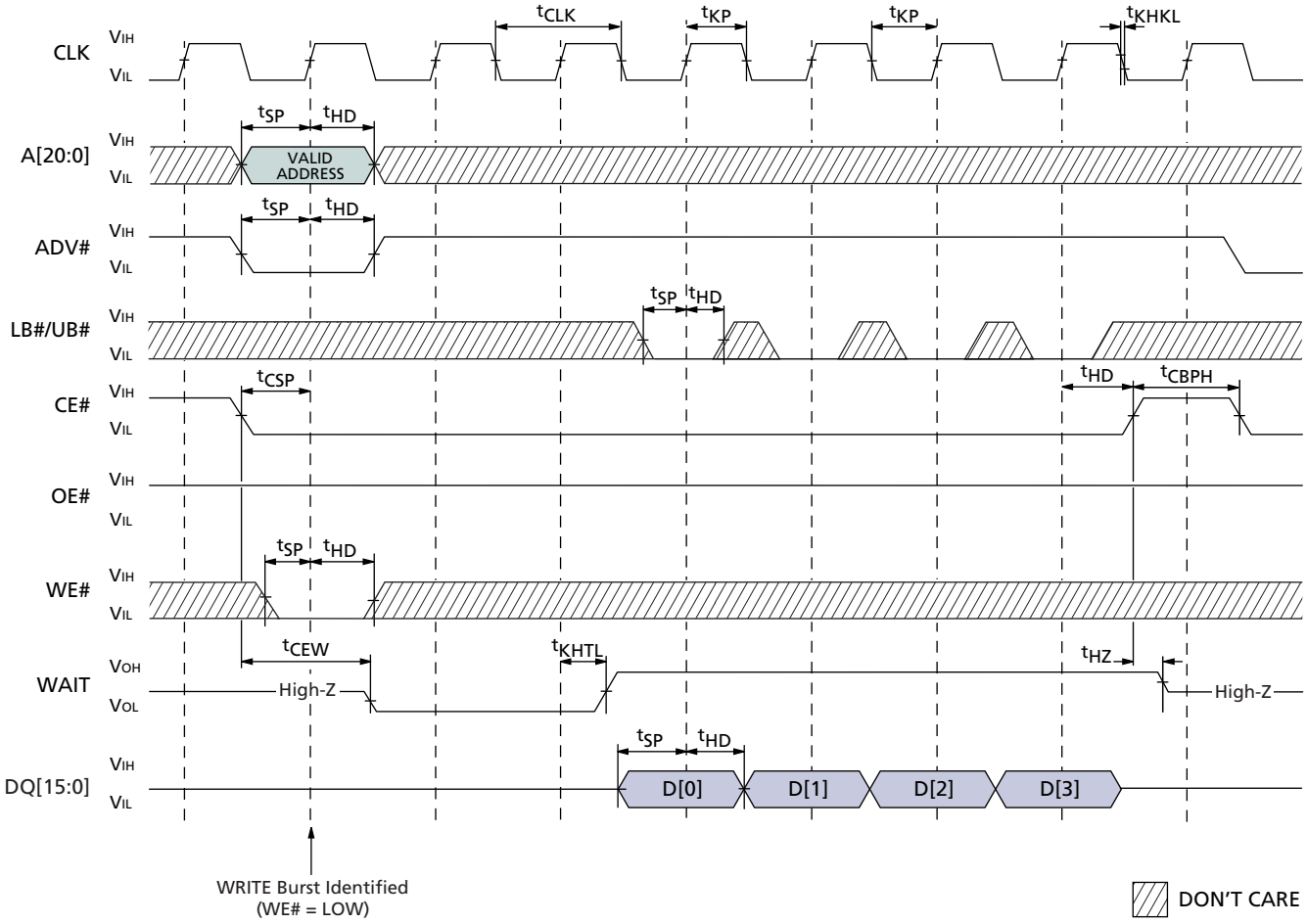


Table 32: Asynchronous WRITE Timing Parameters Using ADV#

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AS}	0		0		ns
t_{AVH}	5		5		ns
t_{AVS}	10		10		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		10		10	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OW}	5		5		ns
t_{VP}	10		10		ns
t_{VPH}	10		10		ns
t_{VS}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns

Figure 35: Burst WRITE Operation[1]



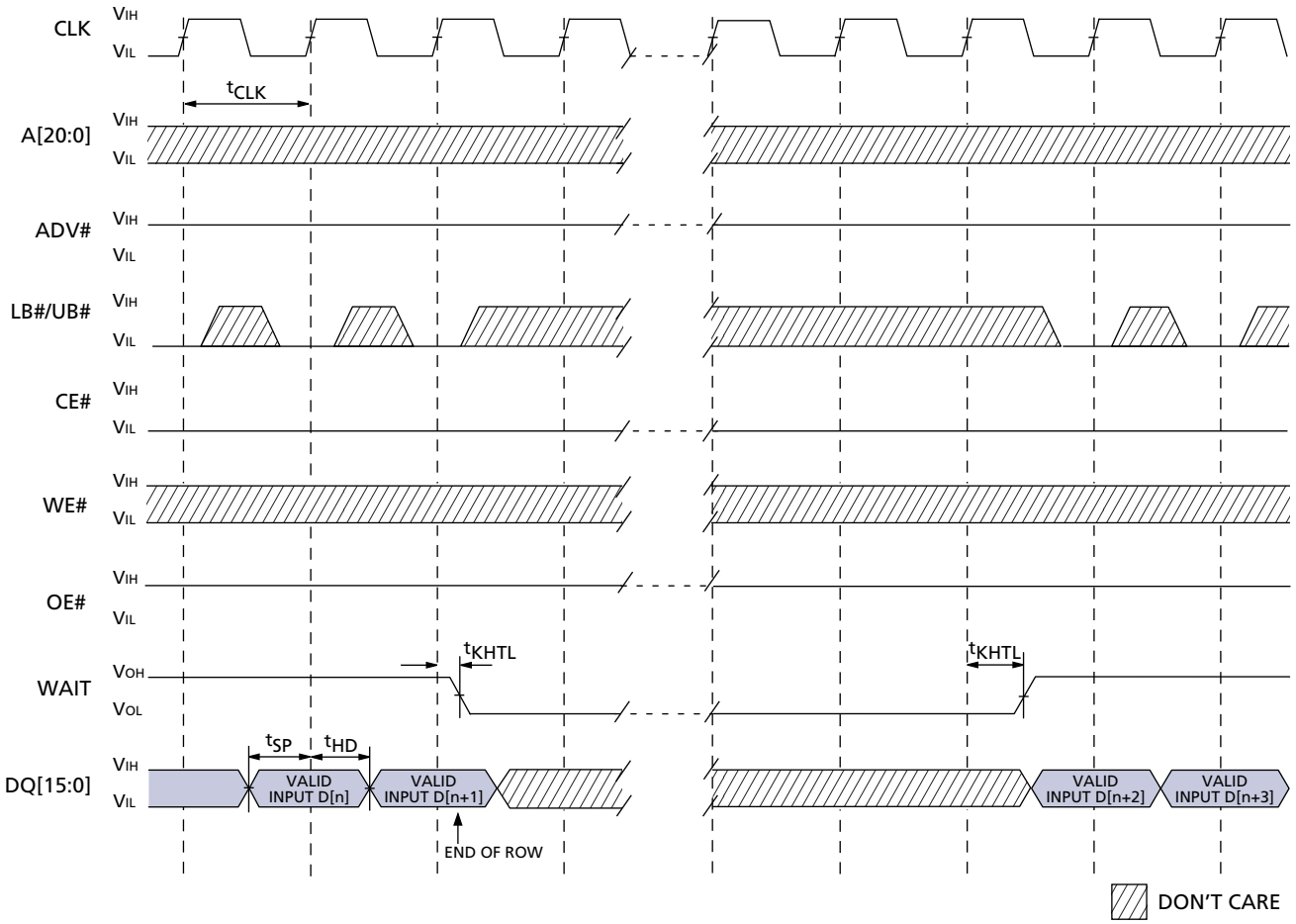
NOTE:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 33: Burst WRITE Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}CBPH	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	5	20	ns
^{t}HD	2		2		ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}HZ		8		8	ns
^{t}KHKL		1.6		1.6	ns
^{t}KHTL		6.5		10	ns
^{t}KP	3		3		ns
^{t}SP	3		3		ns

Figure 36: Continuous Burst WRITE Showing an Output Delay with BCR[8] = 0 for End-of-Row Condition[1]



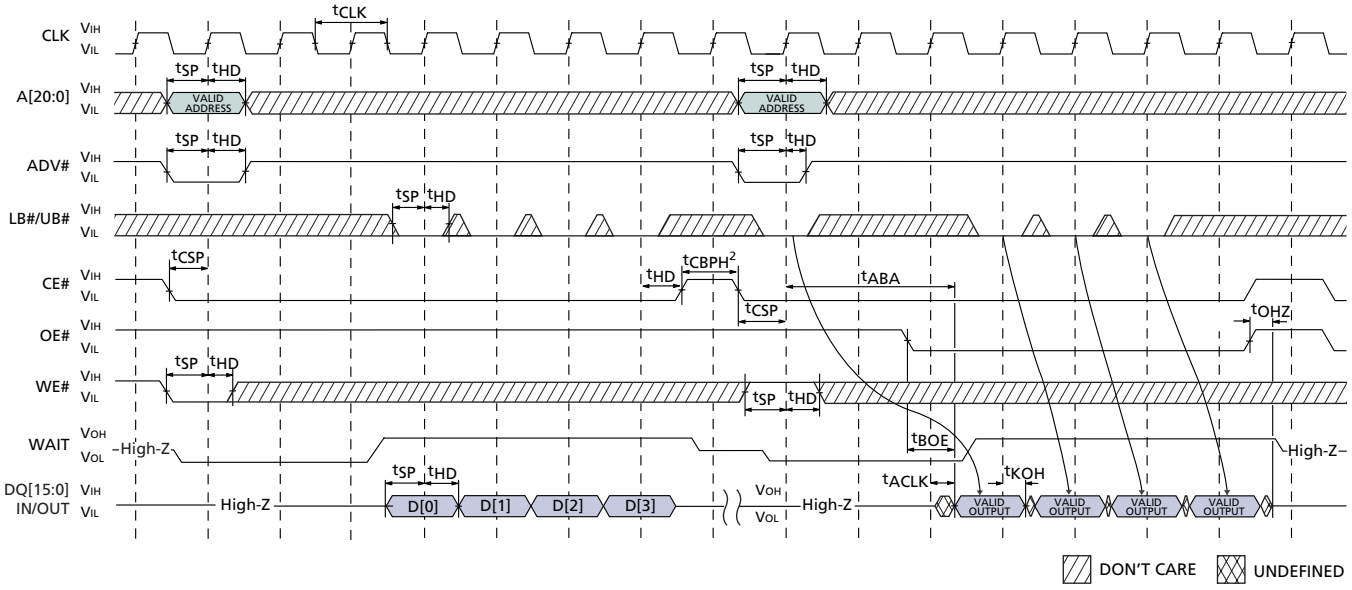
NOTE:
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 34: Burst WRITE Timing Parameters—BCR[8] = 0

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}CLK	9.62	20	15	20	ns
^{t}HD	2		2		ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}KHTL		6.5		10	ns
^{t}SP	3		3		ns

Figure 37: Burst WRITE Followed by Burst READ[1]



NOTE:

1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. To allow self-refresh operations to occur between transactions, CE# must remain HIGH for at least 5ns (^{t}CBPH) to schedule the appropriate internal refresh operation.
3. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 35: WRITE Timing Parameters—Burst WRITE Followed by Burst READ

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}CBPH	5		5		ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	5	20	ns

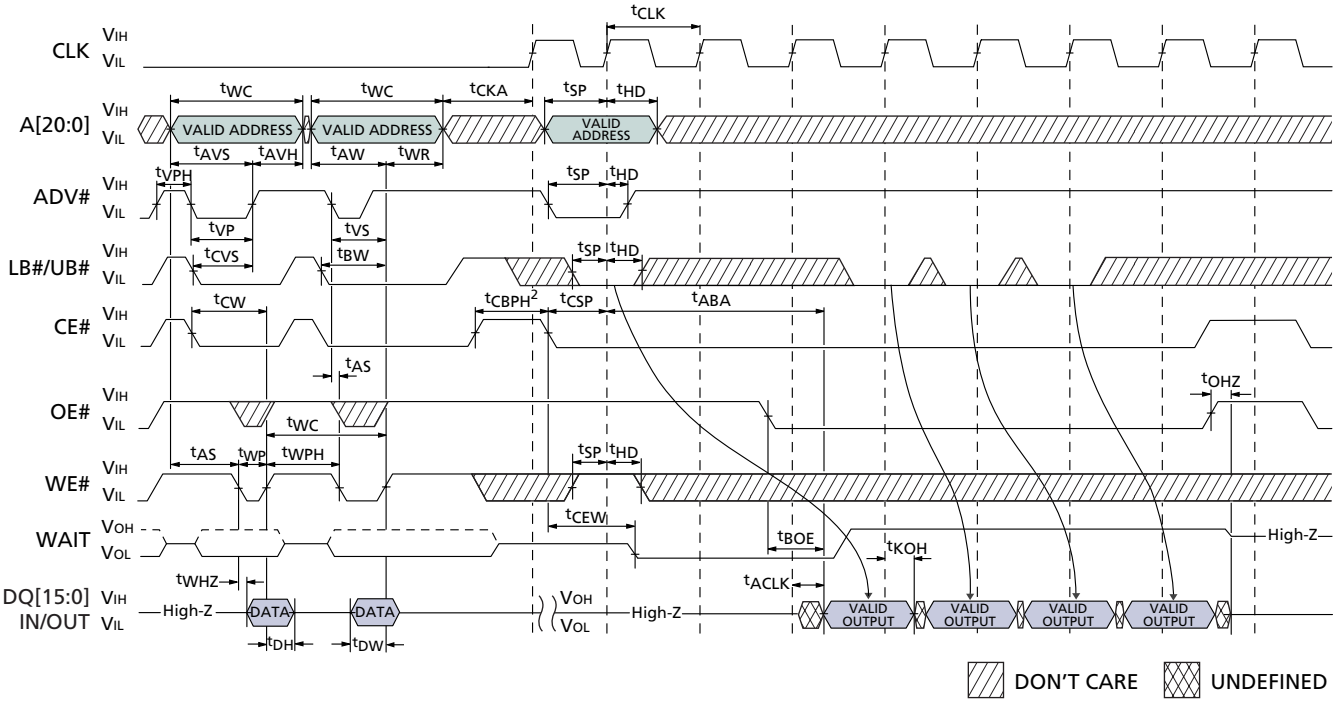
SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}HD	2		2		ns
^{t}SP	3		3		ns

Table 36: READ Timing Parameters—Burst WRITE Followed by Burst READ

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}ABA		35		55	ns
^{t}ACLK		6.5		10	ns
^{t}BOE		20		20	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	5	20	ns

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}HD	2		2		ns
^{t}KOH	2		2		ns
^{t}OHZ		8		8	ns
^{t}SP	3		3		ns

Figure 38: Asynchronous WRITE Followed by Burst READ[1]



NOTE:

1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and burst operations, CE# must go HIGH. CE# must remain HIGH for at least 5ns (^{t}CBPH) to schedule the appropriate internal refresh operation.
3. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 37: WRITE Timing Parameters—Async WRITE Followed by Burst READ

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}AS	0		0		ns
^{t}AVH	5		5		ns
^{t}AVS	10		10		ns
^{t}AW	70		85		ns
^{t}BW	70		85		ns
^{t}CKA	70		85		ns
^{t}CVS	10		10		ns
^{t}CW	70		85		ns
^{t}DH	0		0		ns

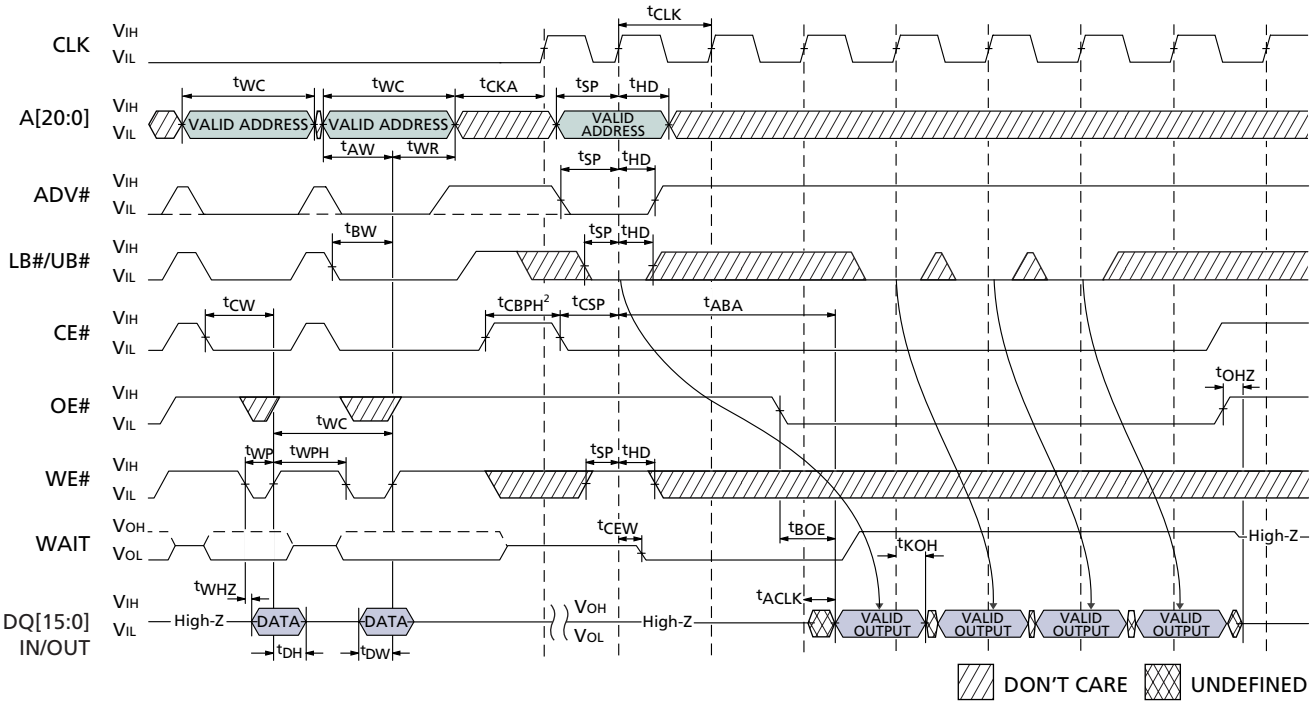
SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}DW	20		23		ns
^{t}VP	10		10		ns
^{t}VPH	10		10		ns
^{t}VS	70		85		ns
^{t}WC	70		85		ns
^{t}WHZ		8		8	ns
^{t}WP	46		55		ns
^{t}WPH	10		10		ns
^{t}WR	0		0		ns

Table 38: READ Timing Parameters—Async WRITE Followed by Burst READ

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}ABA		35		55	ns
^{t}ACLK		6.5		10	ns
^{t}BOE		20		20	ns
^{t}CBPH	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}CSP	4	20	5	20	ns
^{t}HD	2		2		ns
^{t}KOH	2		2		ns
^{t}OHZ		8		8	ns
^{t}SP	3		3		ns

Figure 39: Asynchronous WRITE Followed By Burst READ—ADV# LOW[1]



NOTE:

1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and burst operations, CE# must go HIGH. CE# must remain HIGH for at least 5ns (^{t}CBPH) to schedule the appropriate internal refresh operation.
3. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 39: Asynchronous WRITE Timing Parameters—ADV# LOW

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}AW	70		85		ns
^{t}BW	70		85		ns
^{t}CKA	70		85		ns
^{t}CW	70		85		ns
^{t}DH	0		0		ns
^{t}DW	23		23		ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}WC	70		85		ns
^{t}WHZ		8		8	ns
^{t}WP	46		55		ns
^{t}WPH	10		10		ns
^{t}WR	0		0		ns

Table 40: Burst READ Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}ABA		35		55	ns
^{t}ACLK		6.5		10	ns
^{t}BOE		20		20	ns
^{t}CBPH	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}CSP	4	20	5	20	ns
^{t}HD	2		2		ns
^{t}KOH	2		2		ns
^{t}OHZ		8		8	ns
^{t}SP	3		3		ns

Figure 40: Burst READ Followed by Asynchronous WRITE (WE#-Controlled)

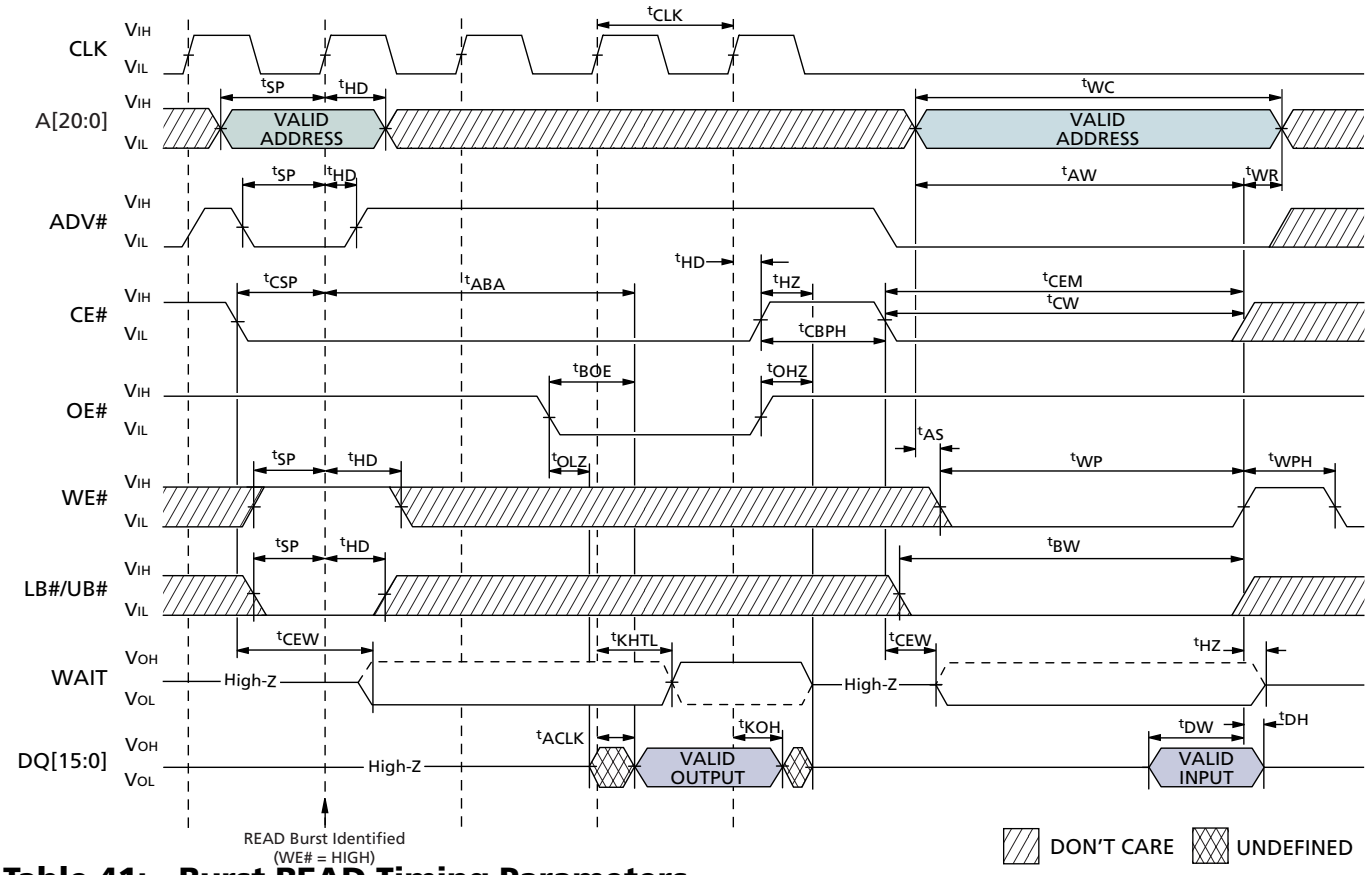


Table 41: Burst READ Timing Parameters

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
t_{ABA}		35		55	ns
t_{ACLK}		6.5		10	ns
t_{BOE}		20		20	ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	9.62	20	15	20	ns
t_{CSP}	4	20	5	20	ns

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
t_{HD}	2		2		ns
t_{HZ}		8		8	ns
t_{KHTL}		6.5		10	ns
t_{KOH}	2		2		ns
t_{OHZ}		8		8	ns
t_{SP}	3		3		ns

Table 42: Asynchronous WRITE Timing Parameters—WE# Controlled

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AS}	0			0	ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		10		10	µs
t_{CW}	70		85		ns
t_{DH}	0		0		ns

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{DW}	23		23		ns
t_{HZ}		8		8	ns
t_{WC}	70		85		ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Figure 41: Burst READ Followed by Asynchronous WRITE Using ADV#

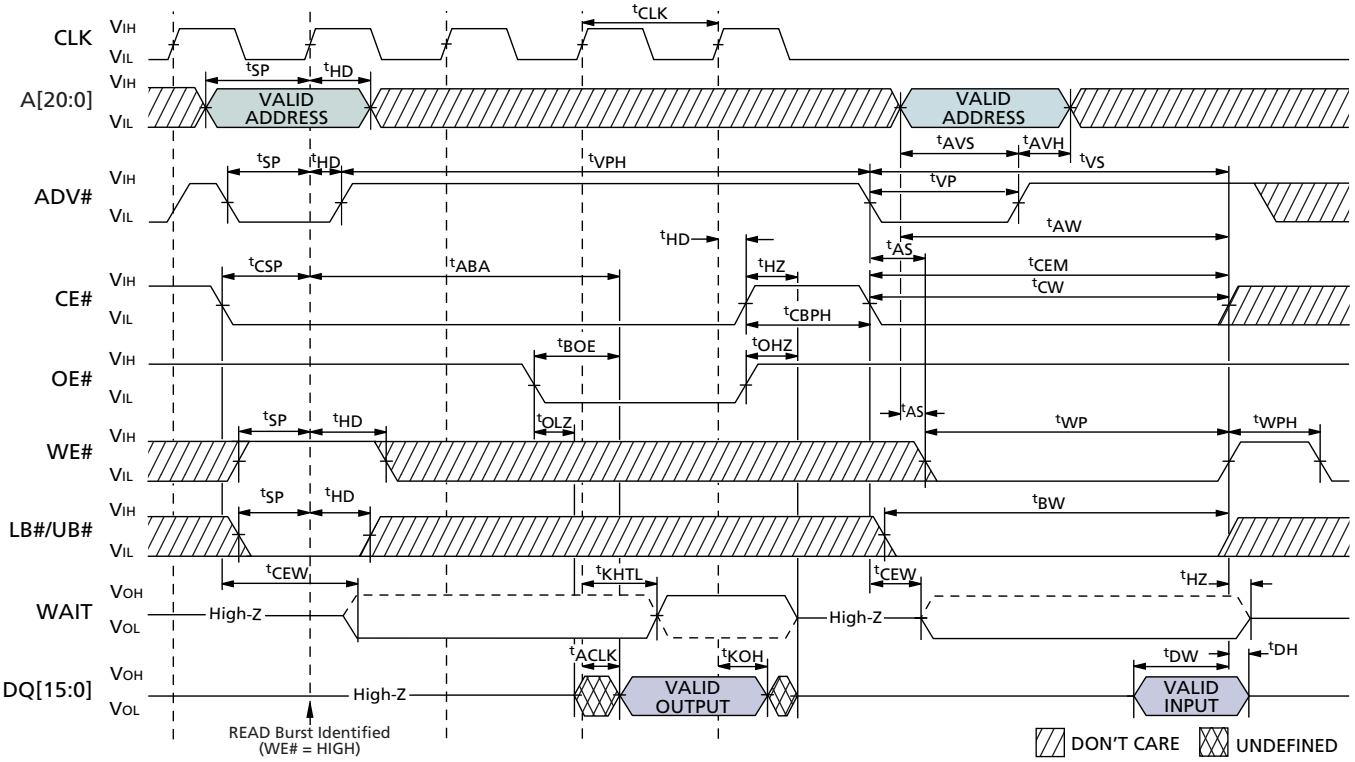


Table 43: Burst READ Timing Parameters

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
t_{ABA}		35		55	ns
t_{ACLK}		6.5		10	ns
t_{BOE}		20		20	ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	9.62	20	15	20	ns
t_{CSP}	4	20	5	20	ns

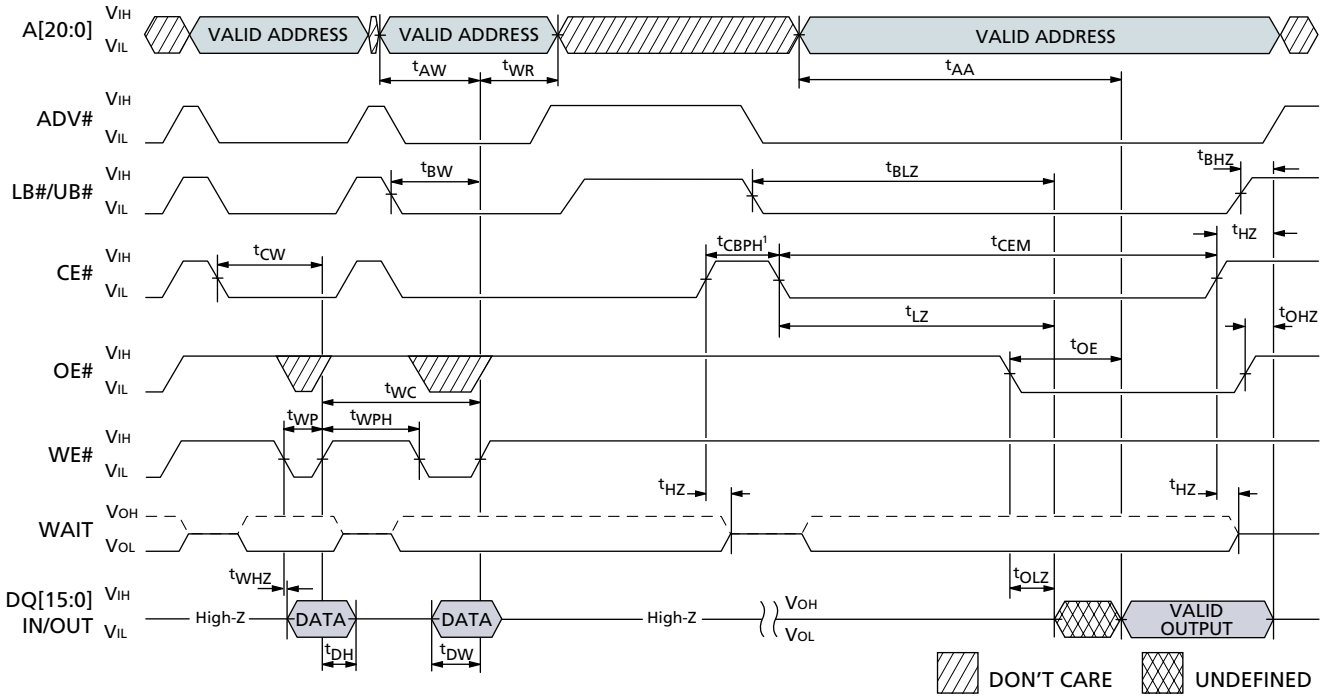
SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
t_{HD}	2		2		ns
t_{HZ}		8		8	ns
t_{KHTL}		6.5		10	ns
t_{KOH}	2		2		ns
t_{OHZ}		8		8	ns
t_{SP}	3		3		ns

Table 44: Asynchronous WRITE Timing Parameters Using ADV#

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AS}	0		0		ns
t_{AVH}	5		5		ns
t_{AVS}	10		10		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		10		10	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{HZ}		8		8	ns
t_{VP}	10		10		ns
t_{VPH}	10		10		ns
t_{VS}	70		85		ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns

Figure 42: Asynchronous WRITE Followed by Asynchronous READ—ADV# LOW



NOTE:

1. CE# must remain HIGH for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.

Table 45: WRITE Timing Parameters—ADV# LOW

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{HZ}		8		8	ns

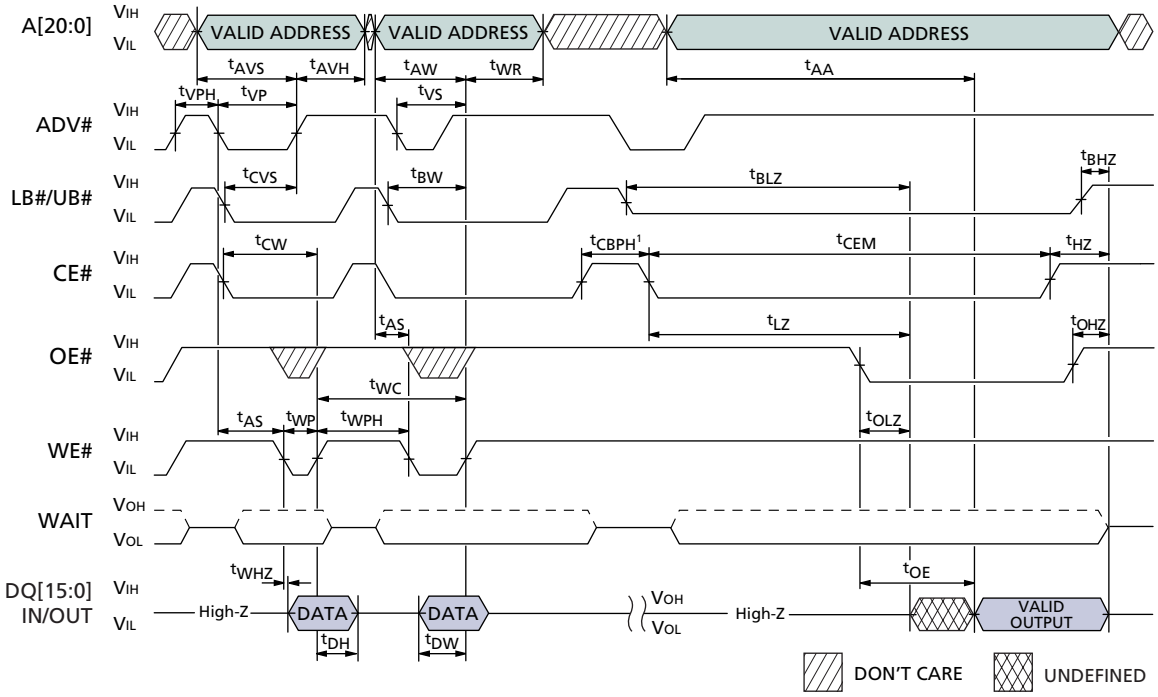
SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Table 46: READ Timing Parameters—ADV# LOW

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AA}		70		85	ns
t_{BHZ}		8		8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEM}		10		10	µs

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns

Figure 43: Asynchronous WRITE Followed by Asynchronous READ



NOTE:

1. CE# must remain HIGH for at least 5ns (^{t}CBPH) to schedule the appropriate internal refresh operation.

Table 47: WRITE Timing Parameters—Async WRITE Followed by Async READ

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}AS	0		0		ns
^{t}AVH	5		5		ns
^{t}AVS	10		10		ns
^{t}AW	70		85		ns
^{t}BW	70		85		ns
^{t}CVS	10		10		ns
^{t}CW	70		85		ns
^{t}DH	0		0		ns
^{t}DW	23		23		ns

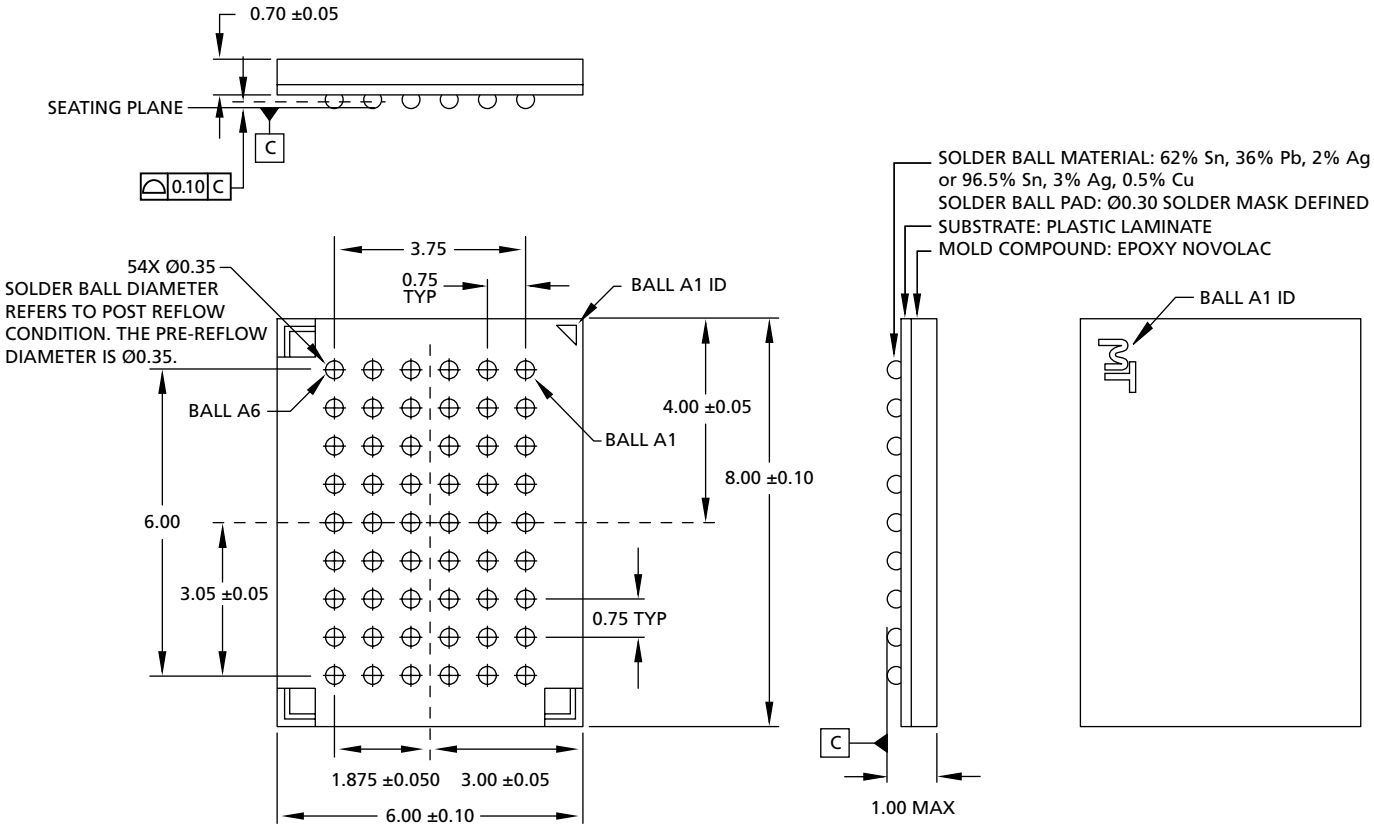
SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}VP	10		10		ns
^{t}VPH	10		10		ns
^{t}VS	70		85		ns
^{t}WC	70		85		ns
^{t}WHZ		8		8	ns
^{t}WP	46		55		ns
^{t}WPH	10		10		ns
^{t}WR	0		0		ns

Table 48: READ Timing Parameters—Async WRITE Followed by Async READ

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}AA		70		85	ns
^{t}BHZ		8		8	ns
^{t}BLZ	10		10		ns
^{t}CBPH	5		5		ns
^{t}CEM		10		10	µs

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}HZ		8		8	ns
^{t}LZ	10		10		ns
^{t}OE		20		20	ns
^{t}OHZ		8		8	ns
^{t}OLZ	5		5		ns

Figure 44: 54-Ball FBGA



NOTE:
1. All dimensions in millimeters; MAX/MIN, or typical, as noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Data Sheet Designation: ADVANCE

This data sheet contains initial descriptions of products still in development.

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APPENDIX A

How Extended Timings Impact CellularRAM™ Operation

Introduction

This note describes CellularRAM™ timing requirements in systems that perform extended operations.

CellularRAM products use a DRAM technology that periodically requires refresh to ensure against data corruption. CellularRAM devices include on-chip circuitry that performs the required refresh in a manner that is completely transparent in systems with normal bus timings. The refresh circuitry imposes constraints on timings in systems that take longer than 10µs to complete an operation. WRITE operations are affected if the device is configured for asynchronous operation. Both READ and WRITE operations are affected if the device is configured for page or burst-mode operation.

Asynchronous WRITE Operation

The timing parameters provided in Table 18 on page 28 require that all WRITE operations must be completed within 10µs. After completing a WRITE operation, the device must either enter standby (by transitioning CE# HIGH), or else perform a second operation (READ or WRITE) using a new address. Figures 45 and 46 demonstrate these constraints as they apply during an asynchronous (page-mode-disabled) operation. Either the CE# active period (^{t}CEM in Figure 45) or the address valid period (^{t}TM in Figure 46) must be less than 10µs during any WRITE operation, otherwise, the extended WRITE timings must be used.

Figure 45: Extended Timing for ^{t}CEM

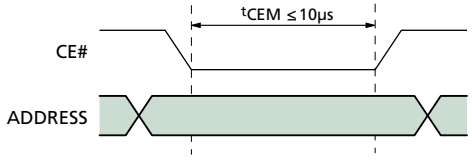


Figure 46: Extended Timing for ^{t}TM

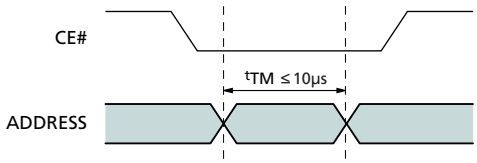


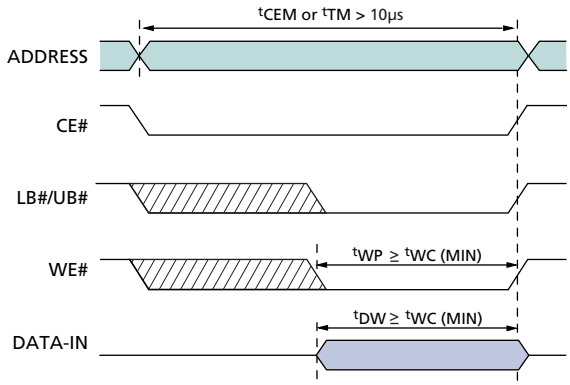
Table 49: Extended Cycle Impact on READ and WRITE Cycles

PAGE MODE	TIMING CONSTRAINT	READ CYCLE	WRITE CYCLE
Asynchronous Page Mode Disabled	^{t}CEM and ^{t}TM > 10µs (See Figures 45 and 46 above.)	No impact.	Must use extended WRITE timing. (See Figure 47 on page 54.)
Asynchronous Page Mode Enabled	^{t}CEM > 10µs (See Figure 45 above.)	Not allowed.	
Burst	^{t}CEM > 10µs (See Figure 45 above.)	Burst must cross a row boundary within 10µs.	

Extended WRITE Timing—Asynchronous WRITE Operation

Modified timings are required during extended WRITE operations (see Figure 47 below). An extended WRITE operation requires that both the write pulse width (^{t}WP) and the data valid period (^{t}DW) be lengthened to at least the minimum WRITE cycle time (^{t}WC [MIN]). These increased timings ensure that time is available for both a refresh operation and a successful completion of the WRITE operation.

Figure 47: Extended WRITE Operation



Page Mode READ Operation

When a CellularRAM device is configured for page mode operation, the address inputs are used to accelerate read accesses and cannot be used by the on-chip circuitry to schedule refresh. If CE# is LOW longer than the ^{t}CEM maximum time of 10µs, no refresh will occur and data may be lost. Page mode should only be used in systems that can limit CE#-LOW times to less than 10µs.

Burst-Mode Operation

When configured for burst-mode operation, it is necessary to allow the device to perform a refresh within any 10µs window. One of two conditions will enable the device to schedule a refresh within 10µs. The first condition is when all burst operations complete within 10µs. A burst completes when the CE# signal is registered HIGH on a rising clock edge. The second condition that allows a refresh is when a burst access crosses a row boundary. The row-boundary crossing causes WAIT to be asserted while the next row is accessed and enables the scheduling of refresh.

Summary

CellularRAM products are designed to ensure that any possible asynchronous timings do not cause data corruption due to lack of refresh. Slow bus timings on asynchronous WRITE operations require that ^{t}WP and ^{t}DW be lengthened. Asynchronous page bus timings must limit CE# LOW to less than 10µs.

Burst mode timings must allow the device to perform a refresh within any 10µs period. A burst operation must either complete (CE# registered HIGH) or cross a row boundary within 10µs to ensure successful refresh scheduling. These timing requirements are likely to have little or no impact when interfacing a CellularRAM device with a low-speed memory bus.

Revision History

Rev. A, Advance 2/04

- CR WRITE diagram titles updated to reflect WRITEs followed by READ ARRAY operation.

Rev. A, Advance 1/04

- Last address not changed by software access sequence.
- Added on-chip sensor to TCR.

Rev. A, Advance 1/04

- Clarified software access.

Rev. A, Advance 12/03

- Initial Release