

## IDM29811 Next-Address Controller

### General Description

The IDM29811 next-address control unit is specifically designed for next address control of the IDM2911A sequencer. The device can be used in high-performance computer control systems, structured state machine designs, or in other applications that utilize microprogramming techniques.

A 4-bit instruction field ( $I_3-I_0$ ) provides sixteen instructions; also, a test input is available for conditional instructions. Among the conditional instructions that can be executed are: conditional jumps, conditional jump to subroutine, conditional return from subroutine, conditional repeat loops, conditional branch to starting address, and so on.

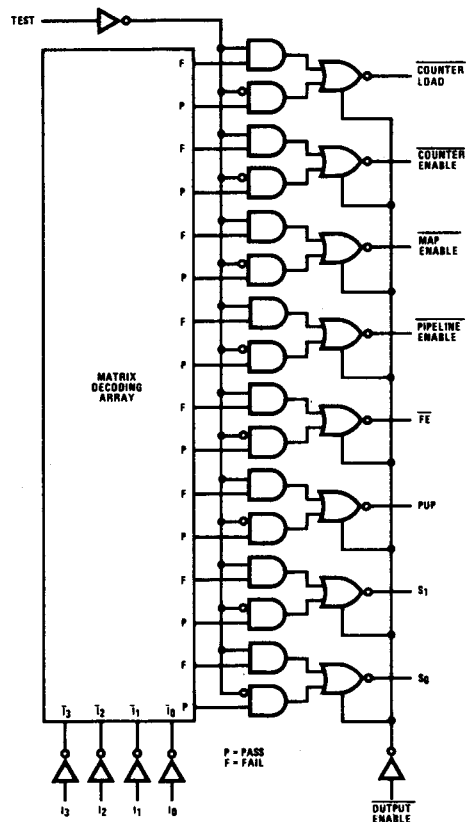
A single IDM29811 can be used to control any number of IDM2911A sequencers. Using one IDM29811 and

three IDM2911As, a sequencer capable of controlling 4k of microprogram memory can be easily implemented.

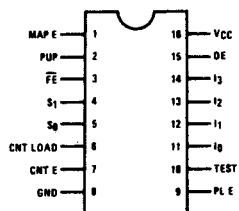
### Features and Benefits

- 16 next-address instructions
- Test input for conditional instructions
- Separate outputs to control the IDM2911A, an independent event counter, and a mapping PROM/branch address interface
- Uses low-power Schottky technology
- Meets all requirements of MIL-STD-883

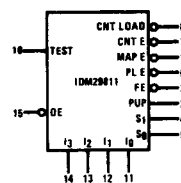
### Logic Diagram



### Connection Diagram



### Logic Symbol



**Absolute Maximum Ratings** (Note 1)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	-0.5V to +V <sub>CC</sub> max
DC Input Voltage	-0.5V to +5.5V
DC Output Current, into Outputs	30 mA
DC Input Current	-30 mA to +5.0 mA

**Operating Range**

P/N	Ambient Temperature	V <sub>CC</sub>
Com'l		
IDM29811JC,NC	0°C to +70°C	4.75V to 5.25V
Mil		
IDM29811JM,JM/883	-55°C to +125°C	4.50V to 5.50V

**DC Electrical Characteristics** (Note 2)

PARAMETER		CONDITIONS	Com'l			Mil			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I <sub>IL</sub>	Input Load Current, All Inputs	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0.45V		-80	-250		-80	-250	μA
I <sub>IH</sub>	Input Leakage Current, All Inputs	V <sub>CC</sub> = Max, V <sub>IN</sub> = 2.7V			25			25	μA
I <sub>I</sub>	Input Leakage Current, All Inputs	V <sub>CC</sub> = Max, V <sub>IN</sub> = 5.5V			1.0			1.0	mA
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 16 mA		0.35	0.5		0.35	0.5	V
V <sub>IL</sub>	Low Level Input Voltage				0.80			0.80	V
V <sub>IH</sub>	High Level Input Voltage		2.0			2.0			V
V <sub>C</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>IN</sub> = -18 mA		-0.8	-1.2		-0.8	-1.2	V
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5V, V <sub>IN</sub> = 2V, T <sub>A</sub> = 25°C, 1 MHz		4.0			4.0		pF
C <sub>O</sub>	Output Capacitance	V <sub>CC</sub> = 5V, V <sub>O</sub> = 2V, T <sub>A</sub> = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = Max, All Inputs Grounded, All Outputs Open		70	110		70	110	mA

**TRI-STATE PARAMETERS**

I <sub>SC</sub>	Output Short Circuit Current	V <sub>O</sub> = 0V, V <sub>CC</sub> = Max, (Note 3)	-20	-45	-70	-20	-45	-70	mA
I <sub>HZ</sub>	Output Leakage (TRI-STATE)	V <sub>CC</sub> = Max, V <sub>O</sub> = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V <sub>OH</sub>	Output Voltage High,	I <sub>OH</sub> = -2 mA				2.4	3.2		V
		I <sub>OH</sub> = -6.5 mA	2.4	3.2					V

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

**Note 2:** These limits apply over the entire operating range unless stated otherwise. All typical values are for V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.

**Note 3:** During I<sub>SC</sub> measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

## Switching Characteristics Over Operating Temperature

Symbol	Description	Test Conditions	Com'l		Mil		Units
			Min.	Max.	Min.	Max.	
tPLH	I <sub>i</sub> to Any Output	C <sub>L</sub> = 15 pF R <sub>L</sub> = 2.0 kΩ		30		40	ns
tPHL							
tPLH	Test to Any Output			30		40	ns
tPHL							
tZH	OE to Any Output			20		30	ns
tZL							
tHZ	OE to Any Output			20		30	ns
tLZ							

## Pinout Descriptions

I <sub>3</sub> /I <sub>2</sub> /I <sub>1</sub> /I <sub>0</sub>	Four instruction inputs
Test	Condition-code input. When test input is low, the device assumes test has failed; when input is high, the test is assumed to have passed. In either case, a branch is made to one of the conditional-code instructions; refer to the tables which follow.
Counter Load	An output used to drive the parallel load input of an up/down counter.
Counter Enable	An output used to drive the enable input of an up/down counter.
Map Enable	An output that controls the three-state outputs of the mapping PROM or PLA used to provide the initial starting address for each machine instruction.
Pipeline Enable	An output used to control the three-state output of the pipeline register which contains the branch address of the computer control unit.
FE File Enable	An output used to drive the file enable input of the IDM2911A. When this output is low, a stack operation will take place.
PUP	An output used to drive the push/pop input of the IDM2911A address controller. When the PUP output is high, a push will take place if the file is enabled. When the PUP output is low, a pop will take place if the file is enabled.

S<sub>0</sub>/S<sub>1</sub>

These outputs are used to drive the S<sub>0</sub>/S<sub>1</sub> inputs of the IDM2911A address controller. These outputs control whether the direct input, the register, the microprogram counter, or the stack is selected as the source of the next address for the microprogram memory.

## Instruction Table

Mnemonic	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Instruction
JZ	L	L	L	L	Jump to Address Zero
CJS	L	L	L	H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register
JMAP	L	L	H	L	Jump to Address at Mapping PROM Output
CJP	L	L	H	H	Conditional Jump to Address in Pipeline Register
PUSH	L	H	L	L	Push Stack and Conditionally Load Counter
JSRP	L	H	L	H	Jump-to-Subroutine with Starting Address Conditionally Selected from IDM2911A Register or Pipeline Register
CJV	L	H	H	L	Conditional Jump to Vector Address
JRP	L	H	H	H	Jump to Address Conditionally Selected from IDM2911A R-Register or Pipeline Register
RFCT	H	L	L	L	Repeat Loop if Counter is Not Equal to Zero
RPCT	H	L	L	H	Repeat Pipeline Address if Counter is Not Equal to Zero
CRTN	H	L	H	L	Conditional Return-from-Subroutine
CJPP	H	L	H	H	Conditional Jump to Pipeline Address and Pop Stack
LDCT	H	H	L	L	Load Counter and Continue
LOOP	H	H	L	H	Test End of Loop
CONT	H	H	H	L	Continue to Next Address
JP	H	H	H	H	Jump to Pipeline Register Address

## Function Table

Mnemonic	Inputs				Test Input	Outputs					
	Instruction I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>		Function	Next ADDR Source	File	Counter	MAP E	PL E
JZ	L	L	L	L	JUMP ZERO	K	D	HOLD	LL*	H	L
CJS	L	L	L	H	COND JSB PL	L H	PC D	HOLD PUSH	HOLD HOLD	H H	L L
JMAP	L	L	H	L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L	L	H	H	COND JUMP PL	L H	PC D	HOLD HOLD	HOLD HOLD	H H	L L
PUSH	L	H	L	L	PUSH/COND LD CNTR	L H	PC PC	PUSH PUSH	HOLD LOAD	H H	L L
JSRP	L	H	L	H	COND JSB R/PL	L H	R D	PUSH PUSH	HOLD HOLD	H H	L L
CJV	L	H	H	L	COND JUMP VECTOR	L H	PC D	HOLD HOLD	HOLD HOLD	H H	H H
JRP	L	H	H	H	COND JUMP R/PL	L H	R D	HOLD HOLD	HOLD HOLD	H H	L L
RFCT	H	L	L	L	REPEAT LOOP, CNTR ≠ 0	L H	F PC	HOLD POP	DEC HOLD	H H	L L
RPCT	H	L	L	H	REPEAT PL, CNTR ≠ 0	L H	D PC	HOLD HOLD	DEC HOLD	H H	L L
CRTN	H	L	H	L	COND RTN	L H	PC F	HOLD POP	HOLD HOLD	H H	L L
CJPP	H	L	H	H	COND JUMP PL & POP	L H	PC D	HOLD POP	HOLD HOLD	H H	L L
LDCT	H	H	L	L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H	H	L	H	TEST END LOOP	L H	F PC	HOLD POP	HOLD HOLD	H H	L L
CONT	H	H	H	L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H	H	H	H	JUMP PL	X	D	HOLD	HOLD	H	L

L = Low      DEC = Decrement  
H = High      \*LL = Special Case  
X = Don't Care

## Truth Table

Mnemonic	Function	Pin No.					4 5		3 2		6 7		1	9
		Inputs					Outputs							
		$I_3$	$I_2$	$I_1$	$I_0$	TEST	Next ADDR Source $S_1$ $S_0$	File FE PUP	Counter LOAD EN	MAPE	PLE			
JZ	JUMP ZERO	L	L	L	L	L	H	H	H	H	L	L	H	L
CJS	COND JSB PL	L	L	L	H	L	L	L	H	H	H	H	H	L
JMAP	JUMP MAP	L	L	H	L	L	H	H	H	H	H	H	L	H
CJP	COND JUMP PL	L	L	H	H	L	L	L	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR	L	H	L	L	L	L	L	L	H	H	H	H	L
JSRP	COND JSB R/PL	L	H	L	H	L	L	H	L	H	H	H	H	L
CJV	COND JUMP VECTOR	L	H	H	L	L	L	L	H	H	H	H	H	H
JRP	COND JUMP R/PL	L	H	H	H	L	L	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR $\neq 0$	H	L	L	L	L	H	L	H	L	H	L	H	L
RPCT	REPEAT PL, CTR $\neq 0$	H	L	L	H	L	H	H	H	H	H	L	H	L
CRTN	COND RTN	H	L	H	L	L	L	L	H	L	H	H	H	L
CJPP	COND JUMP PL & POP	H	L	H	H	L	L	L	H	L	H	H	H	L
LDCT	LD CNTR & CONTINUE	H	H	L	L	L	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP	H	H	L	H	L	H	L	H	L	H	H	H	L
CONT	CONTINUE	H	H	H	L	L	L	L	H	H	H	H	H	L
JP	JUMP PL	H	H	H	H	L	H	H	H	H	H	H	H	L

L = Low, H = High

## Guaranteed Loading Characteristics Over Operating Range (in unit loads)

Pin Nos.	Input/Output	Input Load	Output High	Output Low
1	MAPE	—	100	44
2	PUP	—	100	44
3	FE	—	100	44
4	$S_1$	—	100	44
5	$S_0$	—	100	44
6	CNT LOAD	—	100	44
7	CNT E	—	100	44
8	GND	—	—	—
9	PLE	—	100	44
10	TEST	0.5	—	—
11	$I_0$	0.5	—	—
12	$I_1$	0.5	—	—
13	$I_2$	0.5	—	—
14	$I_3$	0.5	—	—
15	OE	—	100	44
16	VCC	—	—	—

A Low-Power Schottky TTL Unit Load is defined as 20  $\mu$ A measured at 2.7V High and -0.36mA measured at 0.4V Low.