

Description

NEC Electronics Inc. and Crosspoint Solutions, Inc. have joined forces to offer to system designers an expedient way to prototype in Field Programmable Gate Arrays (FPGAs) and easily migrate the design into NEC's family of CMOS Mask Programmable Gate Arrays (MPGAs).

The CP20K series of FPGAs are the first true products that are architecturally compatible with standard MPGAs. They use a macrocell library and a transistor-level interconnect programmability, the same as used with NEC's gate arrays. This compatibility allows improved performance, reduced gate counts, lower power consumption, and a conversion process that is very straightforward and predictable.

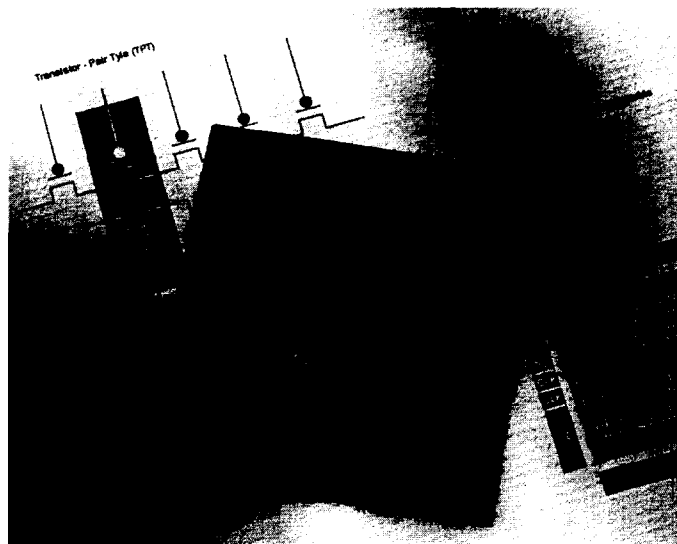
The CP20K series consists of six different master cells with densities that range from 2,200 to 20,000 gates. Gate utilization is 60% to 85% using the automatic placement and automatic routing capabilities of the Crosspoint Design System (CDS™). Interactive placement and routing is also provided which gives fine-tuning capabilities to critical speed paths and optimized gate use.

The CP20K series features the industry's most flexible I/Os. Each general purpose I/O pad can be configured as an input, output or bidirectional pad.

The CP20K series is manufactured in a 0.8μm CMOS process with two-layer metalization. Central to Crosspoint's process architecture is a proprietary antifuse. An antifuse is a programmable element that has a very high impedance initially, but exhibits a low resistance after programming. This translates directly to higher speed, since interconnect RC delays are reduced. The programming is one-time programmable (OTP).

Crosspoint's FPGA products are fully supported by NEC's advanced ASIC design technology. NEC's OpenCAD® integration system lets the CP20K designer choose the most powerful design tools and services available, for schematic entry, synthesis, simulation, timing and fault analysis, and test vector generation. Crosspoint Design System (CDS) is then used to place and route the design. A choice of automatic or interactive place and route features give the designer maximum control for fine tuning critical speed paths and optimizing gate use. When the design is complete, an antifuse map is generated and downloaded to the FPGA programmer, figure 1. It programs the FPGA and also performs functional testing, if desired. Various package options are supported via individual socket adapters.

Figure 1. CP20K FPGAs



CP20K Series of FPGAs

Device	Available Gates	Usable Gates	TPT Count	RLT Count	I/O Pads (Max.)
CP20220	2,246	1,300 – 1,900	1,896	474	91
CP20420	4,245	2,500 – 3,600	3,584	896	130
CP20840	8,425	5,100 – 7,100	6,740	1,685	180
CP21200	12,320	7,200 – 10,800	8,960	2,240	203
CP21600	16,170	9,600 – 13,700	11,760	2,940	250
CP22000	20,262	12,000 – 17,200	14,736	3,684	270

Features

- True gate array architecture
 - Transistor-level interconnect programmability
 - Gate array macro library and design methodology
- Performance comparable to NEC's CMOS gate arrays
- Uses low-impedance antifuse technology
- Four independent clock trees minimize clock skew
- Flexible I/O inputs: CMOS, TTL, Schmitt with or without pull-up resistor
- Flexible I/O outputs: 4, 8 or 12 mA drive; three-state; programmable slew rates; open-drain/source
- High I/O to gate ratio
- Flexible memory block implementation
- Built-in IEEE 1149.1 (JTAG) interface
- Industry-standard EDA tools for design entry, simulation, timing analysis, fault simulation, and test pattern generation
- Gate-level-granularity takes maximum advantage of HDL/Synthesis top-down design methodology
- Automatic or interactive place and route fine tunes performance and increases gate utilization

Circuit Architecture

The CP20K series architecture provides the same gate-level granularity as NEC's MPGAs. Individual transistors are selectively connected to each other or to the power and ground rails to make the specified macrocells. These cells are then connected to perform logic functions. In NEC MPGAs, these connections are made by depositing the desired metalization patterns during wafer fabrication. In Crosspoint FPGAs, antifuses are used to selectively connect metal segments.

The CP20K series is a channeled gate array architecture, figure 2, consisting of logic rows, where the active circuitry resides, and routing channels, where the majority of cell-to-cell interconnections are made. Additional resources in the perimeter surrounding the core array are used to implement input and output cells, the clock network, as well as resources for JTAG boundary scan testing.

Logic Rows

The logic row is made up of two types of building blocks; the Transistor-Pair Tile (TPT™) and the RAM-Logic Tile (RLT™). The TPT is the smallest building block of the array and is identical to that of NEC's MPGAs. It consists of a pair of p-channel and n-channel transistors (figure 3). Connected in the appropriate pattern, groups of TPTs can form combinatorial and sequential logic functions. To isolate adjacent macrocells, the gates of one or more p- and n-channel transistors are connected to V_{CC} or ground, respectively. This results in the highest possible packing density.

The RLT is a logic module that is particularly efficient in implementing memory structures and sequential logic elements (figure 4). Four of the eight RLT ports (RN, WN, CS, and RW) are hard-wired to a set of global lines for memory block implementations. The remaining four ports (FB, IN, CLK, and OUT) may be connected locally through antifuse programming to various other wires inside the adjacent logic rows and routing channels.

TPT and RLT are trademarks of Crosspoint Solutions, Inc.

Figure 2. CP20K Channeled Gate Array Architecture

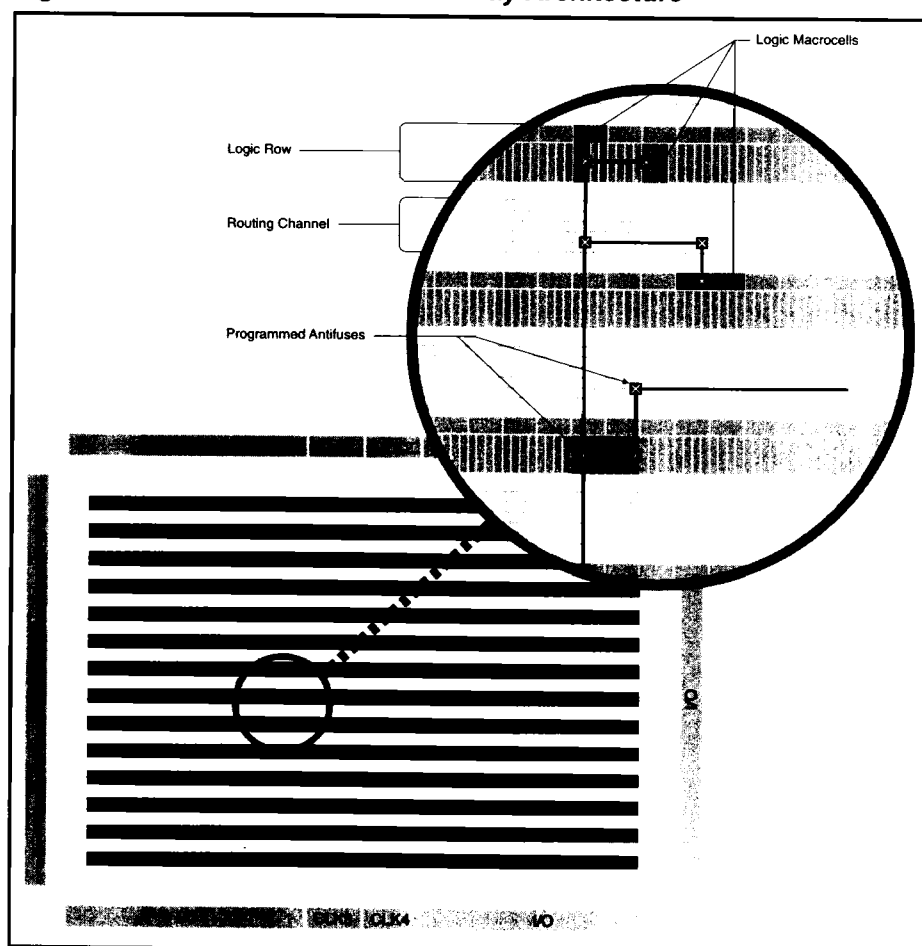


Figure 3. Groups of TPTs, the Smallest Building Block, Can Implement Various Logic Functions

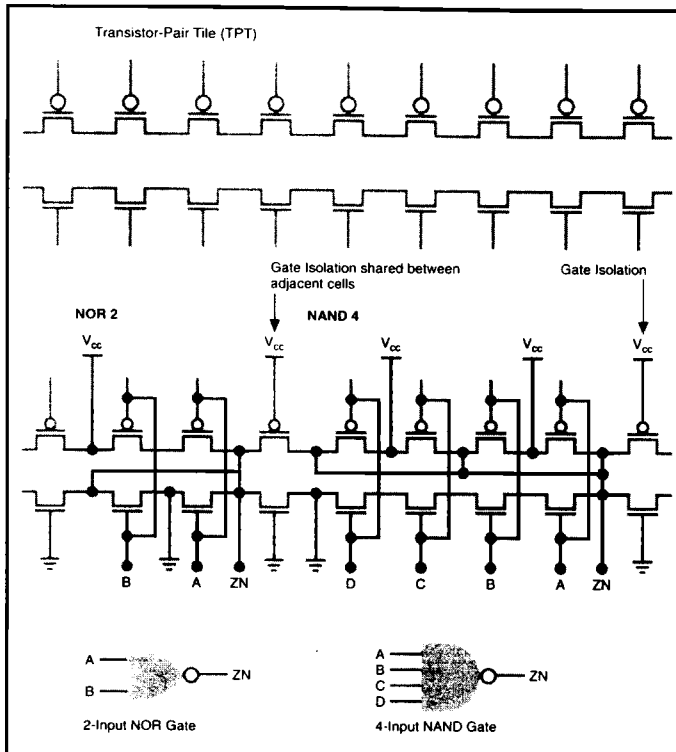
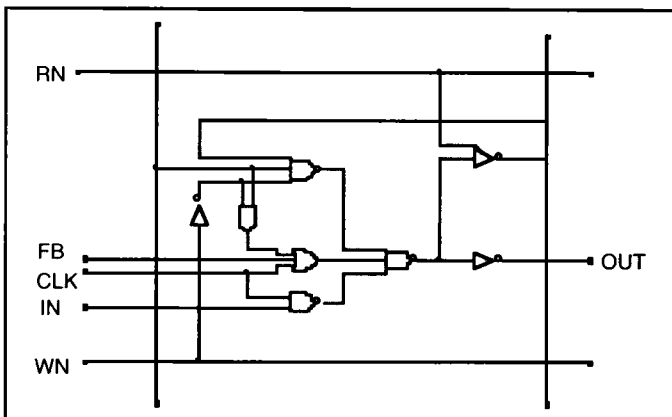


Figure 4. RAM Logic Tile (RLT) Logic Configuration

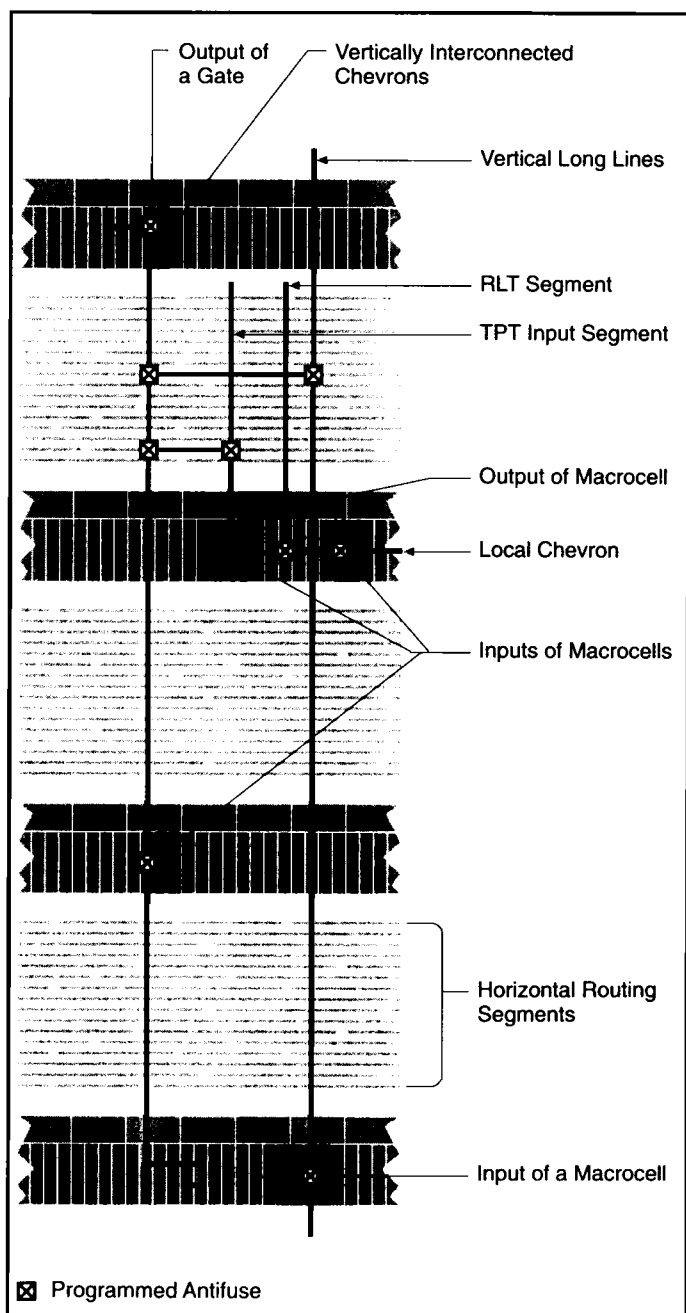


Routing Channels

While some intercell connections are made inside logic rows (local routing), the majority are made through routing channels. Each routing channel consists of a set of horizontal wire segments (figure 5). The lengths of the wire segments vary from a minimum of eight TPTs to the entire length of the row. The quantity, lengths, and positions of the segments are all derived from gate array connectivity statistics. Similar to the logic row, the routing channel has antifuses at each intersection of horizontal and vertical wire.

An approximately equal number of vertical and horizontal interconnect resources exist on each chip. Three types of vertical resources are available. The first is the vertically interconnected chevron (one for every two TPTs) which is a floating wire that originates from a TPT, spans five TPTs horizontally and goes vertically up or down four rows, and finally spans five or more TPTs horizontally. The second is the TPT/RLT input segment which originates from a p-channel gate of a TPT or from one of four ports of an RLT and spans the width of the routing channel immediately above it. The third is the

Figure 5. Routing Channel Structure and a Routing Path Use Vertical and Horizontal Interconnects



vertical long line, a floating wire that traverses several logic rows at a time. Long lines are either full height or half height, one in every four long lines is half height.

Input and Output Cells

As with NEC's MPGAs, many configuration options exist for each I/O cell in the CP20K family. Input cells come with CMOS or TTL thresholds, Schmitt trigger in 7 pins, and with or without pull-up. Output cells can be normal, three-state, open-drain or open-source, and have an optional output latch. The bidirectional cells can take any combination of the input and output cells, with the exception of Schmitt trigger.

I/O buffer circuits, each with a bonding pad terminal, are arranged in a ring around the perimeter of the array. Each I/O buffer can be configured to be an input, an output, a three-state output, or a bidirectional buffer. Options are available to select drive strength, slew-rate control for noise reduction, input voltage levels (CMOS or TTL) and weak pull-up. The connection of I/O cells to the array, figure 6, show four wire segments (DI, DO, DL, DE), which extend from each I/O cell into the routing channel. This allows very fast access to the cells in the core.

Clock Network

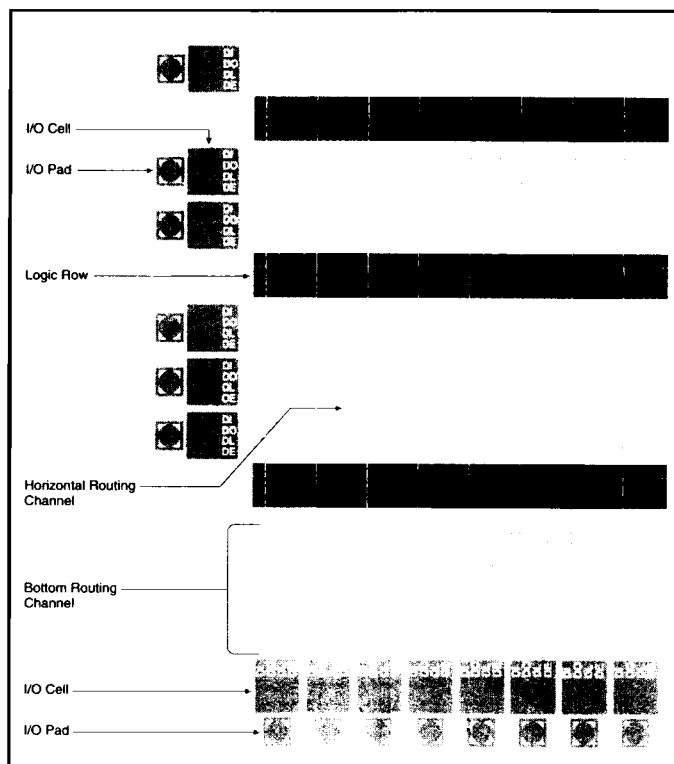
The CP20K series features a highly flexible and low-skew clock architecture (1.0 ns worst-case clock skew). Clock signals originate from the core array or directly from an I/O pin and may be distributed either into the core array or to output buffers around the perimeter (figure 7).

Four pin locations (CLKA, CLKB, CLKC and CLKD) are designated as clock input pins and have CMOS input thresholds. If these pins are not used as clock inputs, they may be used as Schmitt trigger inputs with either TTL or CMOS thresholds. (When used as Schmitt trigger inputs, the clock system is bypassed; the signal is routed directly into the core array). There are eight possible points in the core (T1, T2, T3, T4, T6, T7, and T8) where internal signals can drive the clock networks.

Four independent clock networks or grids (CLK0, CLK1, CLK2, CLK3) are accessible by every cell in the array. Each clock line can be directly connected to the CLK inputs of the RLTs or to the gates of the p-channel transistors in the TPTs. These lines can also be used as global signals such as power-on enable or reset.

In addition to the four grids in the core array, there are five clock lines for distribution of clock signals to the I/O ring. One (P0) is the ring clock which is common to all I/O cells; each of the other four (P1, P2, P3, P4) cover half of the I/O cells and are called corner clocks or L

Figure 6. I/O Cell Structure and Interconnect Scheme Between I/O Cells and the Logic Array



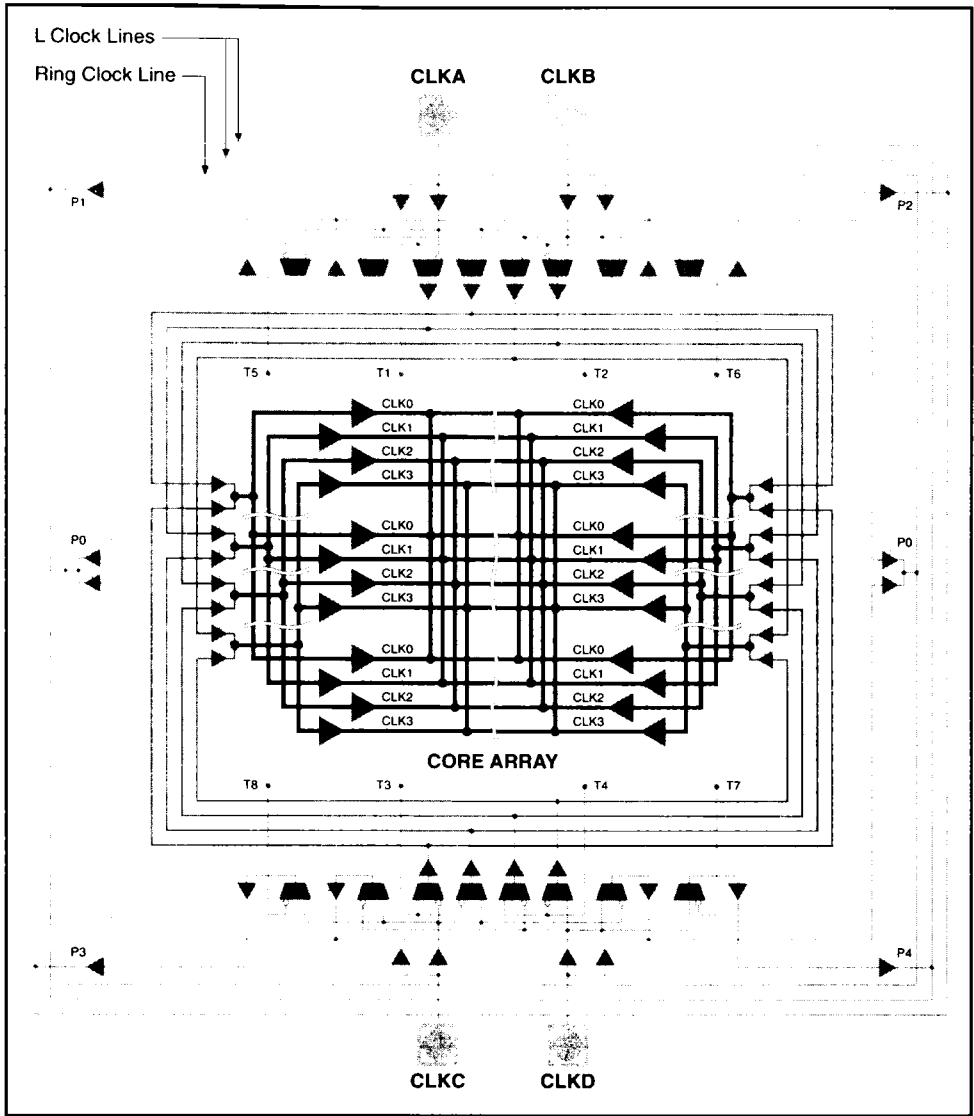
clocks. Each cell in the I/O ring is accessible by three clock lines: a ring clock and two L clocks. An I/O clock line can be connected to either the three-state enable pin or to the latch gate pin of an output or bidirectional buffer.

JTAG Boundary Scan

The CP20K series feature a boundary scan architecture that conforms to the IEEE Standard Access Port and Boundary-Scan Architecture, as defined in IEEE Standard 1149.1-1990. The boundary scan feature is used by the Crosspoint Programmer to load both the antifuse map vectors during programming, as well as the test vectors during functional testing. Boundary scan is a test method that uses a ring of registers at an IC's boundary to control and monitor access during testing, such as shown in figure 8. Full scan capabilities allow testing of every input and output of the device.

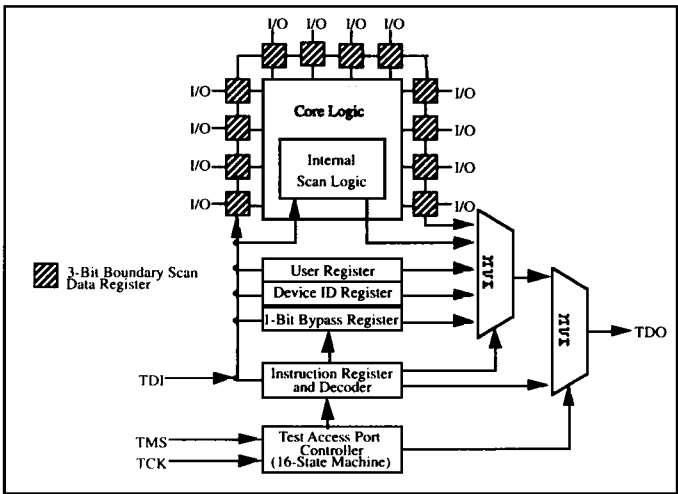
The IEEE 1149.1 standard dictates the following test logic: a data register, bypass register, instruction register, and test access port (TAP). The TAP controller responds to synchronous control signals. When these signals are applied through a 4-wire test port, they generate the control signals for the IEEE 1149.1 test structures on the chip. Four pins are designated as JTAG control pins. If the JTAG feature is not required, three of these pins can be used as Schmitt trigger inputs.

Figure 7. CP20K High Performance Clock Network



In addition to the basic functionality defined in IEEE 1149.1 standard for a JTAG port, Crosspoint provides the following features: a device identification register, a 32-bit configurable user register, a three-stage I/O scan capability, and internal scan capabilities which are accessed through the JTAG test logic (figure 8). Users can select library macros with logic for internal scan test. This boundary scan circuitry is implemented in each I/O cell and is independent of the I/O cell's user-defined configuration. Three boundary scan cells are provided per pad cell, one for each of the DE, DI, and DO signals since, in general, each pad cell can be configured as a bidirectional I/O buffer.

Figure 8. Boundary Scan Architecture



Absolute Maximum Ratings

Power supply voltage, V_{DD}	-0.5 to +7.0 V
Programming voltages, V_{PP} , V_{PB}	-0.5 to +10.5V
Input voltage, V_I	-0.5 V to $V_{DD} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	± 20 mA (typ)
Output current per pin ($V_O = 0$ to V_{DD})	± 25 mA
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	
Ceramic Package	-65 to +150°C
Plastic Package	-40 to +125°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; $f = 1$ MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	25	pF
Output	C_{OUT}	10	25	pF
I/O	$C_{I/O}$	10	25	pF

Note:

(1) Values include package pin capacitance.

Power Consumption

Description	Limits (max)	Unit	Test Conditions
Internal cell	15	μ W/MHz	F/O = 3
Input block	15	μ W/MHz	F/O = 3
Output block	.375	mW/MHz	$C_L = 15$ pF

Recommended Operating Conditions

Parameter	Symbol	CMOS Level		TTL Level		Unit
		Min	Max	Min	Max	
Power supply voltage	V_{DD}	4.5	5.5	4.75	5.25	V
Ambient temperature	T_A	-40	+85	0	+70	°C
Low-level input voltage	V_{IL}	0	$0.3 V_{DD}$	0	0.8	V
High-level input voltage	V_{IH}	$0.7 V_{DD}$	V_{DD}	2.0	V_{DD}	V
Input rise or fall time, normal inputs	t_R, t_F	0	250	0	250	ns
Input rise or fall time, Clock inputs	t_R, t_F	0	100	0	100	ns
Positive Schmitt-trigger voltage	V_P	2.3*	3.7*	1.4	2.4	V
Negative Schmitt-trigger voltage	V_N	1.2*	2.5*	0.8	1.8	V
Hysteresis voltage	V_H	0.5	1.6	0.4	1.2	V

* As an option, three JTAG pins and four clock inputs are required for a Schmitt trigger. Other I/Os have only TTL and CMOS input threshold options.

AC Characteristics

$V_{DD} = 5$ V $\pm 10\%$; $T_A = -40$ to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Delay time, internal gate	t_{PD}		0.968		ns	F/O = 1
Delay time, 2-input NAND gate			2.5		ns	F/O = 3
Delay time, buffer						
Input (BFIC)	t_{PD}		2.4		ns	F/O = 3
Output (BF04)	t_{PD}		5.3		ns	$C_L = 15$ pF
Output rise time	t_R		5.4		ns	$C_L = 15$ pF
Output fall time	t_F		5.3		ns	$C_L = 15$ pF

DC Characteristics

$V_{DD} = 5\text{ V} \pm 10\%$; $T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current (Note 1)	I_L				μA	$V_I = V_{DD}$ or GND
Input leakage current						
Regular	I_I	-10		10	μA	$V_I = V_{DD}$ or GND
Pull-up	I_I	-250		-250	μA	$V_I = \text{GND}$
Off-state output leakage current	I_{OZ}	-10		10	μA	$V_O = V_{DD}$ or GND
Low-level output current (CMOS)						
4 mA (Note 2)	I_{OL}	4			mA	$V_{OL} = 0.4\text{ V}$
8 mA (Note 2)	I_{OL}	8			mA	$V_{OL} = 0.4\text{ V}$
12 mA (Note 2)	I_{OL}	12			mA	$V_{OL} = 0.4\text{ V}$
High-level output current (CMOS)						
4 mA (Note 2)	I_{OH}	-2			mA	$V_{OH} = 3.7\text{ V}$
8 mA (Note 2)	I_{OH}	-4			mA	$V_{OH} = 3.7\text{ V}$
12 mA (Note 2)	I_{OH}	-8			mA	$V_{OH} = 3.7\text{ V}$
Low-level output current (TTL)						
4 mA (Note 3)	I_{OL}	4			mA	$V_{OL} = 0.4\text{ V}$
8 mA (Note 3)	I_{OL}	8			mA	$V_{OL} = 0.4\text{ V}$
12 mA (Note 3)	I_{OL}	12			mA	$V_{OL} = 0.4\text{ V}$
High-level output current (TTL)						
4 mA (Note 3)	I_{OH}	-4			mA	$V_{OH} = 3.0\text{ V}$
8 mA (Note 3)	I_{OH}	-8			mA	$V_{OH} = 3.0\text{ V}$
12 mA (Note 3)	I_{OH}	-12			mA	$V_{OH} = 3.0\text{ V}$
Low-level output voltage	V_{OL}			0.4	V	$I_{OL} = 4, 8, 12\text{ mA}$
High-level output voltage (CMOS) (Note 2)	V_{OH}	-3.7			V	$I_{OH} = -2, -4, -8\text{ mA}$
High-level output voltage (TTL) (Note 3)	V_{OH}	3.0			V	$I_{OH} = -4, -8, -12\text{ mA}$

Notes:

- (1) Outputs are floating.
- (2) CMOS-level output buffer ($V_{DD} = 5\text{ V} \pm 10\%$, $T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$).
- (3) TTL-level output buffer ($V_{DD} = 5\text{ V} \pm 5\%$, $T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$).

CP20K FPGA Package Options

Maximum I/O Pins	Package Dimensions		Master Slice					
	Body Size (mm /in.)	Pin Pitch (mm/in.)	CP20220	CP20420	CP20840	CP21200	CP21600	CP22000
Plastic Quad Flatpack (PQFP)								
160-pin	28 / 1.1	0.65 / .0256	–	P	E	–	–	–
208-pin	28 / 1.1	0.5 / .0196	–	–	P	P	E	E
240-pin	32 / 1.26	0.5 / .0196	–	–	–	E	E	E
Ceramic Quad Flatpack (CQFP)								
160-pin	28 / 1.1	0.65 / .0256	–	A	E	–	–	–
208-pin	28 / 1.1	0.5 / .0196	–	–	P	P	E	E
240-pin	32 / 1.26	0.5 / .0196	–	–	–	E	E	E
Ceramic Pin Grid Array (CPGA)								
155-pin	42/ 1.5	2.54 / .100	–	A	–	–	–	–
223-pin	47 / 1.7	2.54 / .100	–	–	P	–	–	–
299-pin	52 / 2.0	2.54 / .100	–	–	–	A	–	–
383-pin	–	–	–	–	–	–	P	P
Plastic Leaded Chip Carrier (PLCC)								
84-pin	–	–	P	P	E	–	–	–

A = Available; P = Planned; "–" = Not Planned or Unavailable; E = Under Evaluation

Ordering Information

	CP	20420	CPGA	155	A	–	1	C
Part Number Prefix								
Part Number								
2.2K gates:	20220							
4.2K gates:	20420							
8.4K gates:	20840							
12K gates:	21200							
16K gates:	21600							
20K gates:	22000							
Package Type								
CPGA: Ceramic Pin Grid Array								
CQFP: Ceramic Quad Flat Pack								
PQFP: Plastic Quad Flat Pack								
PLCC: Plastic Leaded Chip Carrier								
Pin Count								
Die Revision								
A								
B								
Speed Selection								
1: High Speed								
0: Normal Speed								
Operating Temperature Range								
C: Commercial (0°C to +70°C)								
I: Industrial (-40°C to +85°C)								
M: Military (-55°C to +125°C)								

Publications

This data sheet contains preliminary specifications, package information, and operational data for the CP20K field programmable gate array family. Additional design information is available in NEC's CP20K FPGA Block Library and CP20K FPGA Design Manual. Contact your local NEC Design Center or the NEC Literature Center for further ASIC design information; see the back of this data sheet for locations and phone numbers.

NEC's MPGA/FPGA Design System

The CMOS-X Mask Programmable Gate Arrays (MPGAs) and CP20K Field Programmable Gate Arrays (FPGAs) are fully supported by NEC's network of ASIC Design Centers, listed on the back of this data sheet.

The design flow for these products is shown in figure 9. The user may follow the solid line route, starting with a CMOS-X MPGA and retargeting to the CP20K FPGA for prototyping. Alternately, one may follow the flow suggested by the grey lines, starting with the CP20K FPGA and retargeting to a CMOS-X MPGA. Users may enlist Design Center support at any step in the design flow before prototype fabrication or programmed parts. Among the various levels at which Design Center support may begin (level A through level E), Level C ("Verified Netlist") is the most popular interface.

NEC's MPGA/FPGA suite of development tools tie into many established Electronic Design Automation (EDA) tool environments for schematic entry, logic synthesis, simulation, timing analysis, fault analysis, test pattern generation, etc. (including those from Mentor, Viewlogic, Synopsys, Cadence, and others). This allows users to preserve their investment in EDA tools and training.

Sample CMOS-X MPGA design kits (including the CP20K FPGA Conversion Kit for Synopsys retargeting) are available at no charge to qualified users: contact an NEC ASIC Design Center for more information. (Note: Soft-

ware licensing is required—NEC reserves the right to prioritize support based on user requirements.) Placement and routing for MPGAs are done at NEC's ASIC Design Centers.

The CP20K FPGA tools consist of the design kits, shown in the table below, as well as the Crosspoint Design System (CDS) for the Crosspoint-specific portions of the design process.

The Crosspoint design kits include the following modules, depending on the EDA tool:

Synthesis models: libraries containing information on the functionality, size, and timing of library macrocells

Symbolic symbols: graphical representation created for each macrocell

Simulation models: describes the logical and timing functions of macrocells

Test vector translator: converts stimulus and response vectors from the simulator directly into a form that can be downloaded into the Crosspoint FPGA programmer; the programmer then tests the programmed FPGA for functionality

Delay back annotation: since delays are calculated with CPTOOLS prior to back-annotation, each simulator produces identical post-layout timing when using Crosspoint's simulation models with back-annotation; simulation timing is guaranteed on any platform using the CP20K Design Kit

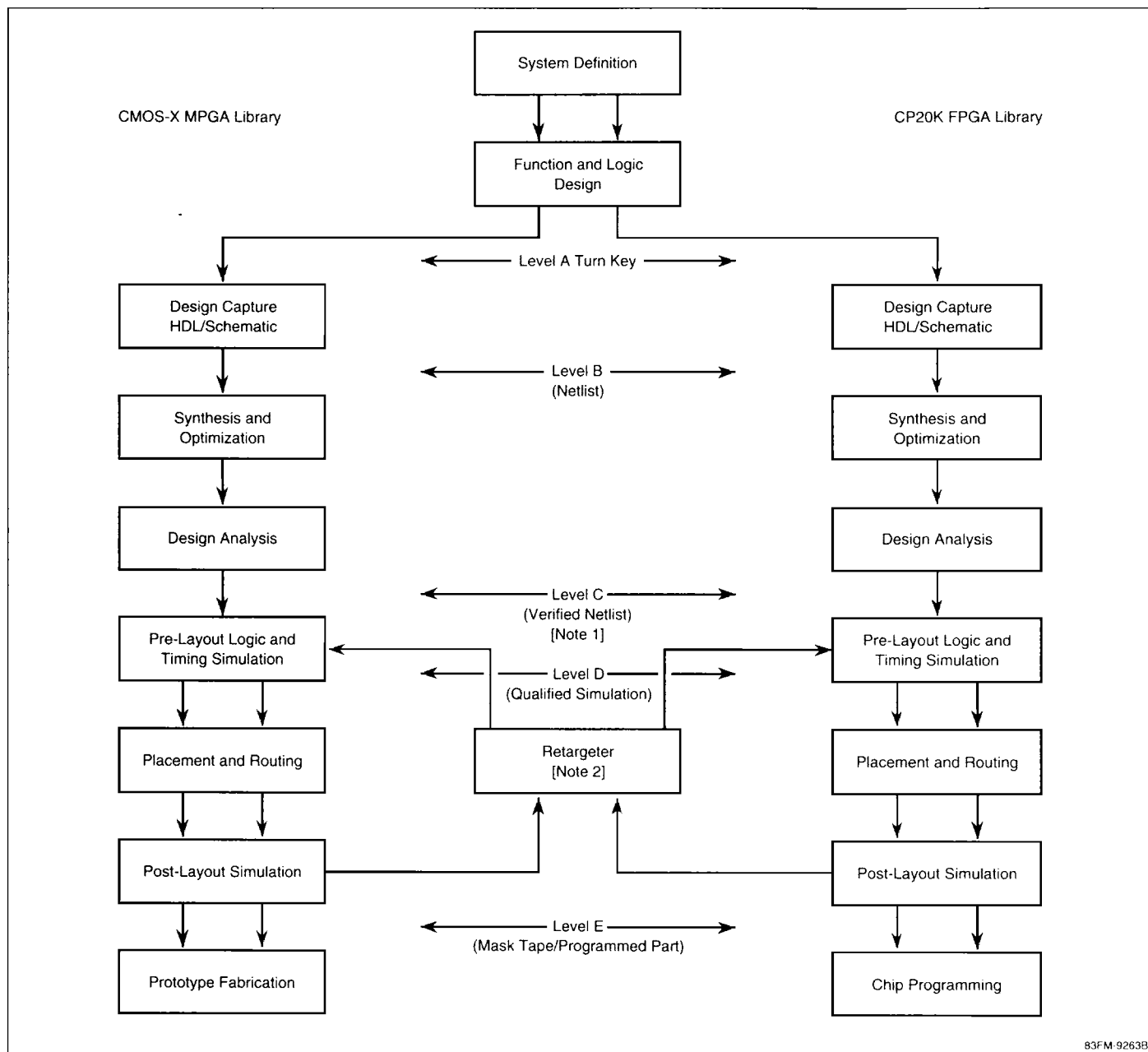
When design entry through the third-party tools is completed, the designs are transferred to CDS for placement and routing. The CDS is an integrated suite of automatic and interactive layout tools for this purpose. A single user interface controls all functions of the tools through pull-down menus, dialog boxes, and keyboard accelerators. The interface of information between the EDA vendor-specific tools and the CDS consist of EDIF netlists, pin delays, and test vectors.

CAD Tools offered for CP20K Designs

Vendor EDA	Synthesis	Schematic	Simulation	Timing Analysis	Fault Analysis
Mentor	—	A Design Architect	A Quicksim II	A Quickpath	P Quickfault/Quickgrade
Viewlogic	P VHDL Designer II	A Viewdraw	A Viewsim/SD	—	—
Synopsys	A Design Compiler	—	P VHDL System Simulator	A	—
Verilog	—	—	A Verilog-XL	P Veritime	P Verifault

A = Available; P = Planned; "—" = Not Planned or Unavailable

Figure 9. MPGA/FPGA Design Flow



83FM-9263B

Note 1: The CMOS-X and CP20K CAD tools supported include Mentor™, Viewlogic™, Synopsys™, and Verilog™.

Note 2: The Retargeter requires the FPGA Conversion Kit and Synopsys.

The functions of the CDS consist of the following:

Logic design mapping from an EDA tool into a CP20K FPGA layout

Package selection and pin assignment

Generation of delay for back-annotation to an EDA simulator

Generation of antifuse maps

Translation of test vectors for the Programmer

Communication with the Programmer during programming and testing of chips

The Crosspoint FPGA programmer/tester (figure 10) is used to convert the antifuse map from a completed place and route into a JTAG bitstream, clock and data into a CP20K packaged part, and program each required antifuse map. At the end of programming, users can verify the part by applying test vectors.

Programmer/Tester Features

Workstation communications: via SCSI interface and IEEE 1149.1 interface to the device to be programmed

2-line by 20-character LCD: for soft setup and local status during programming and testing

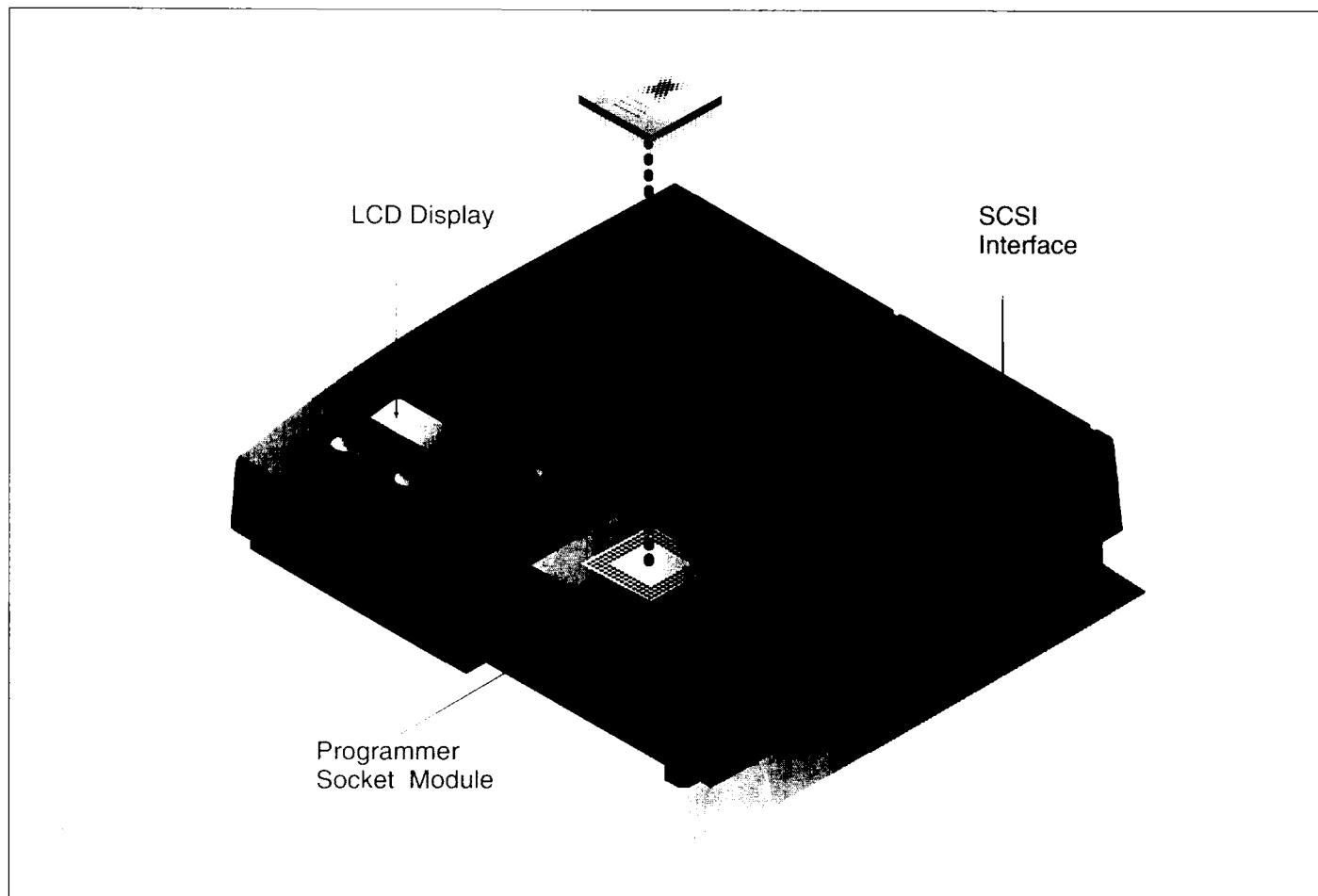
Pre-program testing: fuses open and I/O functionality test to ensure that the part has not been previously

programmed, or damaged from improper handling including ESD, and all connections for programming are present

Post-program synchronous functional testing: slow-speed synchronous test that checks functionality of device only, not speed or timing parameters, done through the IEEE 1149.1 interface using INTEST mode

Socket modules: to accommodate all package types

Figure 10. Programmer/Tester



CP20K FPGAs

Block Library List

The CP20K family of FPGAs offer a variety of blocks, including logic gates, arithmetic functions, latches, flip-flops and RAM. Most of the functions of these blocks are compatible with CMOS-6 MPGAs.

Block List

CP20K Block Name	CMOS-6 Block Name	Description	I _{OL} (mA)
Interface Blocks			
Input Buffers			
BFIC	FI01	CMOS Input Buffer	
BFIT	FI02	TTL Input Buffer	
BFICS	FIS1	CMOS Schmitt Input Buffer	
BFITS	FIS2	TTL Schmitt Input Buffer	
BFICU	FIW1	CMOS Pull-up Input Buffer	
BFITU	FIW2	TTL Pull-up Input Buffer	
Output Buffers			
BFO4	FO01	Output Buffer	4
BFO4R	FO01	Slew Output Buffer	4
BFO8	FO01	Output Buffer	8
BFO8R	FO01	Slew Output Buffer	8
BFO12	FO02	Output Buffer	12
BFO12R	FO02	Slew Output Buffer	12
BFT4	B00E	Tri-state Output Buffer	4
BFT4R	B00E	Tri-state Slew Output Buffer	4
BFT8	B008	Output Buffer	8
BFT8R	B008	Slew Output Buffer	8
BFD12	B007	Tri-state Output Buffer	12
BFD12R	B007	Tri-state Slew Output Buffer	12
BFD4	EXT1	Open Drain Output Buffer	4
BFD4R	EXT1	Open Drain Slew Output Buffer	4
BFD8	EXT1	Open Drain Output Buffer	8
BFD8R	EXT1	Open Drain Slew Output Buffer	8
BFD12	EXT9	Open Drain Output Buffer	12
BFD12R	EXT9	Open Drain Slew Output Buffer	12

CP20K Block Name	CMOS-6 Block Name	Description	I _{OL} (mA)
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Interface Blocks (cont)

Bi-directional I/O Buffers

BFB4C	B00C	CMOS Bidirect Buffer	4
BFB4CR	B00C	CMOS Slew Bidirect Buffer	4
BFB4T	B00D	TTL Bidirect Buffer	4
BFB4TR	B00D	TTL Slew Bidirect Buffer	4
BFB8C	B003	CMOS Bidirect Buffer	8
BFB8CR	B003	CMOS Slew Bidirect Buffer	8
BFB8T	B004	TTL Bidirect Buffer	8
BFB8TR	B004	TTL Slew Bidirect Buffer	8
BFB12C	B001	CMOS Bidirect Buffer	12
BFB12CR	B001	CMOS Slew Bidirect Buffer	12
BFB12T	B002	TTL Bidirect Buffer	12
BFB12TR	B002	TTL Slew Bidirect Buffer	12
BFB4CU	B0UC	CMOS Pull-up Bidirect Buffer	4
BFB4CRU	B0UC	CMOS Slew Pull-up Bidirect Buffer	4
BFB4TU	B0UD	TTL Pull-up Bidirect Buffer	4
BFB4TRU	B0UD	TTL Slew Pull-up Bidirect Buffer	4
BFB8CU	B0U3	CMOS Pull-up Bidirect Buffer	8
BFB8CRU	B0U3	CMOS Slew Pull-up Bidirect Buffer	8
BFB8TU	B0U4	TTL Pull-up Bidirect Buffer	8
BFB8TRU	B0U4	TTL Slew Pull-up Bidirect Buffer	8
BFB12CU	B0U1	CMOS Pull-up Bidirect Buffer	12
BFB12CRU	B0U1	CMOS Slew Pull-up Bidirect Buffer	12
BFB12TU	B0U2	TTL Pull-up Bidirect Buffer	12
BFB12TRU	B0U2	TTL Slew Pull-up Bidirect Buffer	12

Clock Buffers

BFCKGB	FIB1	Clock Driver: pad input, 2-port outputs
BFCKG1	FIB1	Clock Driver: pad input, inverting output
BFCKGN	FIB1	Clock Driver: pad input, non-inverting output
CKGB	FIB1	Clock Driver: internal input, 2-port outputs
CKGI	FIB1	Clock Driver: internal input, inverting output
CKGN	FIB1	Clock Driver: internal input, non-inverting output

CP20K Block Name	Description	CP20K Gates	TPTs, RLTs
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Function Blocks

Inverters

IN1	Inverter: 1X drive	1	2, 0
IN1N	Inverter	1	4, 0
IN1P	Inverter: 1X pull-down, 2X pull-up drive	1	4, 0
IN1R	Inverter: using RLT	1	0, 1
IN2	Inverter: 2X drive	1	4, 0
IN2P	Inverter: 2X pull-down, 3X pull-up drive	2	4, 0
IN2PP	Inverter: 2X pull-down, 4X pull-up drive	2	6, 0

Buffers

BI1	Internal buffer: 2-polar outputs	1	3, 0
NI1	Non-inverting buffer: 1X drive	1	3, 0
NI1R	Non-inverting buffer: using RLT	1	0, 1
NI2	Non-inverting buffer: 2X drive	1	4, 0

NOR Gates

NR2	2-input NOR	1	3, 0
NR3	3-input NOR	2	4, 0
NR4	4-input NOR	2	6, 0
NR5	5-input NOR	4	10, 0
NR6	6-input NOR	5	11, 0
NR8	8-input NOR	6	17, 0

OR Gates

OR2	2-input OR	2	5, 0
OR2H	High-drive 2-input OR	2	6, 0
OR2R	2-input OR using RLT	2	0, 1
OR3	3-input OR	2	5, 0
OR3H	High drive 3-input OR	3	6, 0
OR4	4-input OR	3	8, 0
OR5	5-input OR	5	9, 0
OR6	6-input OR	6	10, 0
OR8	8-input OR	5	15, 0

NAND Gates

ND2	2-input NAND	1	3, 0
ND2R	2-input NAND using RLT	1	0, 1
ND3	3-input NAND	2	4, 0
ND4	4-input NAND	2	5, 0
ND5	5-input NAND	4	10, 0
ND5L	Minimum-area 5-input NAND	3	6, 0
ND6	6-input NAND	5	11, 0
ND8	8-input NAND	6	15, 0

AND Gates

AN2	2-input AND	2	5, 0
AN2H	High drive 2-input AND	2	6, 0
AN2I	2-input AND with 1 inverted input	2	0, 1
AN3	3-input AND	2	5, 0
AN3H	High drive 3-input AND	3	6, 0
AN4	4-input AND	3	7, 0
AN4H	High drive 4-input AND	3	8, 0
AN5	5-input AND	4	9, 0
AN5H	High drive 5-input AND	4	8, 0
AN5L	Minimum-area 5-input AND	3	7, 0
AN6	6-input AND	5	10, 0
AN8	8-input AND	5	13, 0

CP20K Block Name	Description	CP20K Gates	TPTs, RLTs
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Function Blocks

AND-NOR Gates

AO21	2-input AND into 2-input NOR	2	5, 0
AO211	2-input AND into 3-input NOR	2	5, 0
AO2111	2-input AND into 4-input NOR	2	7, 0
AO22	Two 2-input ANDs into 2-input NOR	2	6, 0
AO221	Two 2-input ANDs into 3-input NOR	2	8, 0
AO2211	Two 2-input ANDs into 4-input NOR	2	9, 0
AO222	Three 2-input ANDs into 3-input NOR	5	14, 0
AO31	3-input ANDs into 2-input NOR	2	6, 0
AO311	3-input AND into 3-input NOR	2	6, 0
AO3111	3-input AND into 4-input NOR	3	8, 0
AO32	3-input AND, 2-input AND into 2-input NOR	5	7, 0
AO321	3-input AND, 2-input AND into 3-input NOR	5	9, 0
AO3211	3-input AND, 2-input AND into 4-input NOR	5	9, 0
AO33	Two 3-input ANDs into 2-input NOR	5	8, 0
AO41	4-input AND into 2-input NOR	4	7, 0
AO42	4-input AND, 2-input AND into 4-input NOR	6	9, 0
MJ23	Majority of 2-of-3 Inverting "Voter"	3	6, 0

OR-NAND Gates

OA21	2-input OR into 2-input NAND	2	5, 0
OA211	2-input OR into 3-input NAND	2	5, 0
OA22	Two 2-input ORs into 2-input NAND	2	7, 0
OA222	Three 2-input ORs into 3-input NAND	5	14, 0
OA2222	Four 2-input ORs into 4-input NAND	7	20, 0

Exclusive-OR Functions

XN2	2-input XNOR	4	2, 1
XN2A	2-input OR, 2-input NAND into 2-input NAND	3	7, 0
XN2T	2-input XNOR using TPTs	3	6, 0
XN3	3-input XNOR	7	2, 0
XO2	2-input XOR	3	0, 1
XO2A	2-input AND, 2-input NOR into 2-input NOR	3	7, 0
XO2T	2-input XOR using TPTs	3	6, 0
XO3	3-input XOR	6	0, 2
XO3T	3-input XOR using TPTs	6	12, 0

Parity Generators

CLS180*	8-bit odd/even parity generator/checker	26	—
CLS280*	9-bit odd/even parity generator/checker	37	—

Adders

FA1	1-bit full-adder	10	2, 3
HA1	1-bit half-adder	5	5, 1
CLS82*	2-bit full-adder	14	—
CLS181*	Arithmetic logic unit/function generator	94	—
CLS182*	Look-ahead carry generator	29	—
CLS183*	Dual carry save full-adders	26	—
CLS283*	4-bit binary full-adder with fast carry	62	—

Miscellaneous

MX8x9*	1 of 8-9 bit wide multiplexer bus	224	92, 45
MX8x18*	1 of 8-18 bit wide multiplexer bus	440	160, 90
MX16x9*	1 of 16-9 bit wide multiplexer bus	417	192, 81
MX16x18*	1 of 16-18 bit wide multiplexer bus	773	326, 152

Note: * Macrofunction library: contact NEC for availability;
CLS prefix indicates compatibility with TTL74 series functions

CP20K Block Name	Description	CP20K Gates	TPTs, RLTs
Function Blocks			
Tri-State Buffers			
IT1	Inverting tri-state buffer: 1X drive	1	3, 0
IZ1	Inverting tri-state bus receiver	2	9, 0
NT1	Non-inverting tri-state buffer: 1X drive	1	3, 0
NZ1	Non-inverting tri-state bus receiver	1	9, 0
Decoders/Encoders			
DE12*	1 to 2 decoder	4	—
DE24*	2-bit decoder	8	—
DE24G*	2-bit decoder, with enable	11	—
DE38G*	3-bit decoder, with enable	18	—
CLS137*	3-to-8 decoder/demultiplexer with address latches	36	—
CLS138*	3-to-8 decoder/demultiplexer	22	—
CLS139*	Dual 2-to-4 decoder/demultiplexer	22	—
CLS154*	4-to-6 decoder/demultiplexer	87	—
CLS155*	Dual 2-to-4 decoder/demultiplexer	21	—
CLS148*	8-to-3 priority encoder	44	—
CLS147*	10-to-4 priority encoder	41	—
Multiplexers			
MX21	2 to 1 MUX, non-inverting	4	2, 1
MX21N	2 to 1 MUX, inverting	3	2, 1
MX21NT	2 to 1 MUX, inverting using TPTs	3	6, 0
MX21T	2 to 1 MUX, non-inverting using TPTs	4	7, 1
MX21X	2 to 1 MUX, inverting input D1	4	0, 1
MX21XT	2 to 1 MUX, inverting input D1 using TPTs	4	8, 0
MX31	3 to 1 MUX, non-inverting	8	4, 1
MX31N	3 to 1 MUX, inverting	7	2, 2
MX31X	3 to 1 MUX, inverting inputs D1 and D2	6	0, 2
MX41	4 to 1 MUX, non-inverting	14	4, 3
MX41T	4 to 1 MUX, non-inverting using TPTs	6	16, 0
MX51	5 to 1 MUX, non-inverting	19	6, 4
MX81	8 to 1 MUX, non-inverting	32	8, 7
CLS97*	MUX: synchronous 6-bit binary rate	136	—
CLS150*	Selector/MUX: 16-bit data	98	—
CLS151*	Selector/MUX: 1-of-8 data, strobe	51	—
CLS152*	Selector/MUX: 1-of-8 data	24	—
CLS157*	Selector/MUX: quadruple 2-of-1 data, non-inverted out	15	—
CLS158*	Selector/MUX: quadruple 2-of-1 data, inverted out	11	—
CLS298*	MUX: quadruple 2-input, storage	34	—
Latches			
LDNB	D-Latch: clear, set, gate active low	5	9, 1
LDNC	D-Latch: clear, gate active low	4	5, 1
LDNN	D-Latch: gate active low	3	2, 1
LDNS	D-Latch: set, gate active low	4	6, 1
LDPB	D-Latch: clear, set, gate active high	5	7, 1
LDPC	D-Latch: clear, gate active high	4	7, 1
LDPN	D-Latch: gate active high	3	2, 1
LDPS	D-Latch: set, gate active high	4	6, 1
LSNN	SR-Latch: set, and reset are asserted low	4	0, 2
LDP4*	4-bit D-Latch	20	—
LDPC4*	4-bit D-Latch: CLR	26	—
CLS259*	8-bit addressable latch	87	—

CP20K Block Name	Description	CP20K Gates	TPTs, RLTs
Function Blocks			
Flip-Flops			
FDP1B	Positive triggered DFF: set, clear	7	15, 2
FDP1BB	Positive triggered DFF: set, clear, 2-polar outputs	9	15, 2
FDP1BL	Positive triggered DFF: set, clear, scan MUX	12	17, 2
FDP1C	Positive triggered DFF: clear,	9	7, 2
FDP1CB	Positive triggered DFF: clear, 2-polar outputs	6	8, 2
FDP1CL	Positive triggered DFF: clear, scan MUX	14	9, 3
FDP1N	Positive triggered DFF	6	3, 2
FDP1NB	Positive triggered DFF: 2-polar outputs	7	3, 2
FDP1NL	Positive triggered DFF: scan MUX	11	5, 3
FDP1S	Positive triggered DFF: set	8	10, 2
FDP1SB	Positive triggered DFF: set, 2-polar outputs	8	9, 2
FDP1SL	Positive triggered DFF: set, scan MUX	13	12, 3
FJP1B	Positive triggered JK-FF: set, clear	11	15, 3
FJP1BB	Positive triggered JK-FF: set, clear, 2-polar outputs	12	17, 3
FJP1BL	Positive triggered JK-FF: set, clear, scan MUX	16	17, 4
FJP1C	Positive triggered JK-FF: clear,	13	7, 3
FJP1CB	Positive triggered JK-FF: clear, 2-polar outputs	14	9, 3
FJP1CL	Positive triggered JK-FF: clear, scan MUX	18	9, 4
FJP1N	Positive triggered JK-FF	10	3, 3
FJP1NB	Positive triggered JK-FF: 2-polar outputs	11	5, 3
FJP1NL	Positive triggered JK-FF: scan MUX	15	5, 4
FJP1S	Positive triggered JK-FF: set	12	10, 3
FJP1SB	Positive triggered JK-FF: set, 2-polar outputs	13	12, 3
FJP1SL	Positive triggered JK-FF: set, scan MUX	17	12, 4
FTP1C	Positive triggered toggle-FF: clear	8	8, 2
FDP1S	Positive triggered toggle-FF: set	8	9, 2
FDP4*	4-bit DFF	28	—
FDPC4*	4-bit DFF: clear	33	—
Shift Registers			
LFR2*	2-bit shift register	10	—
LFRC2*	2-bit shift register: CLR	12	—
LFRB2*	2-bit shift register: CLR, SET	14	—
LFRC4*	4-bit shift register: CLR	23	—
CLS91*	8-bit shift register	41	—
CLS94*	4-bit shift register	49	—
CLS95*	4-bit shift register	35	—
CLS96*	5-bit shift register: dual parallel-in, parallel-out	53	—
CLS164*	8-bit shift register: parallel-out	53	—
CLS165*	8-bit shift register: parallel-load	84	—
CLS166*	8-bit shift register: parallel-load	76	—
CLS194*	4-bit shift register: bidirectional universal	63	—
CLS195*	4-bit shift register: parallel access	41	—
CLS198*	8-bit shift register: parallel-in, parallel-out bidirectional	95	—
CLS199*	8-bit shift register: parallel-in, parallel-out, JK input	79	—

Note: * Macrofunction library: contact NEC for availability;
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CP20K Block Name	Description	CP20K Gates	TPTs, RLTs
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Function Blocks

Counters

CLS90*	Counter: decade	39	—
CLS92*	Counter: divide-by-12	32	—
CLS93*	Counter: 4-bit binary	32	—
CLS98*	4-bit data selector/storage register	34	—
CLS99*	4-bit right-shift left-shift register	42	—
CLS160*	Counter: synchronous decade	75	—
CLS161*	Counter: synchronous 4-bit binary	76	—
CLS162*	Counter: fully synchronous decade	72	—
CLS163*	Counter: fully synchronous 4-bit binary	74	—
CLS168*	Counter: synchronous decade up/down	87	—
CLS169*	Counter: synchronous binary up/down	77	—
CLS176*	Counter: presettable decade	65	—
CLS177*	Counter: presettable 4-bit binary	57	—
CLS190 [†]	Counter: synchronous up/down decade, single clock	92	—
CLS191*	Counter: synchronous up/down 4-bit, single clock	87	—
CLS192*	Counter: synchronous up/down decade, dual clock	82	—
CLS193*	Counter: synchronous up/down 4-bit, dual clock	78	—
CLS290*	Counter: decade	40	—
CLS293*	Counter: 4-bit binary	32	—
CLS390*	Counter: dual decade	66	—
CLS393*	Counter: dual 4-bit binary	58	—
CLS490*	Counter: dual 4-bit decade	76	—
CLS668*	Counter: synchronous up/down decade	89	—
CLS669*	Counter: synchronous up/down 4-bit binary	78	—

Comparators

CMP4*	4-bit equality comparator	12	—
CMP85*	4-bit magnitude comparator	70	—

CP20K Block Name	Description	CP20K Gates	TPTs, RLTs
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Memory Blocks

RAM Blocks (Fixed-Place)

RAM8x4*	8 word by 4 bits	186	100, 36
RAM16x4*	16 word by 4 bits	332	110, 72
RAM32x4*	32 word by 4 bits	631	130, 144
RAM64x4*	64 word by 4 bits	1232	204, 288
RAM8x8*	8 word by 8 bits	334	108, 72
RAM16x8*	16 word by 8 bits	624	122, 144
RAM32x8*	32 word by 8 bits	1215	150, 288
RAM64x8*	64 word by 8 bits	2408	264, 576
RAM8x9*	8 word by 9 bits	371	110, 81
RAM16x9*	16 word by 9 bits	697	125, 162
RAM32x9*	32 word by 9 bits	1361	155, 324
RAM8x16*	8 word by 16 bits	630	124, 144
RAM16x16*	16 word by 16 bits	1208	146, 288
RAM32x16*	32 word by 16 bits	2383	190, 576
RAM8x32*	8 word by 32 bits	1222	156, 288
RAM16x32*	16 word by 32 bits	2376	194, 576

Note: * Macrofunction library: contact NEC for availability;
CLS prefix indicates compatibility with TTL74 series functions