



SANYO Semiconductors

DATA SHEET

LA3883M

Monolithic Linear IC

For Car television

**SIF + noise canceller + Japanese television
sound multiplex demodulator.**

Overview

The LA3883M is a signal processing IC for car TV systems, which incorporates TV SIF, noise canceller, and sound multiplex demodulator on a single chip.

Functions

[SIF block]

- OSC circuit built-in.(f = 43.55MHz)
- Differential IF amplifier
- S meter output 6-phase pick-up.
- AF pre-amplifier
- SD output (operating with remote mute)
- Noise canceller block
- Twin pulse noise elimination
 - main pulse noise elimination
 - Sub pulse noise elimination
- Diversity switching noise elimination

- MIXER
- IF limiter amplifier
- Quadrature type detector
- Small input muting
- Independent setting of noise focused point and mute start point.

[Sound multiplex demodulation block]

- Stereo/bilingual supported
- Q-BPF, SUB-BPF, and DE-EMPHASIS built-in.
- Q signal detection function 922.5Hz(BIL), 982.5Hz(ST) detection
- SUB signal demodulation function pulse count detection
- MAIN/SUB/DUAL output signal switching function
- STEREO/BILINGUAL display output
- MUTE function
- MRC(Multi pass noise Reduction Circuit)built-in.

- SNC/HCC

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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		10	V
Allowable power dissipation	Pd max	Ta ≤ 85°C *	1000	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-40 to +150	°C

* Mounted on a 114.3mm×76.1mm×1.6mm, glass epoxy board.

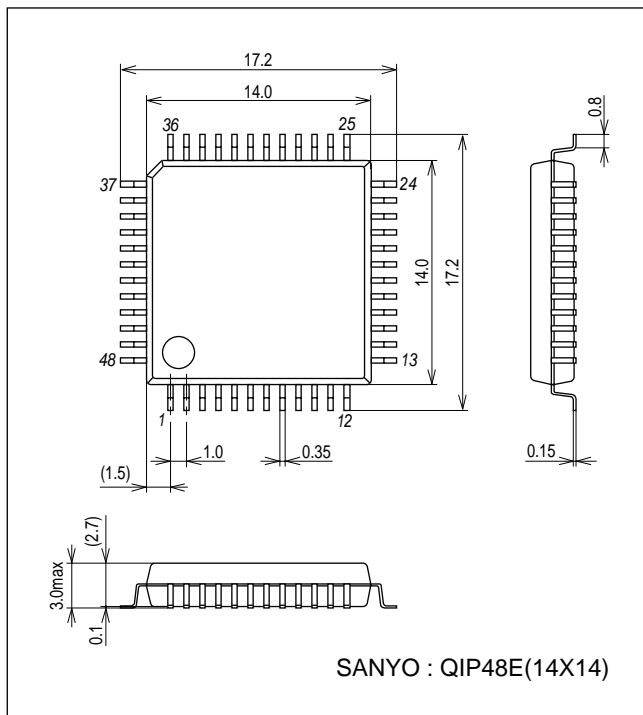
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		8	V
Operating supply voltage	V _{CC} op		7.5 to 8.5	V
Input signal voltage	V _{IN}	MONO, 100% mod	80	mV

Package Dimensions

unit : mm (typ)

3156A



Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 8\text{V}$

Parameter	Symbol	Input Conditions	Test Conditions	min	typ	max	unit
Current drain	I _{CCO}	No signal		80	100	115	mA
Mixer block (Mixer input – Mixer output)							
Mixer change output level	V _{O-Mix}	fr = 54.25MHz, 100dB _i -IN, Non-dev.	Mixer coil output load resistance = 330Ω Mixer output (10.7MHz) level	175	250	350	mVrms
SIF block (IF input – IF output)							
Detection output	V _{O-IF}	Unless otherwise specified, fr = 10.7MHz, 100dB _i -IN fm = 1kHz, 25kHz-dev.	Unless otherwise specified, PIN24, IHF-BPF IN	70	95	125	mVrms
Distortion ratio	THD-IF				0.5	0.9	%
S/N ratio	S/N-IF			61	68		dB
AM control ratio	AMR	IF-IN = 90dB _i , AM30% mod, fm = 1kHz		50	57		dB
Input limiting voltage	V _{i-Lim}	Input level at which output level becomes -3dB.		34	34	40	dB _μ
SD sensitivity	SD-sen	2·1PIN→LOW, R33 = 15kΩ Input level that becomes SD-ON.	PIN32 output (DC)	58	68	78	dB _μ
Muting sensitivity	V _{i-Mute}	Input level that becomes V26 = 2V, R26 = 22kΩ	PIN26 voltage (DC)	24	29	35	dB _μ
Muting band	BW	Frequency band width that becomes V26 < 2V.	PIN26 voltage (DC)	80	150	240	kHz
S meter output	V _{IN} = no input	V _{IN} = 0dB _μ , Non-modulation, R31 = 22kΩ			0.1	0.3	V
	V _{IN} = 60dB _μ	V _{IN} = 60dB _μ , Non-modulation		0.5	1.2	2.0	V
	V _{IN} = 80dB _μ	V _{IN} = 80dB _μ , Non-modulation		2.0	3.1	4.2	V
	V _{IN} = 100dB _μ	V _{IN} = 100dB _μ , Non-modulation		4.0	5.1	6.2	V
Mute drive output	V _{i-Mute}	V _{IN} = 100dB _μ , Non-modulation	PIN26 voltage (DC)			0.2	V
Sound multiplex demodulation block							
Output level	V _O	Unless otherwise specified, fm=1kHz, : Referenced to MONO = 100% (80mVrms)	Unless otherwise specified, PIN13, IHF-BPF IN	285	360	450	mVrms
Output channel balance	CB		PIN13/14 output level difference	-1.5	0	+1.5	dB

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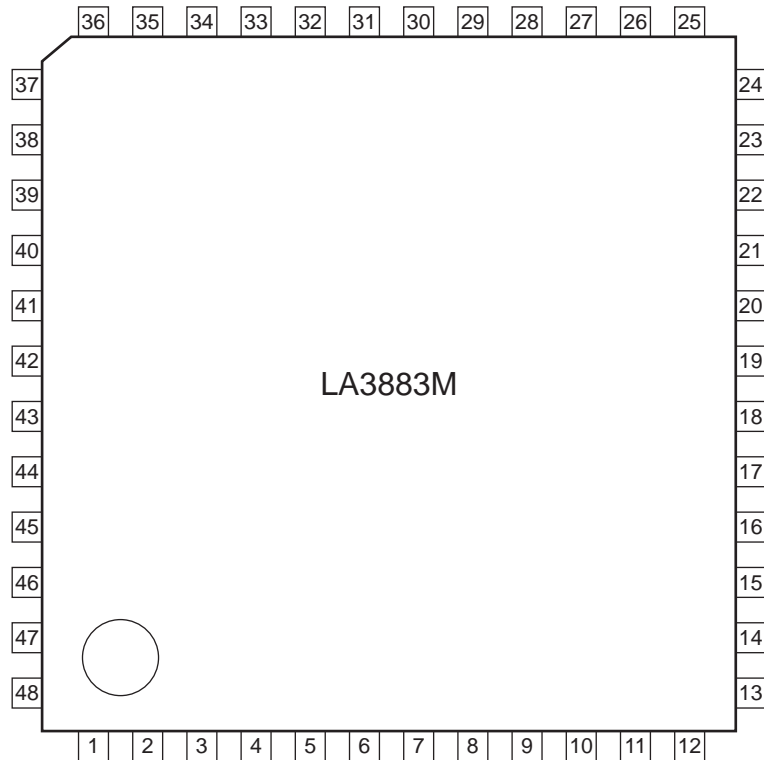
Parameter	Symbol	Input Conditions	Test Conditions	min	typ	max	unit
S/N ratio	MONO			55	62		dB
	ST	L+R = 100%		52	59		dB
	BIL-M/M	MAIN = 100%, V39 = Low		52	62		dB
	BIL-S/S	SUB = 100%, V39 = High		50	58		dB
Output channel separation	SEP	L or R signal input	Output level difference for L/R input. (When adjusted to Sep max with Sep. ADJ.)	25	35		dB
SNC-1 (V _{snc} = separation for 0.5V)	SNC-1	Separation when VSNC (pin 7) = 0.5V.		3	7	11	dB
SNC-2 (V _{snc} = separation for 0.1V)	SNC-2	Separation when VSNC (pin 7) = 0.1V.		0	0.3	1	dB
HCC output attenuation	HCC-1	f _m = 10kHz, MONO Attenuation when VHCC (PIN9) = 0.5V.	Attenuation from output level when VHCC = 3V.	-3.5	-6	-8.5	dB
	HCC-2	f _m = 10kHz, MONO Attenuation when VHCC (PIN9) = 0.1V.	Attenuation from output level when VHCC = 3V.	-6.5	-9	-11.5	dB
Distortion	MONO				0.5	1.2	%
	ST-L+R	L+R = 100%			0.5	1.2	%
	SUB	SUB = 100%			0.9	2.0	%
Q detection sensitivity	ST	PIN = 21 → High Calculated level for L+R.	The level at which pin 32 becomes Low.		20	45	mVrms
	BIL	Calculated level for MAIN.	The level at which pin 21 becomes Low.		20	45	mVrms
Capture range	ST+	Detection range (+ side) when the Q signal (982.5 Hz) frequency is variable.	(Limited frequency/982.5) × 100 [%]		+0.66		%
	ST-	Detection range (- side) when the Q signal (982.5 Hz) frequency is variable.	(Limited frequency/982.5) × 100 [%]		-0.45		%
	BIL+	Detection range (+ side) when the Q signal (922.5 Hz) frequency is variable.	(Limited frequency/922.5) × 100 [%]		+0.70		%
	BIL-	Detection range (- side) when the Q signal (922.5 Hz) frequency is variable.	(Limited frequency/922.5) × 100 [%]		-0.27		%

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Parameter	Symbol	Input Conditions	Test Conditions	min	typ	max	unit
Crosstalk	MAIN→S/S	MAIN=100%	Main signal leak level for the SUB/SUB mode.	44	49		dB
	SUB→M/M	SUB=100%	SUB signal leak level for the MAIN/MAIN mode.	53	60		dB
Mode switching voltage	MAIN	Pin 39 voltage for switching to the SUB/SUB mode.		GND		0.5	V
	DUAL	Pin 39 voltage for switching to DUAL mode.		1.7		3.2	V
	SUB	Pin 39 voltage for switching to MAIN/MAIN mode.		4.5		V _{DD}	V
Output DC offset	MONO/ST	mod. = 0%	Output DC voltage difference for MONO/ST.	-80		+80	mV
	MONO/BIL	mod. = 0%	Output DC voltage difference for MONO/BIL.	-80		+80	mV
	MONO/MUTE	mod. = 0%	Output DC voltage difference for MONO/MUTE.	-100		+100	mV
Mute sensitivity (V ₂₅ = 2.5V)	ATT	Output attenuation when V ₂₅ = 0→2V.		28	35	42	dB
MRC block							
MRC output	MRC-OUT	V ₁₀ = 2.5V, PIN35 input (70kHz, 5mVrms)	PIN8 output voltage (DC)	1.9	2.05	2.2	mVrms
MRC operating level	MPC OP	Pin 35 input level (f _c = 70kHz) that becomes V ₁₀ = 2.5V, V _B = 1.5V.	PIN8 output voltage (DC)	10	25	42	mVrms
Noise canceller block							
Gate time (1) t gate 1 [Design value]	τ gate1	PW = 1μsec, 100mVp-o, f = 1kHz PULSE-INPUT	The time when pin 4 voltage is Low at PIN4→100kΩ→GND.		9		μs
Gate time (1) t gate 2 [Design value]	τ gate2	PW = 1μsec, 100mVp-o, f = 1kHz PULSE-INPUT	The time when pin 48 voltage is Low at PIN48→100kΩ→GND.		84		μs
Noise sensitivity (1kHz, 1μs, PULSE INPUT)	NS	PW = 1μsec, f = 1kHz, PULSE-INPUT	Pulse input level to start the Gate operation (pin 4, pin 48 are low).		16		mVp-p

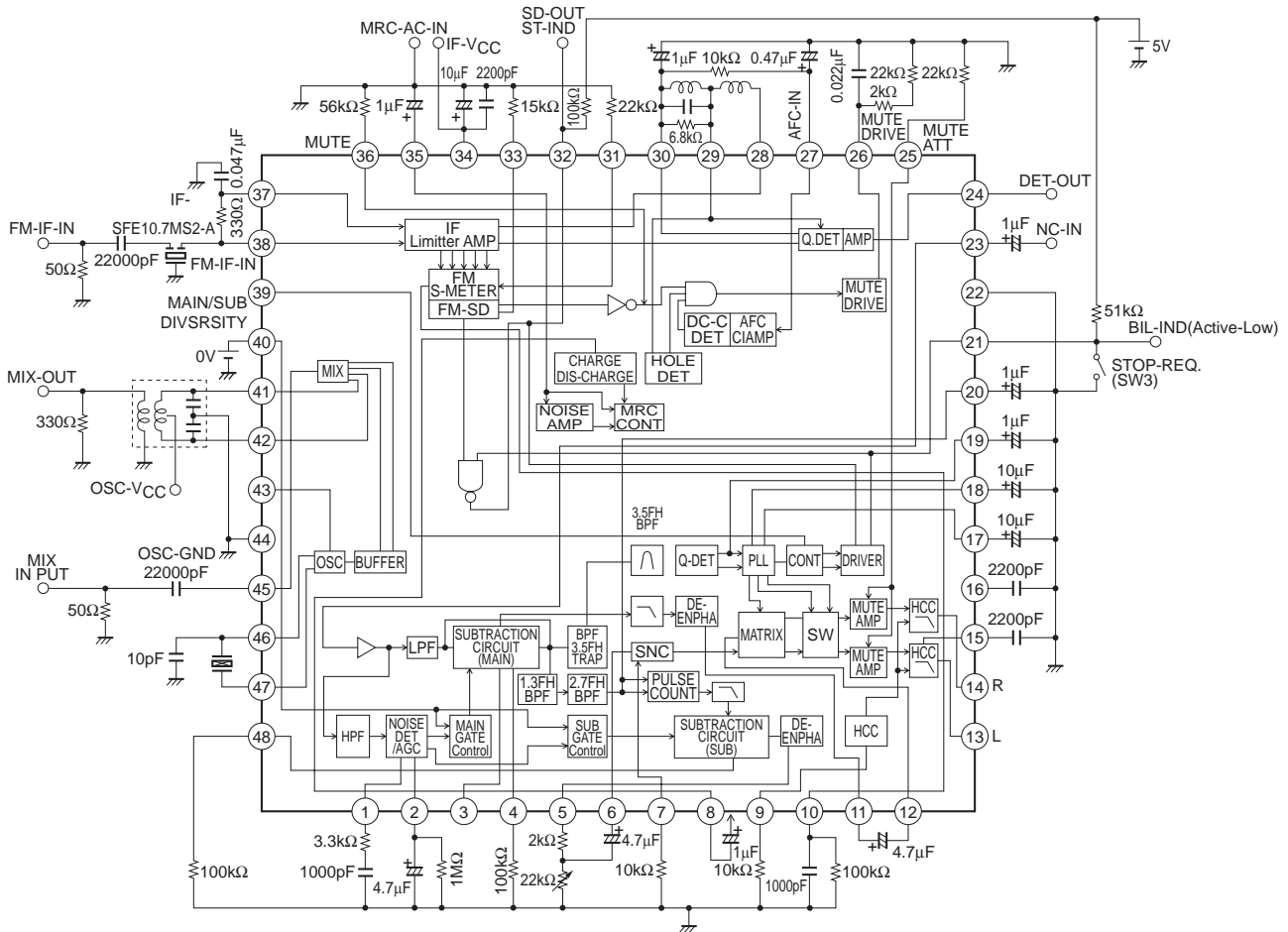
Pin Assignment



Pin function

Pin No.	Block	Function	Pin No.	Block	Function
1	NC	Noise sensitivity setting	25	IF	Setting of mute attenuation
2	NC	Noise AGC setting	26	IF	Mute drive output
3	NC	Low-Pass-Filter OUT	27	IF	AFC IN
4	NC	Hold circuit (MAIN)	28	IF	QD OUT
5	Multiplex	SUB demodulation signal output	29	IF	QD IN
6	Multiplex	MATRIX circuit SUB input	30	IF	VREF
7	Multiplex	SNC control input pin	31	IF	S meter shifter
8	MRC	MRC output pin	32	Multiplex	ST. indicator and SD output/ST
9	Multiplex	HCC control input pin	33	IF	SD.ADJ.
10	Multiplex	S meter output	34		V _{CC} (Sound Multiplex)
11	Multiplex	MAIN demodulation signal output	35	IF	S meter output (for MRC)
12	Multiplex	MATRIX circuit MAIN input	36	IF	Mute On ADJ.
13	Multiplex	Lch output	37	IF	IF-BYPASS
14	Multiplex	Rch output	38	IF	IF input
15	Multiplex	Capacitor (L) for High-Cut	39	Multiplex	BLL. Mode selector pin
16	Multiplex	Capacitor (R) for High-Cut	40	NC	Density gate control
17	Multiplex	Q signal detection (BIL)	41	FE	MIX output
18	Multiplex	Q signal detection (ST)	42	FE	MIX output
19	Multiplex	Q signal filter output	43		V _{CC} (OSC)
20	Multiplex	SUB signal filter output	44		GND(OSC)
21	Multiplex	BIL.IND and STOP request	45	FE	MIX input
22		GND (Sound Multiplex)	46	FE	OSC
23	NC	Noise canceller input	47	FE	OSC
24	IF	IF detection output	48	NC	Hold circuit (SUB)

Block Diagram and Test Circuit



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