D3005, DECEMBER 1986 - REVISED JULY 1989

- Each Device Drives 32 Lines
- 180-V Open-Drain Parallel Outputs
- 220-mA Parallel Output Sink Current Capability
- CMOS-Compatible Inputs
- Strobe Input Provided
- Serial Data Output for Cascade Operation
- Inputs Have Built-in Electrostatic Discharge Protection

description

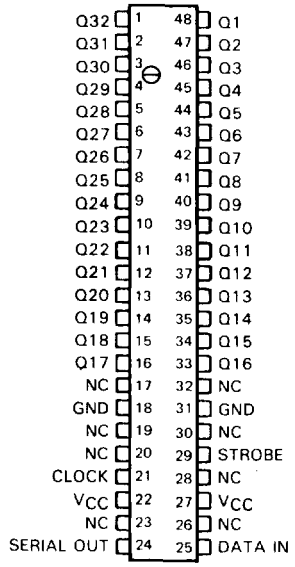
The SN751506 and the SN751516 are monolithic integrated circuits designed to drive the scan lines of a dc plasma panel display. The SN751516 pin sequence is reversed from the SN751506 for ease in printed circuit board layout.

Each device consists of a 32-bit shift register and 32 OR gates. Serial data is entered into the shift register on the high-to-low transition of the clock input. When STROBE is low, all Q outputs are in the off-state. Outputs are open-drain JFET transistors with a breakdown voltage in excess of 180 V. The outputs have a 220-mA sink current capability in the on state. Only one Q output should be allowed to be in the on state at a time.

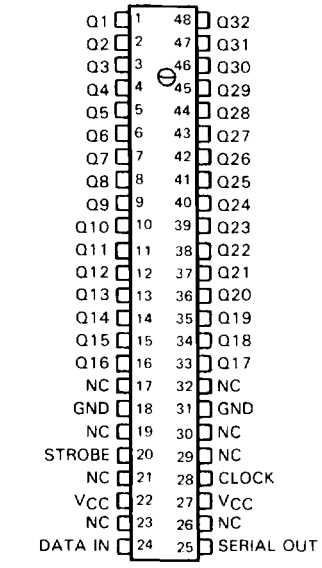
Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the strobe input. All inputs are CMOS compatible with ESD protection built in.

The SN751506 and SN751516 are characterized for operation from 0°C to 70°C.

SN751506 . . . FT PACKAGE
(TOP VIEW)

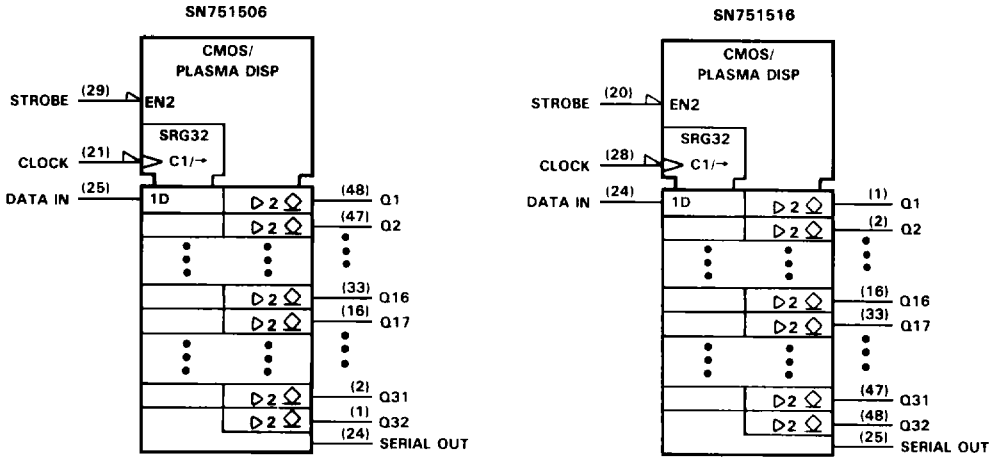


SN751516 . . . FT PACKAGE
(TOP VIEW)



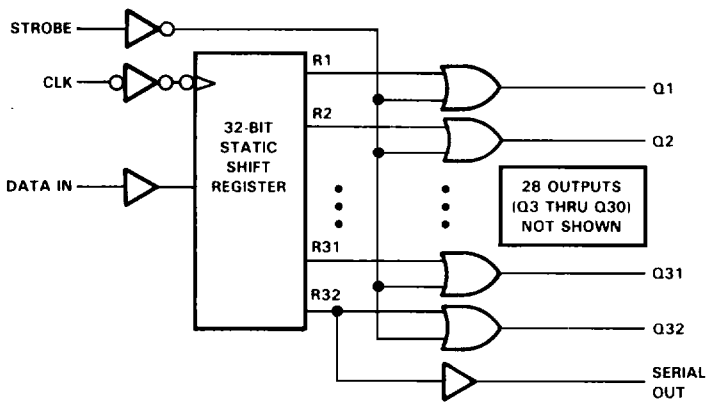
NC – No internal connection

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

FUNCTION	CONTROL INPUTS		SHIFT REGISTERS	OUTPUTS	
	CLOCK	STROBE	R1 THRU R32	SERIAL	Q1 THRU Q32
LOAD	↓	X	Load and shift‡	R32	Determined by STROBE
	No↓	X	No change	R32	
STROBE	X	L	As determined above	R32	All high impedance
	X	H		R32	R1 thru R32

H = high level, L = low level, X = irrelevant, ↓ = high to low transition.
‡ R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

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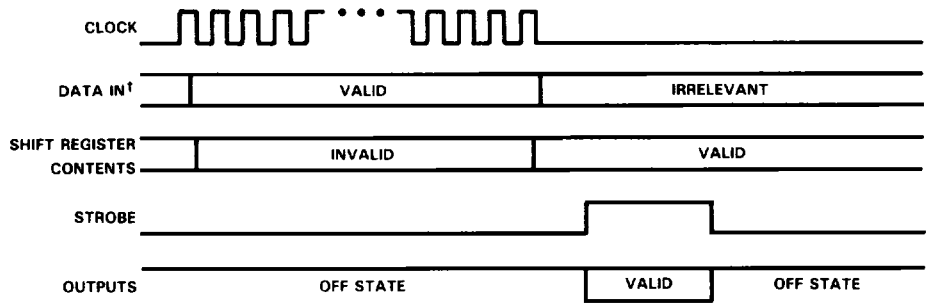
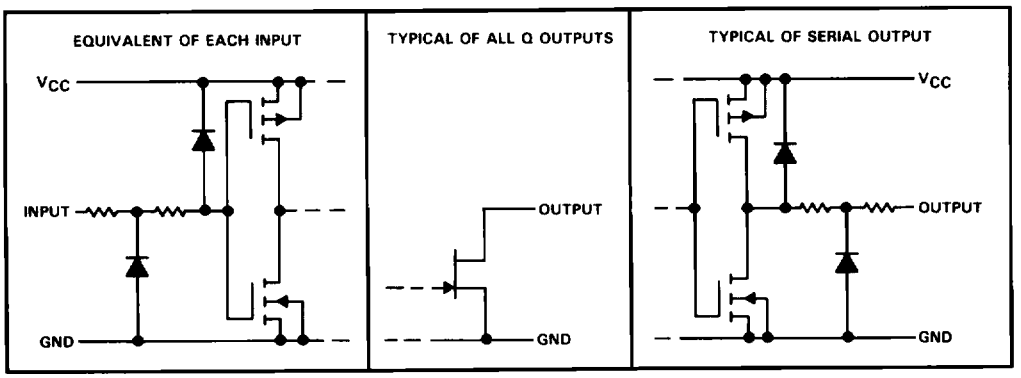
typical operating sequence



†Only 1 bit in 32 should be low in the input data.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	−0.4 V to 7 V
On-state Q output voltage, V_O	−0.4 V to 125 V
Off-state Q output voltage, V_O	−0.4 V to 180 V
Input voltage	−0.4 V to V_{CC} + 0.4 V
Serial output voltage	−0.4 V to V_{CC} + 0.4 V
Q output on-state time duration (see Note 2)	100 μs
Q output duty cycle (see Note 2)	1/200
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 3)	1025 mW
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to GND.
2. Only one Q output should be on at a time.
3. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4	5	6	V
Peak on-state Q output voltage, $V_{O(on)}$				110	V
High-level input voltage, V_{IH}	V_{CC} = 4 V	3.2			V
	V_{CC} = 6 V	4.8			
Low-level input voltage, V_{IL}	V_{CC} = 4 V			0.8	V
	V_{CC} = 6 V			1.2	
Output current, I_O (T_A = 25°C)				220	mA
Clock frequency, f_{clock}				200	kHz
Pulse duration, CLOCK high or low, t_{wCLK}		1.5†			μs
Pulse duration, DATA, t_{wD}		5			μs
Pulse duration, STROBE, t_{wSTRB}		2			μs
Setup time, DATA IN before CLOCK↓, t_{su}		1			μs
Hold time, DATA IN after CLOCK↓, t_h		1.2			μs
Operating free-air temperature, T_A		0		70	°C

† The minimum clock period is 5 μs.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	SERIAL OUT	I_{OH} = −0.1 mA	4.5			V
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 180 mA		6	10	V
		SERIAL OUT	I_{OL} = 0.1 mA			0.5	
$I_{O(off)}$	Off-state output current	Q outputs	V_{OH} = 110 V			1	μA
I_{OL}	Low-level output current	Q outputs	V_{OL} = 16 V	220			mA
I_{IH}	High-level input current		V_I = V_{CC}			1	μA
I_{IL}	Low-level input current		V_I = 0			−1	μA
C_i	Input capacitance					15	pF
I_{CC}	Supply current		All Q outputs off			1	mA
			One Q output on		20	40	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, CLOCK to SERIAL OUT	C_L = 15 pF		0.2	0.5	μs
t_{DHL}	Delay time, high-to-low-level Q output from STROBE or CLOCK inputs	C_L = 150 pF, R_L = 470 Ω, See Figures 2 and 3		0.2‡	0.6	μs
t_{DLH}	Delay time, low-to-high-level Q output from STROBE or CLOCK inputs			0.35‡	1	μs
t_{THL}	Transition time, high-to-low-level Q output			0.1	0.3	μs
t_{TLH}	Transition time, low-to-high-level Q output			0.35	1	μs

‡ Typical values are for clock inputs. Typical from strobe inputs will be less.

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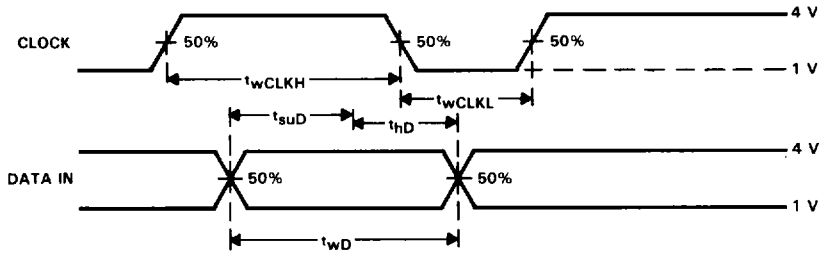


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

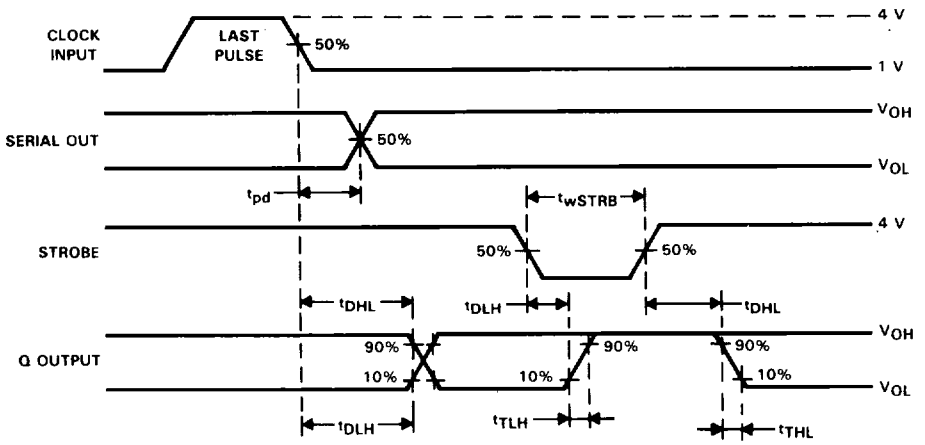
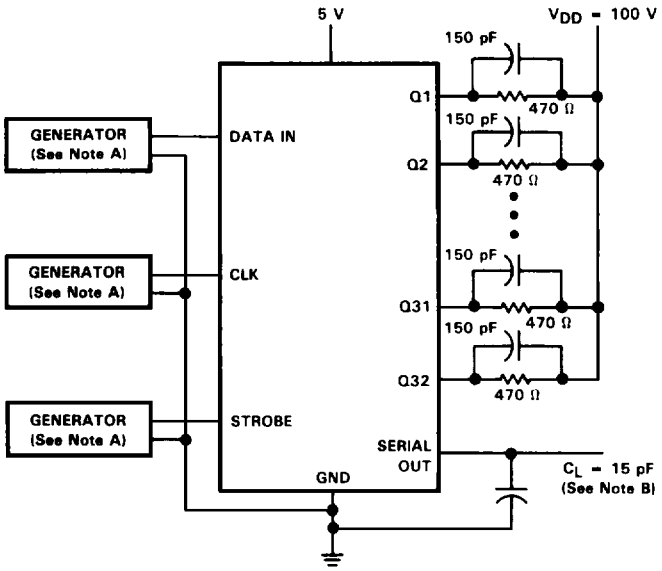


FIGURE 2. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w 1.25 μs, PRR ≤ 200 kHz, t_r ≤ 30 ns, t_f ≤ 30 ns, Z_o = 50 Ω.

B. C_L includes probe and jig capacitance.

FIGURE 3. TEST CIRCUIT

TYPICAL CHARACTERISTICS

LOW-LEVEL Q OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

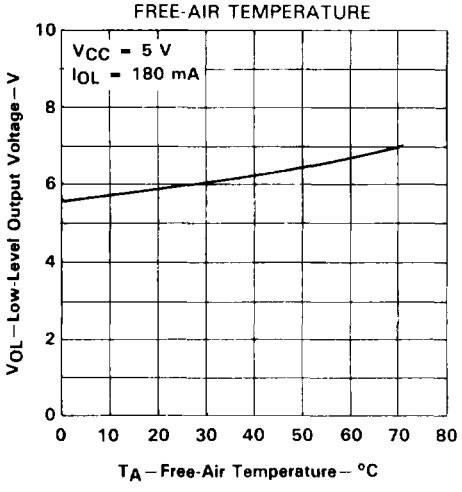


FIGURE 4

LOW-LEVEL Q OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

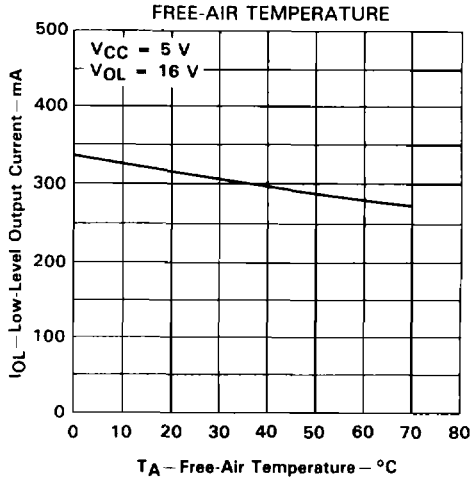


FIGURE 5

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

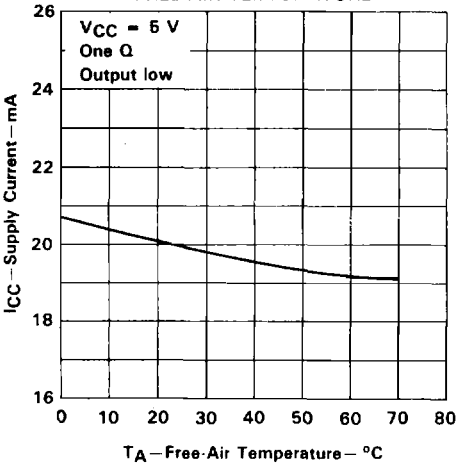


FIGURE 6

PROPAGATION DELAY TIME,
CLOCK TO SERIAL OUTPUT
vs
FREE-AIR TEMPERATURE

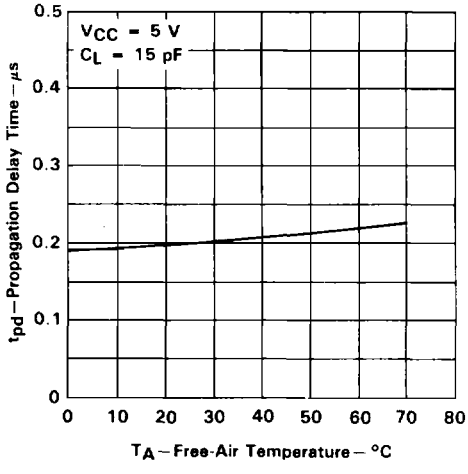


FIGURE 7

TYPICAL CHARACTERISTICS

DELAY TIME,
HIGH-TO-LOW-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

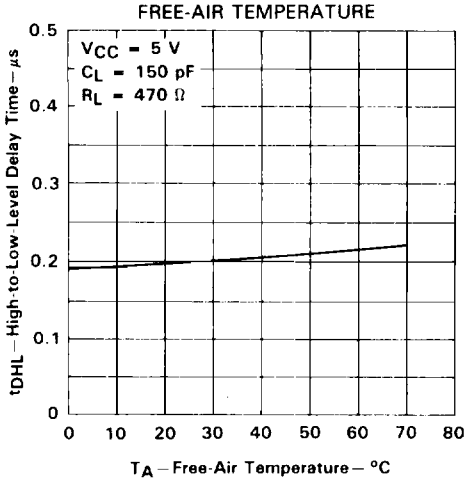


FIGURE 8

DELAY TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

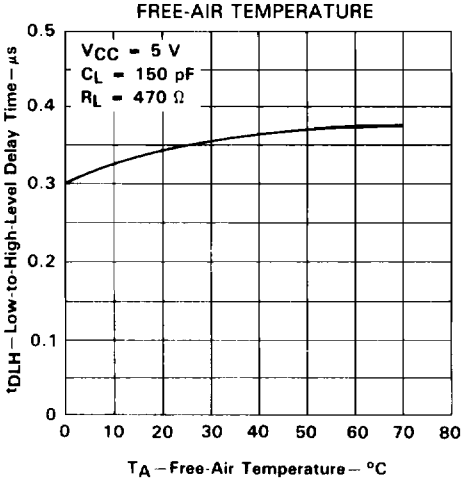


FIGURE 9

TRANSITION TIME,
HIGH-TO-LOW-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

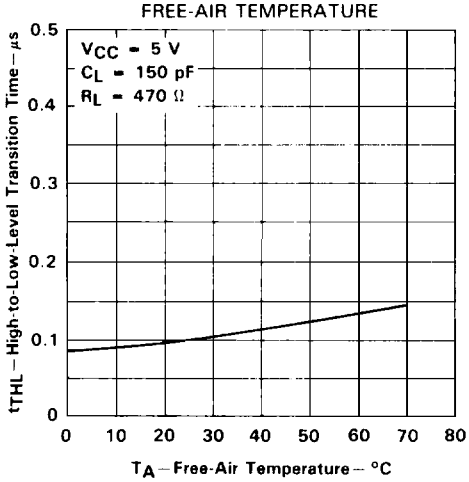


FIGURE 10

TRANSITION TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

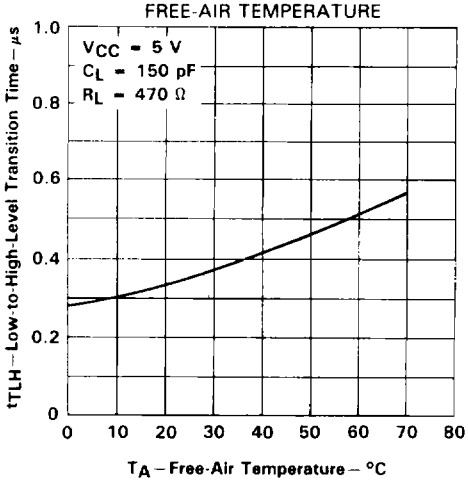


FIGURE 11