

54FCT273 Octal D-Type Flip-Flop

General Description

The 'FCT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

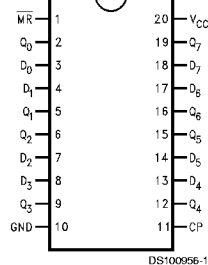
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'FCT377 for clock enable version
- See 'FCT373 for transparent latch version
- See 'FCT374 for TRI-STATE® version
- Output sink capability of 32 mA, source capability of 12 mA
- TTL input and output level compatible
- CMOS power consumption
- Standard Microcircuit Drawing (SMD) 5962-8765601

Ordering Code

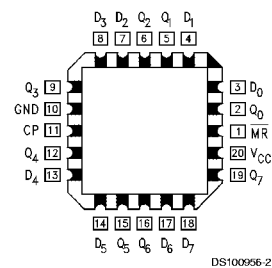
Military	Package Number	Package Description
54FCT273DMQB	J20A	20-Lead Ceramic Dual-In-Line
54FCT273FMQB	W20A	20-Lead Cerpack
54FCT273LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams

Pin Assignment for DIP and Flatpack



Pin Assignment for LCC



Pin Names	Description
D ₀ -D ₇	Data Inputs
\overline{MR}	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
Q ₀ -Q ₇	Data Outputs

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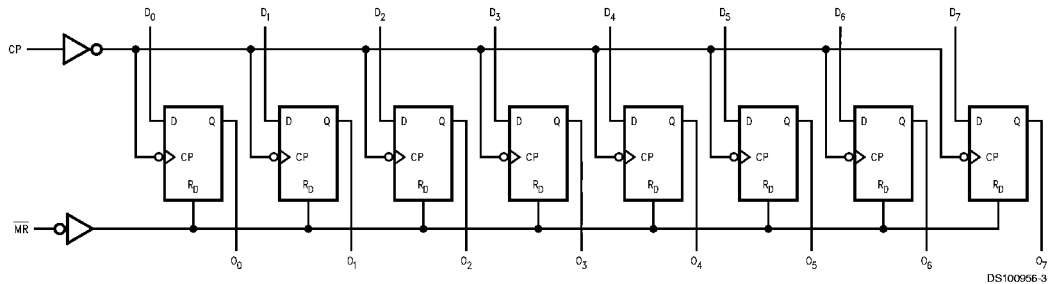
Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	\overline{MR}	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load "1"	H	N	h	H
Load "0"	H	N	l	L

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial
N = LOW-to-HIGH clock transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to +4.75V
in the HIGH State	-0.5V to V _{CC}

Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current (Across Comm Operating Range)	-500 mA
Over Voltage Latchup	V _{CC} + 4.5V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	FCT240		Units	V _{CC}	Conditions
		Min	Max			
V _{IH}	Input HIGH Voltage	2.0		V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage	0.8		V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage	-1.2		V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54FCT	4.3	V	Min	I _{OH} = -300 μA
		54FCT	2.4	V	Min	I _{OH} = -12 mA
V _{OL}	Output LOW Voltage	54FCT	0.2	V	Min	I _{OL} = 300 μA
		54FCT	0.5	V	Min	I _{OL} = 32 mA
I _{IH}	Input HIGH Current	5		μA	Max	V _{IN} = 5.5V
I _{IL}	Input LOW Current	-5		μA	Max	V _{IN} = 0.0V
I _{OS}	Output Short-Circuit Current	-60		mA	Max	V _{OUT} = 0.0V
I _{CCQ}	Power Supply Current	1.5		mA	Max	V _{IN} = 0.2V or V _{IN} = 5.3V
ΔI _{CC}	Power Supply Current	2.0		mA	Max	V _{IN} = 3.4V
I _{CCT}	Total Power Supply Current	6.0		mA	Max	V _{IN} = 3.4V or V _{IN} = GND, \overline{OE} = GND, f _i = 10Mhz, outputs open, one bit toggling - 50% duty cycle
		4.0		mA	Max	V _{IN} = 5.3V or V _{IN} = 0.2V, \overline{OE} = GND, f _i = 10Mhz, outputs open, one bit toggling - 50% duty cycle
I _{CCD}	Dynamic I _{CC}	0.25		mA/MHz	Max	Outputs Open, \overline{OE} = GND, One Bit Toggling, 50% Duty Cycle

AC Electrical Characteristics

Symbol	Parameter	54FCT		Units	Fig. No.
		T _A = -55°C to +125°C			
		V _{CC} = 4.5V to 5.5V			
		C _L = 50 pF			
		Min	Max		
t _{PLH}	Propagation Delay	2.0	15.0	ns	Figures 2, 5
t _{PHL}	CP to O _n	2.0	15.0		
t _{PHL}	Propagation Delay	2.0	15.0	ns	Figures 2, 5
	M \overline{R} to O _n				

AC Operating Requirements

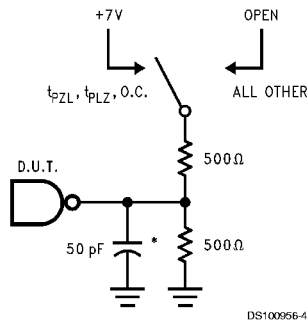
Symbol	Parameter	54FCT		Units	Fig. No.
		$T_A = -55^\circ\text{C to }+125^\circ\text{C}$ $V_{CC} = 4.5\text{V to }5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW D_n to CP	3.5		ns	Figure 6
$t_s(\text{L})$		3.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW D_n to CP	2.5		ns	Figure 6
$t_h(\text{L})$		2.5			
$t_w(\text{H})$	Pulse Width, CP, HIGH or LOW	7.0		ns	Figure 2
$t_w(\text{L})$		7.0			
$t_w(\text{L})$	Master Reset Pulse Width, LOW	7.0		ns	Figure 2
t_{REC}	Recovery Time MR to CP	5.0		ns	Figure 6

Capacitance

Symbol	Parameter	Max	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	10	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 3)	Output Capacitance	12	pF	$V_{CC} = 5.0\text{V}$

Note 3: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

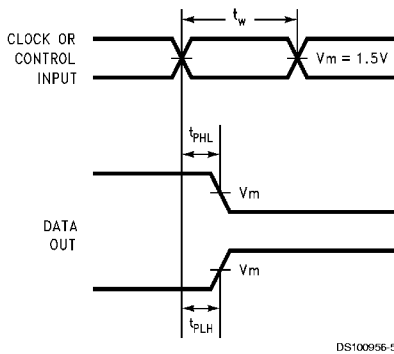


FIGURE 2. Propagation Delay, Pulse Width Waveforms

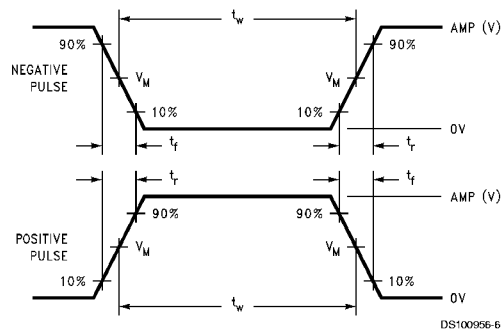


FIGURE 3. $V_M = 1.5V$ Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 4. Test Input Signal Requirements

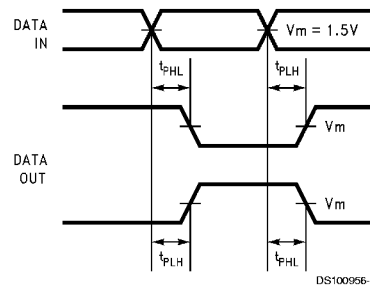


FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

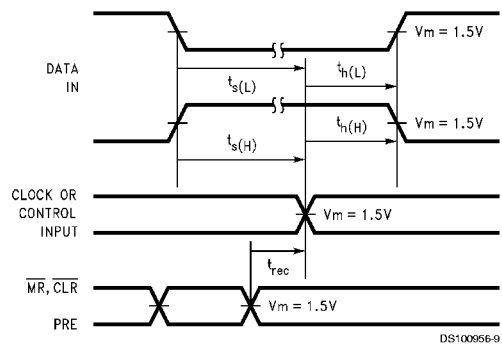
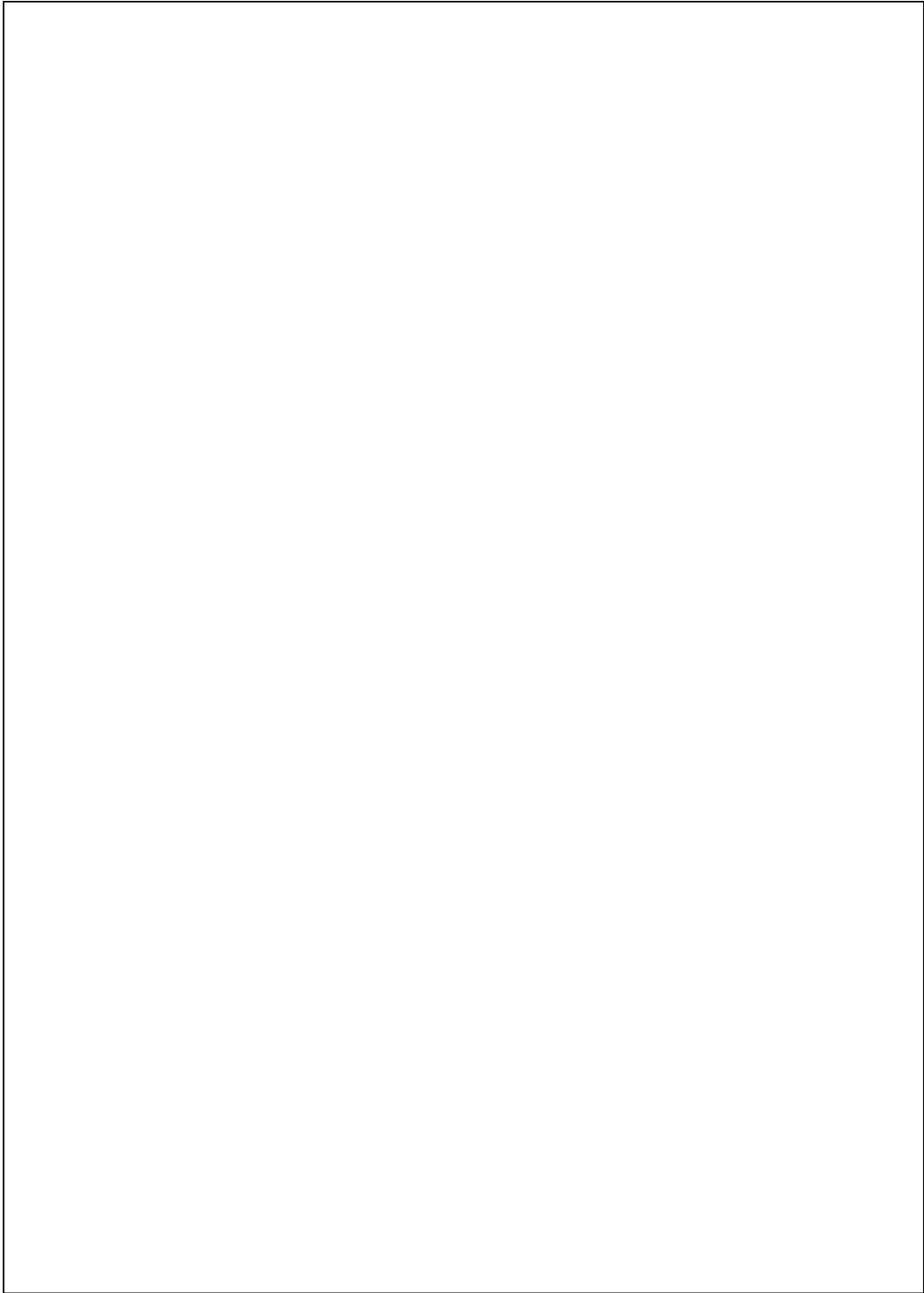
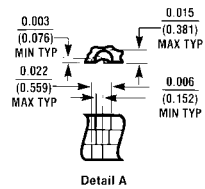
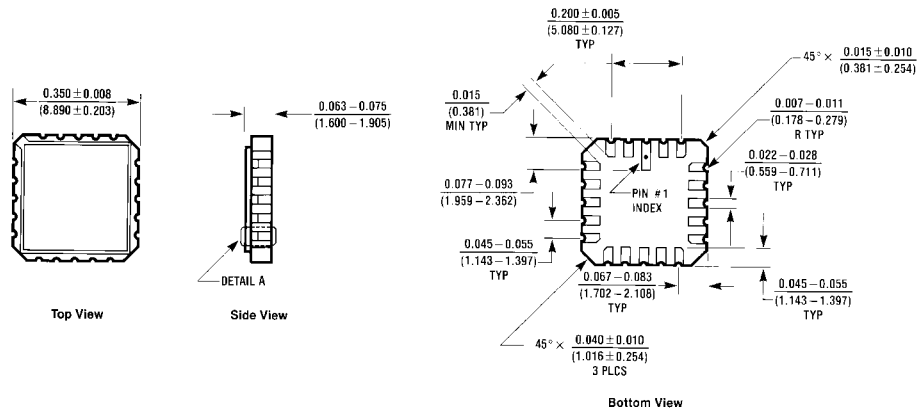


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

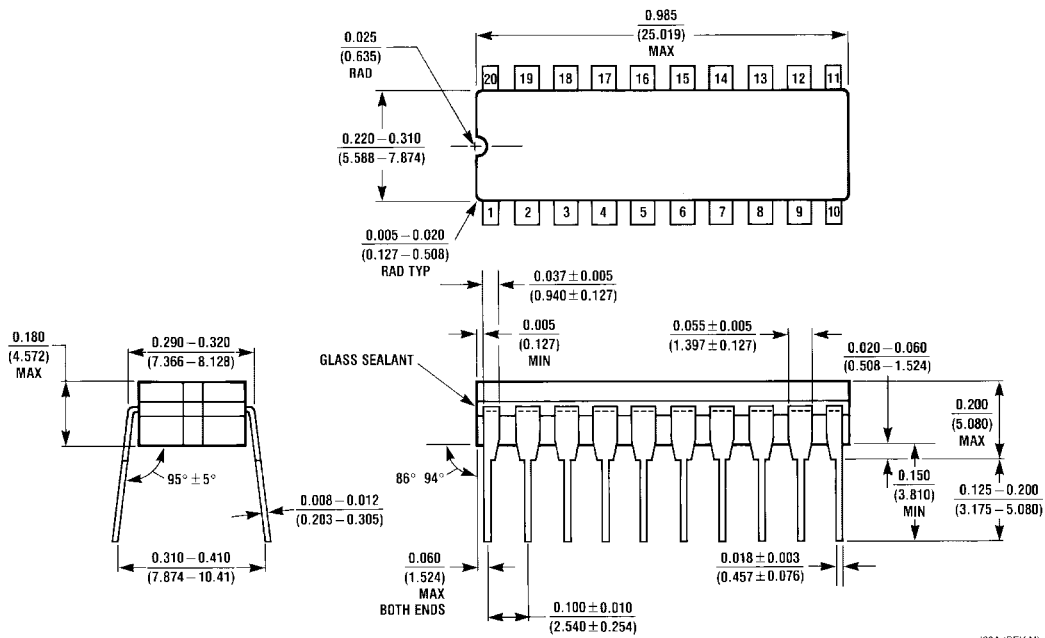


Physical Dimensions inches (millimeters) unless otherwise noted



L20A (REV D)

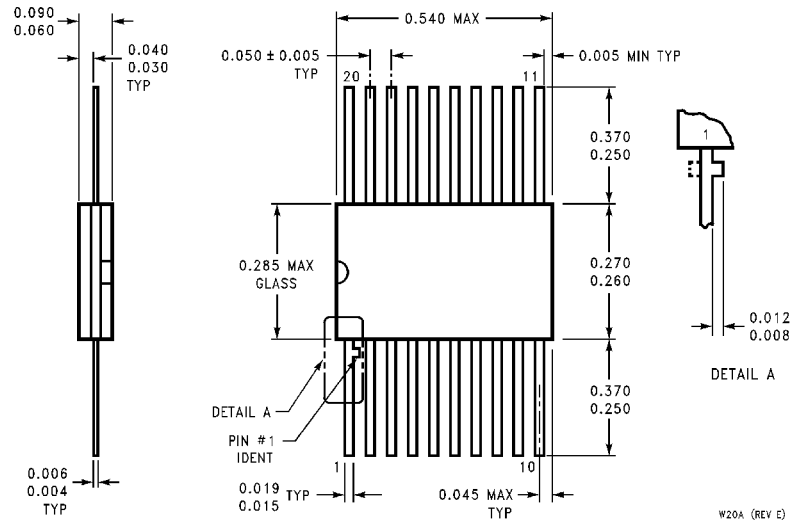
**20-Terminal Ceramic Chip Carrier (L)
 NS Package Number E20A**



J20A (REV M)

**20-Lead Ceramic Dual-In-Line (D)
 NS Package Number J20A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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